PCI Express Architecture Configuration Space

Test Specification

Revision 4.0, Version 0.9

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Revision	Revision History	Date
1.0	Initial release for PCI Express 1.0a.	04/26/2004
1.1	Updated for PCI Express 1.1.	12/03/2006
2.0	Updated for PCI Express 2.0.	08/25/2008
2.0a	Updated to include 2.0 Test Specification errata and changes in the Errata for the PCI Express Base Specification Revision 2.0 document. Also, typographical, grammatical, and formatting errors were corrected.	06/19/2009
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1

1. Introduction

This document primarily covers PCI Express testing of all defined PCI Express device types and RCRBs for the standard Configuration Space mechanisms, registers, and features in Chapter 6 of the PCI Local Bus Specification (Base 3.x or earlier only) and Chapters 7, 9 (Base 4.x or later only), 10 (Base 4.x or later only) of the *PCI Express Base Specification* (some additional tested registers are described in other specifications that are referenced in the individual test description). This specification does not describe the full set of PCI Express tests for these devices.

For overall compliance, devices must also meet the requirements and tests described in the latest versions of the following documents as well as any other tests provided by the PCI-SIG:

PCI Express Architecture PHY Test Specification
PCI Express Architecture Platform Init/Config Test Specification
PCI Express Architecture Link Layer and Transaction Layer Test Specification

The test descriptions can be referenced to obtain specific details on how the specific registers will be tested. Test descriptions also list which device types are tested. Test descriptions include "The test *fails* if" sub-sections that provide a list of some of the specific conditions that would cause the test to fail. Some test descriptions also include The test *warns* if sub-sections that provide a list of some of the specific conditions that would cause the test to only issue a warning message. Test descriptions include a reference to the applicable specifications and the specification revision.

The test program supports a manual mode of operation, where the user is prompted to provide inputs required by the test. The test program may optionally support an automatic mode of operation, where parameters are used to provide inputs required by the test.

1.1. Document Conventions

Capitalization

Register names and the names of fields and bits in registers and headers are presented with the first letter capitalized and the remainder in lower case. Multiple word names have the first letter of each word capitalized.

Numbers and Number Bases

Hexadecimal numbers are written with a lower case "h" suffix, (e.g., FFFh and 80h). Hexadecimal numbers larger than four digits are represented with a space dividing each group of four digits, as in 1E FFFF FFFFh.

Binary numbers are written with a lower case "b" suffix, (e.g., 1001b and 10b). Binary numbers larger than four digits are written with a space dividing each group of four digits, as in 1000 0101 0010b.

Numbers with an "x" in them indicate that the position of the "x" in the number is a don't care value and can have any legal value for that number base (e.g., 1x00b represents both 1000b and 1100b).

All numbers without a suffix are decimal.

Special Characters

Square brackets are used to denote a test program internal variable. For example, [NAME] indicates an internal variable called "NAME" that would be used by the test program to store some test sequence specific information.

1.2. Coverage

The Configuration Space Test Consideration for the PCI Express Architecture covers items in Chapter 6 of the PCI Local Bus Specification (Base 3.x or earlier only) and Chapters 7, 9 (Base 4.x or later only), 10 (Base 4.x or later only) of the *PCI Express Specification* and configuration items from other specifications that apply to PCI Express devices.

Revision 1.0 of this document includes updates based on the *PCI Express Base Specification Revision 1.0a*.

Revision 1.1 of this document includes updates based on the *PCI Express Base Specification Revision 1.1*.

Revision 2.0 of this document includes updates based on the *PCI Express Base Specification Revision 2.0*.

Revision 2.0a of this document includes updates based on the document *Errata for the PCI Express Base Specification Revision 2.0*, dated Feb 27, 2009. For 2.0 compliance testing, two interpretations will be accepted, the original Base 2.0 specification requirement, and the updated Base 2.0 requirement that includes the 2.0 errata document. For future compliance testing, only the updated interpretation will be accepted.

Revision 3.0 of this document includes updates based on the *PCI Express Base Specification Revision 2.1*. This is equivalent to *PCI Express Base Specification Revision 2.0* (including Base 2.0 errata) plus all applicable ECNs to 2.0. In addition to this, it also includes updates based on various ECNs to the *PCI Express Base Specification Revision 2.1*. Since the ECNs to Base 2.1 are optional, a 2.1 compliant device may choose to implement or not implement any or all of these ECNs to Base 2.1. For 2.1 compliance testing, a device that implements any of these released ECNs to Base 2.1 will be tolerated by the test and will be considered to pass if it implements those specific ECNs to Base 2.1 correctly. This revision of this document also includes the *Single Root I/O Virtualization and Sharing Specification Revision 1.0* and any Base 1.x or Base 2.x device that implements SR-IOV features must comply with this revision of the specification.

Revision 3.0 of this document includes updates based on the *PCI Express Base Specification Revision 3.0*. This revision of this document also includes updates to the *Single Root I/O Virtualization and Sharing Specification Revision 1.1*. A Base 3.x device that implements SR-IOV features must comply with this revision of the specification. A Base 2.x device that implements SR-IOV features may comply with either this revision of the specification or the previous *Single Root I/O Virtualization and Sharing Specification Revision 1.0*. A Base 1.x device that implements SR-IOV features must comply with the previous *Single Root I/O Virtualization and Sharing Specification Revision 1.0*.

Revision 3.1 of this document includes updates based on the *PCI Express Base Specification Revision 3.1*. This is equivalent to *PCI Express Base Specification Revision 3.0* (including Base 3.0 errata) plus all applicable ECNs to 3.0, up to and including the Readiness Notifications (RN) ECN. In addition to this, it also includes updates based on various ECNs to the *PCI Express Base Specification Revision 3.1*. Since the ECNs to Base 3.1 are optional, a 3.1 compliant device may choose to implement or not implement any or all of these ECNs to Base 3.1. For 3.1 compliance testing, a device that implements any of these released ECNs to Base 3.1 will be tolerated by the test and will be considered to pass if it implements those specific ECNs to Base 3.1 correctly. This revision of this document also includes updates to the *Single Root I/O Virtualization and Sharing Specification Revision 1.1*. A Base 3.x device that implements SR-IOV features must comply with this revision of the specification. A Base 2.x device that implements SR-IOV features may comply with either this revision of the specification or the previous *Single Root I/O Virtualization and Sharing Specification Revision 1.0*. A Base 1.x device that implements SR-IOV features must comply with the previous *Single Root I/O Virtualization and Sharing Specification Revision 1.0*.

Revision 4.0 of this document includes updates based on the *PCI Express Base Specification Revision 4.0*. A Base 4.x device that implements SR-IOV features must comply with this revision of the specification. This revision of this document also includes updates to the *Single Root I/O Virtualization and Sharing Specification Revision 1.1*. A Base 3.x device that implements SR-IOV features must comply with this revision of the specification. A Base 2.x device that implements SR-IOV features may comply with either this revision of the specification or the previous *Single Root I/O Virtualization and Sharing Specification Revision 1.0*. A Base 1.x device that implements SR-IOV features must comply with the previous *Single Root I/O Virtualization and Sharing Specification Revision 1.0*.

Note: Register names and fields reflect those listed in the Base Specification revision applicable to the test document revision. The only exception is the Link Capabilities register bits 3-0, which are listed in this document as "Max Link Speed/Supported Link Speeds", to reflect its changed definition from Base 2.x to Base 3.x.

Note: The following Capability structures are not tested because they control the Configuration Space decoding and may interfere with system operation:

- Enhanced Allocation
- Flattening Portal Bridge

1.3. Test Options for Base Specification Revision

The Configuration Space Test Consideration for the PCI Express Architecture covers several different revisions of the Base Specification. In manual mode, a user prompt is used to configure the test to a specific Base Specification Revision. In automatic mode, the test program shall accept a parameter that specifies the Base Specification Revision to be used by the test. The highest Base Specification Revision supported by the test program is the selection used in automatic mode, when no parameter is specified. The requirements for each of these individual Base Specification Revision selection options may change with each revision of this document, as may the number of Base Specification Revision selection options. The Base Specification Revision selection options and their requirements are stated below.

If implemented by the DUT, ECNs to the indicated Base Specification will be tested and will result in a fail if the DUT does comply with the ECN. If not implemented by the DUT, ECNs to the

indicated Base Specification will not affect pass/fail. The ECNs are listed in the individual test descriptions.

"Test against either 1.1 or 2.0 Spec"

This selection will consider a DUT to pass if it complies with the following (including either of the following Base Specifications):

- *PCI Express Base Specification Revision 1.1* with *Errata for the PCI Express Base Specification Revision 1.1* (dated Feb 8, 2007)
- *PCI Express Base Specification Revision 2.0* with *Errata for the PCI Express Base Specification Revision 2.0* (dated Feb 27, 2009)
- *Single Root I/O Virtualization and Sharing Specification Revision 1.0* (optional)

"Test against 2.0 Spec Only"

This selection will consider a DUT to pass if it complies with the following:

- *PCI Express Base Specification Revision 2.0* with *Errata for the PCI Express Base Specification Revision 2.*0 (dated Feb 27, 2009)
- *Single Root I/O Virtualization and Sharing Specification Revision 1.0* (optional)

"Test against 2.1 or 2.0 Spec"

This selection will consider a DUT to pass if it complies with the following (including either of the following Base Specifications):

- *PCI Express Base Specification Revision 2.0* with *Errata for the PCI Express Base Specification Revision 2.0* (dated Feb 27, 2009)
- *PCI Express Base Specification Revision 2.1*
- *Single Root I/O Virtualization and Sharing Specification Revision 1.1* or *Revision 1.0* (optional)

"Test against 3.0 Spec Only"

This selection will consider a DUT to pass if it complies with the following:

- *PCI Express Base Specification Revision 3.0*
- *Single Root I/O Virtualization and Sharing Specification Revision 1.1* (optional)

"Test against 3.1 or 3.0 Spec"

This selection will consider a DUT to pass if it complies with the following (including either of the following Base Specifications):

- *PCI Express Base Specification Revision 3.0* with *Errata for the PCI Express Base Specification Revision 3.0* (dated October 23, 2014)
- *PCI Express Base Specification Revision 3.1*
- *Single Root I/O Virtualization and Sharing Specification Revision 1.1* (optional)

"Test against 4.0 Spec Only"

This selection will consider a DUT to pass if it complies with the following:

- *PCI Express Base Specification Revision 4.0*

1.4. Function Under Test Discovery

The test program shall test hardware at the function level of granularity. This means that the test will run on an individual function under test identified by a unique Bus Number/Device Number/Function Number address. In manual mode, the test program shall provide the user with a selection prompt to allow them to choose the specific function under test to run the test on. The user selection prompt will group each function under test by its reported Device/Port Type (PCI Express Capability). In automatic mode, the test program shall accept a parameter that identifies the function under test, providing that the specified parameter indicates a function that is present in the topology. BDF = 0000h is the selection used in automatic mode, when no parameter is specified.

1.4.1. Discovery of Basic Functions, ARI Functions, Base Functions, Physical Functions, and Virtual Functions

The test program shall scan all supported Bus Numbers (0-256), all supported Device Numbers (0-31), and all supported Function Numbers (0-7).

(Note: Some systems limit the maximum number of supported buses to less than 256. The test program shall use appropriate SBIOS ACPI tables to determine the maximum number of supported buses before beginning the scan.)

(Note: All Function Numbers shall be scanned regardless of the setting of the Multi-Function Device bit in the Header Type register. This ensures that functions that do not correctly implement the Multi-function bit will still be selectable as a function under test.)

A device that supports ARI may support up to 256 functions. In order to do this, the standard Device Number field is no longer used, and the Function Number field now goes from 0-255. (Test software can still use the Device Number field as a concept to allow the same algorithm to handle both non-ARI and ARI functions.)

The test program creates a 16 bit value of Bus number/Device number/Function number [BDF] and increments it by 1 for each pass through the scan. The [BDF] value consists of: bits 15-8 = Bus Number; bits 7-3 = Device Number; bits 2-0 = Function Number.

A physical function (PF) that support SR-IOV may contain virtual functions (VFs) that are hidden by default. Once the PF is programmed to enable the VFs, there may be up to 65536 VFs visible. VFs require special VF aware detection algorithms, as they always return Vendor ID of FFFFh and Device ID of FFFFh. Any number of VFs greater than 256, require additional Bus Numbers to be available to the VF, and the bus hierarchy must be programmed to route the additional bus numbers to the path leading to the VFs.

The scan starts with [BDF] as 0000h.

a. Set the ARI Downstream Enabled Flag [ARIDEF] to 0.

b. Read back a WORD at location 00h (Vendor ID register) in Configuration Space and if 0001h (CRS Software Visibility notification) is found, continue reading this location until a value other than 0001h is found. If a value other than 0001h is not found within 1 second, then this [BDF]

location is broken (though it could be a detected later as part of PF detection) and the scan restarts at step a) with the next [BDF] value.

c. Read back a WORD at location 00h (Vendor ID register) in Configuration Space and if FFFFh is found, this [BDF] location is empty (though it could be a VF which will be detected later as part of PF detection) and the scan restarts at step a) with the next [BDF] value.

d. Examine the Capability ID field for each of the function's Capability structures. Determine how many instances of the Capability ID of 10h (PCI Express Capability) are found. If one is found, this [BDF] location contains a PCI Express function that may be selected as the function under test. If none are found, this [BDF] location is not a PCI Express function and the scan restarts at step a) with the next [BDF] value.

e. Having found the PCI Express Capability at this [BDF], read a DWORD at offset 02h (PCI Express Capabilities register) in the PCI Express Capability structure and use the Device/Port Type field value to identify the PCI Express type that the function will be listed under, in manual mode, in the user selection prompt. Any functions reporting reserved encodings for Device/Port Type must be listed, in manual mode, under the category "Unknown" in the user selection prompt. These can still be selected as the function under test.

f. If the current Function Number is 0, then examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 000Eh (ARI Extended Capability) are found. If none are found, this [BDF] location does not contain an ARI Extended Capability, so skip to step h).

g. If an ARI Extended Capability was found, then find the immediate downstream port connected to this function (the device at the other end of the link for this function) and write ARI Forwarding Enable (Device Control 2 register) to 1 and also set [ARIDEF] to 1. (This will allow an ARI capable downstream port to forward all Device Numbers on this port. This will cause any ARI functions on this link to become detectable by test software. Setting this bit on a non-ARI capable downstream port will not cause any change since this bit would not be implemented on such a port.) Note: It is important that this setting remain unchanged for this port for the remainder of all testing, otherwise the ARI functions will disappear. If a test specifically causes this bit to be cleared (when it was previously set in this step), the test must restore the set value before proceeding. This is important for any test that would cause any downstream port with this bit set, to revert to its default values.

h. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0010h (SR-IOV Extended Capability) are found. If none are found, this [BDF] location does not contain a SR-IOV Extended Capability, so skip to step dd).

i. If a SR-IOV Extended Capability was found, then write ARI Capable Hierarchy (SR-IOV Control register) as follows:
 - if [ARIDEF] is 1, then write ARI Capable Hierarchy to 1
 - if [ARIDEF] is 0, then write ARI Capable Hierarchy to 0

 (This will control whether the device will decode up to 8 VFs per bus number, or up to 256 VFs per bus number. Note: It is important that this setting remain unchanged for the lowest numbered PF in the device for the remainder of all testing, otherwise the VF functions may disappear from their current location. If a test specifically causes this field to be changed (when it was previously programmed in this step), the test must restore the programmed value before

proceeding. This is important for any test that would cause any PF with this programmed field to revert to its default values.

j. If a SR-IOV Extended Capability was found, read a WORD at offset 0Eh (TotalVFs register) in the SR-IOV Extended Capability. If this value is 0000h, this PF does not contain any VFs, so skip to step dd).

k. If the value read from TotalVFs is non-zero, write this value to the WORD at offset 10h (NumVFs). Then write VF Enable (SR-IOV Control register) to 1. (This will cause all VF functions in this PF between 1 and the value in InitialVFs to become detectable by test software as long as they remain in the Active.Available state.) Note: It is important that these settings remain unchanged for this PF for the remainder of all testing, otherwise the VF functions will disappear. If a test specifically causes this field to be changed or this bit to be cleared (when they were previously programmed in this step), the test must restore the programmed values before proceeding. This is important for any test that would cause any PF with this programmed field and this bit set, to revert to its default values.

l. If the value read from InitialVFs is not less than the value read from TotalVFs, then all VFs are already in the Active.Available state, so skip to step t.

m. If TotalVFs register returns a value greater than 0 and VF Migration Capable (SR-IOV Capabilities register) returns 1, then read VF Migration State Offset and VF Migration State BIR (both in VF Migration State Array Offset register) and calculate the VF Migration State Array starting address value and record it in Migration State Array Address [MSAA] as follows: [MSAA] = VF Migration State Array Offset value + the value returned in the BAR indicated by the value in VF Migration State BIR.

n. After enabling Memory Space access for the PF, set the Inactive VF Number [IVFN] to the value in InitialVFs + 1.

o. If [IVFN] is less than or equal to the value in TotalVFs, read a byte from the Memory Space address given by: [MSAA] + ([IVFN] – 1). Use this value masking out the lower two bits and combine it with the Migration State value of 01b (Dormant.MigrateIn). Write this new byte (bits 7-2 containing read back value, bits 1-0 containing 01b) back to the same address.

p. Wait 100 ms.

q. If [IVFN] is less than or equal to the value in TotalVFs, read a byte from the Memory Space address given by: [MSAA] + ([IVFN] – 1). Use this value masking out the lower two bits and combine it with the Migration State value of 11b (Active.Available). Write this new byte (bits 7-2 containing read back value, bits 1-0 containing 11b) back to the same address. (This will cause all VF functions in this PF between InitialVFs and the value in TotalVFs to become detectable by test software as long as they remain in the Active.Available state). Note: It is important that these settings remain unchanged for this PF for the remainder of all testing, otherwise the VF functions will disappear. If a test specifically causes this field to be changed (when they were previously programmed in this step and the previous two steps), the test must restore the programmed values, using the same programming sequence before proceeding. This is important for any test that would cause any PF with this programmed field, to revert to its default values.

r. Wait 100 ms.

s. Increment [IVFN] by adding 1, and if the new [IVFN] is less than or equal to the value in TotalVFs, repeat steps o-s).

t. If [ARDEF] is 0 and the value written to NumVFs is greater than 7, then the test program must ensure that additional bus numbers are available on the immediate downstream port connected to this function (the device at the other end of the link for this function). The Subordinate Bus Number register for the downstream port device must return a value that includes the required number of bus numbers for all the VFs (required number of bus numbers = TotalVFs divided by 7, rounded up to the next integer value). If the number of allocated bus numbers (number of allocated bus numbers = Subordinate Bus Number minus Secondary Bus Number) is not sufficient, additional bus numbers must be allocated to this specific hierarchy (including any other devices in the upstream hierarchy), so that all the VFs may be visible. In doing so, some bus numbers may need to be re-allocated, which may require a partial or complete rescan of the Bus Numbers. Note: It is It is important that these bus number allocations remain unchanged for the remainder of all testing, otherwise some VF functions will disappear. If a test specifically causes these bus number allocations to change, the test must restore the programmed allocation before proceeding.

u. If [ARDEF] is 1 and the value written to NumVFs is greater than 255, then the test program must ensure that additional bus numbers are available on the immediate downstream port connected to this function (the device at the other end of the link for this function). The Subordinate Bus Number register for the downstream port device must return a value that includes the required number of bus numbers for all the VFs (required number of bus numbers = TotalVFs divided by 255, rounded up to the next integer value). If the number of allocated bus numbers (number of allocated bus numbers = Subordinate Bus Number minus Secondary Bus Number) is not sufficient, additional bus numbers must be allocated to this specific hierarchy (including any other devices in the upstream hierarchy), so that all the VFs may be visible. In doing so, some bus numbers may need to be re-allocated, which may require a partial or complete rescan of the Bus Numbers. Note: It is It is important that these bus number allocations remain unchanged for the remainder of all testing, otherwise some VF functions will disappear. If a test specifically causes these bus number allocations to change, the test must restore the programmed allocation before proceeding.

v. If a SR-IOV Extended Capability was found, read a WORD at offset 14h (First VF Offset register) in the SR-IOV Extended Capability.

w. If a SR-IOV Extended Capability was found, read a WORD at offset 16h (VF Stride register) in the SR-IOV Extended Capability.

x. Set VF Number [VFN] to 1.

y. Using the current [BDF] value, calculate the VF location as follows: [VF BDF] = ([BDF] + First VF Offset + (([VFN]-1) * VF Stride)) mod 2 ** 16.

z. Read back a WORD at location 00h (Vendor ID register) in Configuration Space and if 0001h (CRS Software Visibility notification) is found, continue reading this location until a value other than 0001h is found. If a value other than 0001h is not found within 1 second, then this [VF BDF] location is broken so ignore it and skip to step cc.

aa. Examine the Capability ID field for each of the function's Capability structures. Determine how many instances of the Capability ID of 10h (PCI Express Capability) are found. If one is found, this [VF BDF] location contains a PCI Express function that may be selected as the function

under test. If none are found, this [VF BDF] location is not a PCI Express function so skip to step cc.

bb. Having found the PCI Express Capability at this [VF BDF], read a DWORD at offset 02h (PCI Express Capabilities register) in the PCI Express Capability structure and use the Device/Port Type field value to identify the PCI Express type that the VF will be listed under, in manual mode, in the user selection prompt. Any VFs reporting reserved encodings for Device/Port Type must be listed under, in manual mode, the category "Unknown" in the user selection prompt. These can still be selected as the function under test. Any VFs reporting non-Endpoint encodings for Device/Port Type must be listed under, in manual mode, their reported category in the user selection prompt. These can still be selected as the function under test.

cc. Increment [VFN] by 1, and if the new [VFN] is less than the value in NumVFs do the following:
- If [ARDEF] is 0 and ([VF BDF] = ([BDF] + First VF Offset + (([VFN]-1) * VF Stride)) mod 2 ** 16) does not produce a carry out of the lower 3 bits (i.e., the Function Number does not wrap past Function Number 7), repeat steps y-cc, still using the current [BDF].
- If [ARDEF] is 0 and ([VF BDF] = ([BDF] + First VF Offset + (([VFN]-1) * VF Stride)) mod 2 ** 16) produces a carry out of the lower 3 bits (i.e., the Function Number wraps past Function Number 7), increment the current [BDF] by increasing the Bus Number (upper 8 bits) by 1, and if the new [BDF] is less than or equal to the highest Bus Number/Device Number/Function Number supported on this system, then repeat steps y-cc, using this new [BDF].
- If [ARDEF] is 1 and ([VF BDF] = ([BDF] + First VF Offset + (([VFN]-1) * VF Stride)) mod 2 ** 16) does not produce a carry out of the lower 8 bits (i.e., the ARI Function Number does not wrap past Function Number 255), repeat steps y-cc, still using the current [BDF].
- If [ARDEF] is 1 and ([VF BDF] = ([BDF] + First VF Offset + (([VFN]-1) * VF Stride)) mod 2 ** 16) produces a carry out of the lower 8 bits (i.e., the ARI Function Number wraps past Function Number 255), increment the current [BDF] by increasing the Bus Number (upper 8 bits) by 1, and if the new [BDF] is less than or equal to the highest Bus Number/Device Number/Function Number supported on this system, then repeat steps y-cc, using this new [BDF].

dd. Increment [BDF] by 1, and if the new [BDF] is less than or equal to the highest Bus Number/Device Number/Function Number supported on this system, repeat steps a-dd).

In manual mode, the user selection prompt shall appear as a list of all the defined Device/Port Type values. Only if a function with a reserved encoding of Device/Port Type is found, an additional "Unknown" type value will also appear.

In manual mode, when the user selects one of these Device/Port Types, a new selection prompt will appear that lists each discovered function for that type, by giving its Bus Number/Device Number/Function Number address. (For a standard display format, the Device Number field can still be displayed for ARI functions, since any downstream device function that is not on Device Number 0, will be an ARI function.)

Functions, BFs, PFs, and VFs can all be listed using the same standard display format, as the user does not need to be able to distinguish between them, since the test will do so as needed by individual test cases.

When a specific function is selected, that function will be designated as the function under test.

1.5. Test Options for Data Rate

For functions under test that have a link, the test program shall test their link at the common link speed supported by the two sides of the link. This means that the test will run on an individual function under test at the Data Rate selected, as long as it is supported by the Base Specification Revision selection, and is supported by the link partners. In manual mode, the test program shall provide the user with a selection prompt to allow them to choose the Data Rate to run the test at. In automatic mode, the test program shall accept a parameter that identifies the Data Rate selection, providing that the specified parameter indicates a supported Data Rate. "Maximum supported speed only" is the selection used in automatic mode, when no parameter is specified. The requirements for each of these individual Data Rate selection options may change with each revision of this document, as may the number of Data Rate selection options. The Data Rate selection options and their requirements are stated below.

"Maximum supported speed only"

This selection will only run the individual tests at the maximum link speed supported by the Base Specification Revision selection and supported by the link partners.

"2.5 GT/s only"

This selection will only run the individual tests at 2.5 GT/s.

"5.0 GT/s only"

This selection will only run the individual tests at 5.0 GT/s, but only if it is supported by the Base Specification Revision selection and supported by the link partners.

"8.0 GT/s only"

This selection will only run the individual tests at 8.0 GT/s, but only if it is supported by the Base Specification Revision selection and supported by the link partners.

"16.0 GT/s only"

This selection will only run the individual tests at 16.0 GT/s, but only if it is supported by the Base Specification Revision selection and supported by the link partners.

"All supported speeds"

This selection will repeat the individual tests at all link speeds supported by the Base Specification Revision selection and supported by the link partners. It starts at 2.5 GT/s and ends at the maximum link speed supported.

1.6. Test Options for Achievable Link Width

For functions under test that have a link, the test program shall test their link at the largest Achievable Link Width supported by the two sides of the link. The Achievable Link Width can be altered, by the addition of link width reduction interposer cards between the link partners. For those tests that check for a specific link width, the test program needs to know what the Achievable Link Width is. In manual mode, the test program shall provide the user with a selection prompt to allow them to report the Achievable Link Width that the test should expect. In manual mode, the Achievable Link Width selection option is only presented, if the selected tests include a test that

requires this information. In automatic mode, the test program shall accept a parameter that identifies the Achievable Link Width selection. "Maximum supported width only" is the selection used in automatic mode, when no parameter is specified. The Achievable Link Width selection options and their requirements are stated below.

Note: There is no selection option for thirty-two lanes wide, as no current form-factor supports such a wide connector.

Maximum supported width only"

This selection will tell the test program to expect the negotiated link width to be the maximum link width supported by the link partners.

"x1"

This selection will tell the test program to expect the negotiated link width to be one lane wide.

"x2"

This selection will tell the test program to expect the negotiated link width to be two lanes wide.

"x4"

This selection will tell the test program to expect the negotiated link width to be four lanes wide.

"x8"

This selection will tell the test program to expect the negotiated link width to be eight lanes wide.

"x12"

This selection will tell the test program to expect the negotiated link width to be twelve lanes wide.

"x16"

This selection will tell the test program to expect the negotiated link width to be sixteen lanes wide.

2

2. Test Descriptions

This document describes only tests that can be run without special purpose test hardware.

2.1. Common Procedures and Routines

The Configuration Space Registers common tests cover mainly the registers defined in Chapter 6 of the *PCI Local Bus Specification* (Base 3.x or earlier only) and Chapters 7, 9 (Base 4.x or later only), 10 (Base 4.x or later only) of the *PCI Express Base Specification*. There is more than one state in which many of these tests can be run. Many of the tests are run with the function under test in more than one of these states. Each of the states and procedure used to put the function under test into this state are described here. This information is provided to help with debugging in cases where the function under test is not even reaching the desired starting state for the test. The individual tests mention which states they are run on, but do not repeat the setup procedure description.

2.1.1. Standard Initialization Procedure

Note: Test software blocks the operating system PCI/PCI Express stack from interacting with the function under test once the initialization sequence has started. This means that all the functions in the device containing the function under test, and all functions connected to the link hierarchy either started by the function under test, or for a downstream component, started by the upstream component connected to the function under test, must not have any active software driver. This can be accomplished, by either not installing the software driver, or by using the operating system's device-specific controls to disable the function (e.g., for a Windows operating system, using Device Manager to disable those functions). Additional steps must be taken to ensure that a primary boot device is not used as the function under test (e.g., the primary display device must not be used as the function under test, as it will cause the test's display output to disappear and the operating system to hang).

2.1.1.1 Reset Sequences

The test requires that the function under test, be put into its default state. This is achieved by executing an appropriate Reset Sequence that will cause the function under test to execute its internal hardware initialization, and put the hardware into a defined initial state. Different Reset Sequences are possible under PCI Express, each with small variations in the resulting hardware behaviour.

Each Reset Sequence is defined below, with any special effect on the hardware indicated. A summary of the Reset Sequences is shown in Table 2.1.

Note: For 2.x and earlier testing, Link Disable/Enable (DL_Down) is the only Reset Sequence used by test software.

For 3.x testing, Link Disable/Enable (DL_Down), Secondary Bus Reset (Hot Reset), and Function Level Reset (FLR) are the only Reset Sequences used by test software.

The Reset Sequences do not take advantage of the optional Readiness Notifications. Instead they will always wait the maximum allowed time for each sequence.

In manual mode, a user prompt is used to configure the test to select a specific Reset Sequence. In automatic mode, the test program shall accept a parameter that specifies the Reset Sequence to be used by the test. In manual mode, an additional selection ("Use device type dependent default reset mechanism") is provided to allow the test program to automatically select the default Reset Sequence based on the DUT's Device/Port Type. This is also the selection used in automatic mode, when no parameter is specified. The Reset Sequence selection options, their requirements, and default selections are stated below.

2.1.1.1.1 Link Disable/Enable (DL_Down) Reset Sequence

This is the default Reset Sequence for all functions under test that are connected to an upstream port (e.g., Legacy Endpoints, PCI Express Endpoints, Switch Upstream Ports, PCI Express to PCI/PCI-X Bridges) and all functions under test that are controlled by an upstream port component (e.g., Switch Downstream Ports).

1. If the function under test has a Type 1 Configuration Space Header, then the following registers are read and their values recorded for later restoration: Primary Bus Number; Secondary Bus Number; Subordinate Bus Number. The values must be recorded for all of the following: a) if the function under test is not a Root Port then the function itself; b) if the function under test is a Switch Downstream Port then the Switch Upstream Port that the Function under test is subordinate to; c) all Switch Ports and Bridges connected below the link hierarchy originating from the function under test; d) all functions behind the Function under test that also have a Type 1 Configuration Space Header. (Note: Resetting a Switch Downstream Port or PCI/PCI-X to PCI Express Bridge will cause it to transmit Hot Reset while resetting a PCI Express to PCI/PCI-X Bridge will cause it to assert bus reset, either of which will clear the bus number registers of all Switch Ports and Bridges below it. This will make the Switch Port and Bridge functions behind the Switch Port or Bridge disappear, so after the reset completes all these bus numbers must be restored before testing can continue.)
2. If the function under test does not connect to a link, then this is not a failure and the remaining steps are skipped. Note: For this device type, the test will report skipped for any sticky or default value portions of the test, when this type of Reset Sequence is used.
3. If the function under test is a Switch Downstream Port, the Link Disable field in the Link Control register on the next higher downstream port (the port connected to the link of the Switch Upstream Port that the function under test is immediately subordinate to) is set to 1 using a WORD access, while preserving all the other fields in this register.
4. If the function under test has a non-Switch downstream port, the Link Disable field in the Link Control register on the function under test is set to 1 using a WORD access, while preserving all the other fields in this register. Note: For this device type, the test will report skipped for any sticky or default value portions of the test, when this type of Reset Sequence is used.
5. If the function under test has an upstream port, the Link Disable field in the Link Control register on the immediate downstream port (the port connected to the link of the function under test) is set to 1 using a WORD access, while preserving all the other fields in this register.

6. After 50 ms the Link Disable field that was previously set in any one of steps 3-5 is cleared to 0 using a WORD access, while preserving all the other fields in this register.
7. Software starts a timer which will be called the Reset Timeout Timer [RTT]. The [RTT] is started with a value of 0. Note: The [RTT] must be capable of counting up to at least 1 second.
8. (Note: In the interest of saving time, this step may be skipped if the function under test does not support 8.0 GT/s or greater.) If the function under test has an upstream port, the immediate downstream port connected to the function under test is checked to see if it has completed training. If the function under test is a Switch Downstream Port, the immediate downstream port connected to the link of the Switch Upstream Port (that the function under test is immediately subordinate to) is checked to see if it has completed training. If the function under test has a non-Switch downstream port, the function under test is checked to see if it has completed training. Firstly, the Data Link Layer Link Active Reporting Capable field in the Link Capabilities register is read and if it returns 0, then go on to the next step. If the Data Link Layer Link Active Reporting Capable field returned 1, then continuously read the Data Link Layer Link Active field in the Link Status register, and when it returns 1, go on to the next step. If the Data Link Layer Link Active field does not return 1 before the [RTT] reaches 1 second, then report this as a link training failure, and skip the remaining steps.
9. Test software waits for 100 ms.
10. If the function under test is a Switch Downstream Port, then for the Switch Upstream Port (that the function under test is immediately subordinate to) test software restores all the values recorded in step 1 for: Primary Bus Number; Secondary Bus Number; Subordinate Bus Number.
11. (This step only applies to a function that is not an RCRB.) Read from the function under test, a WORD at location 00h (Vendor ID register) in Configuration Space and if it returns 0001h (CRS Software Visibility notification), then the read is repeated, until a different value is returned. If the different value is not returned before the [RTT] reaches 1 second, then report a function not detected failure, and skip the remaining steps.
12. (This step only applies to a function that is not a VF and not an RCRB.) Read from the function under test, a WORD at location 00h (Vendor ID register) in Configuration Space and if it returns FFFFh, then the read is repeated, until a different value is returned. If the different value is not returned before the [RTT] reaches 1 second, then report a function not detected failure, and skip the remaining steps.
13. If the function under test is a Switch Downstream Port, then steps 8-9 are repeated, by checking the downstream port of the function under test.
14. Stop the [RTT] timer.
15. Test software restores all the values recorded in step 1 for: Primary Bus Number; Secondary Bus Number; Subordinate Bus Number. These individual values must be restored in the Switch Port, all subordinate Switch Ports and Bridges, and in the Type 1 Configuration Space and any subordinate Type 1 Configuration Spaces.

2.1.1.1.2 Secondary Bus Reset (Hot Reset) Reset Sequence

This is the default Reset Sequence selected automatically, for all functions under test that are connected to a downstream port that are not controlled by an upstream port component (e.g., Root Ports, PCI/PCI-X to PCI Express Bridges).

1. If the function under test has a Type 1 Configuration Space Header, then the following registers are read and their values recorded for later restoration: Primary Bus Number; Secondary Bus Number; Subordinate Bus Number. The values must be recorded for all of the following: a) if the function under test is not a Root Port then the function itself; b) if the function under test is a Switch Downstream Port then the Switch Upstream Port that the Function under test is subordinate to; c) all Switch Ports and Bridges connected below the link hierarchy originating from the function under test; d) all functions behind the Function under test that also have a Type 1 Configuration Space Header. (Note: Resetting a Switch Downstream Port or PCI/PCI-X to PCI Express Bridge will cause it to transmit Hot Reset while resetting a PCI Express to PCI/PCI-X Bridge will cause it to assert bus reset, either of which will clear the bus number registers of all Switch Ports and Bridges below it. This will make the Switch Port and Bridge functions behind the Switch Port or Bridge disappear, so after the reset completes all these bus numbers must be restored before testing can continue.)
2. If the function under test does not connect to a link, then this is not a failure and the remaining steps are skipped. Note: For this device type, the test will report skipped for any sticky or default value portions of the test, when this type of Reset Sequence is used.
3. If the function under test has an upstream port, the Secondary Bus Reset field in the Bridge Control register on the immediate downstream port (the port connected to the link of the function under test) is set to 1 using a WORD access, while preserving all the other fields in this register.
4. If the function under test is a Switch Downstream Port, the Secondary Bus Reset field in the Bridge Control register on the next higher downstream port (the port connected to the link of the Switch Upstream Port that the function under test is immediately subordinate to) is set to 1 using a WORD access, while preserving all the other fields in this register.
5. If the function under test is a PCI/PCI-X to PCI Express Bridge, the Secondary Bus Reset field in the Bridge Control register on the next higher bus device (the device sourcing the bus that the function under test is on) is set to 1 using a WORD access, while preserving all the other fields in this register.
6. If the function under test is a Root Port, the Secondary Bus Reset field in the Bridge Control register on the function under test is set to 1 using a WORD access, while preserving all the other fields in this register. Note: For this device type, the test will report skipped for any sticky or default value portions of the test, when this type of Reset Sequence is used.
7. After 50 ms the Secondary Bus Reset field that was previously set in any one of steps 3-6 is cleared to 0 using a WORD access, while preserving all the other fields in this register.
8. Software starts a timer which will be called the Reset Timeout Timer [RTT]. The [RTT] is started with a value of 0. Note: The [RTT] must be capable of counting up to at least 1 second.
9. (Note: In the interest of saving time, this step may be skipped if the function under test does not support 8.0 GT/s or greater.) If the function under test has an upstream port, the immediate downstream port connected to the function under test is checked to see if it has

completed training. If the function under test is a Switch Downstream Port, the immediate downstream port connected to the link of the Switch Upstream Port (that the function under test is immediately subordinate to) is checked to see if it has completed training. If the function under test has a non-Switch downstream port, the function under test is checked to see if it has completed training. Firstly, the Data Link Layer Link Active Reporting Capable field in the Link Capabilities register is read and if it returns 0, then go on to the next step. If the Data Link Layer Link Active Reporting Capable field returned 1, then continuously read the Data Link Layer Link Active field in the Link Status register, and when it returns 1, go on to the next step. If the Data Link Layer Link Active field does not return 1 before the [RTT] reaches 1 second, then report this as a link training failure, and skip the remaining steps.

10. Test software waits for 100 ms.
11. If the function under test is a Switch Downstream Port, then for the Switch Upstream Port (that the function under test is immediately subordinate to) test software restores all the values recorded in step 1 for: Primary Bus Number; Secondary Bus Number; Subordinate Bus Number.
12. (This step only applies to a function that is not an RCRB.) Read from the function under test, a WORD at location 00h (Vendor ID register) in Configuration Space and if it returns 0001h (CRS Software Visibility notification), then the read is repeated, until a different value is returned. If the different value is not returned before the [RTT] reaches 1 second, then report a function not detected failure, and skip the remaining steps.
13. (This step only applies to a function that is not a VF and not an RCRB.) Read from the function under test, a WORD at location 00h (Vendor ID register) in Configuration Space and if it returns FFFFh, then the read is repeated, until a different value is returned. If the different value is not returned before the [RTT] reaches 1 second, then report a function not detected failure, and skip the remaining steps.
14. If the function under test is a Switch Downstream Port, then steps 9-10 are repeated, by checking the downstream port of the function under test.
15. Stop the [RTT] timer.
16. Test software restores all the values recorded in step 1 for: Primary Bus Number; Secondary Bus Number; Subordinate Bus Number. These individual values must be restored in the Switch Port, all subordinate Switch Ports and Bridges, and in the Type 1 Configuration Space and any subordinate Type 1 Configuration Spaces.

2.1.1.1.3 Function Level Reset (FLR) Reset Sequence

This is the default Reset Sequence selected automatically, for all functions under test that are Endpoints but are not connected to a link (e.g., Root Complex Integrated Endpoints, Root Complex Event Collectors). Since FLR does not affect the register fields that control the link of the device containing the function under test, it is not the primary choice for initializing functions under test that are connected to a link. When using FLR, test software must be aware of those register fields that are not reset (see Section 2.1.2.11). FLR is only supported on Endpoints. FLR is an optional feature and may not be implemented by the function under test.

1. If the function under test has a Type 1 Configuration Space Header, then the following registers are read and their values recorded for later restoration: Primary Bus Number; Secondary Bus Number; Subordinate Bus Number. The values must be recorded for all of the following: a) if

the function under test is not a Root Port then the function itself; b) if the function under test is a Switch Downstream Port then the Switch Upstream Port that the Function under test is subordinate to; c) all Switch Ports and Bridges connected below the link hierarchy originating from the function under test; d) all functions behind the Function under test that also have a Type 1 Configuration Space Header. (Note: Resetting a Switch Downstream Port or PCI/PCI-X to PCI Express Bridge will cause it to transmit Hot Reset while resetting a PCI Express to PCI/PCI-X Bridge will cause it to assert bus reset, either of which will clear the bus number registers of all Switch Ports and Bridges below it. This will make the Switch Port and Bridge functions behind the Switch Port or Bridge disappear, so after the reset completes all these bus numbers must be restored before testing can continue.)

2. If the function under test has its Function Level Reset Capability field in the Device Capabilities register return 0, then this is not a failure and the remaining steps are skipped. Note: The test will report skipped for any sticky or default value portions of the test.
3. If the function under test has its Function Level Reset Capability field in the Device Capabilities register return 1, the Initiate Function Level Reset field on the function under test is set to 1 using a WORD access, while preserving all the other fields in this register.
4. Software starts a timer which will be called the Reset Timeout Timer [RTT]. The [RTT] is started with a value of 0. Note: The [RTT] must be capable of counting up to at least 1 second.
5. Test software waits for 100 ms.
6. (This step only applies to a function that is not an RCRB.) Read from the function under test, a WORD at location 00h (Vendor ID register) in Configuration Space and if it returns 0001h (CRS Software Visibility notification), then the read is repeated, until a different value is returned. If the different value is not returned before the [RTT] reaches 1 second, then report a function not detected failure, and skip the remaining steps.
7. (This step only applies to a function that is not a VF and not an RCRB.) Read from the function under test, a WORD at location 00h (Vendor ID register) in Configuration Space and if it returns FFFFh, then the read is repeated, until a different value is returned. If the different value is not returned before the [RTT] reaches 1 second, then report a function not detected failure, and skip the remaining steps.
8. Stop the [RTT] timer.
9. Test software restores all the values recorded in step 1 for: Primary Bus Number; Secondary Bus Number; Subordinate Bus Number. These individual values must be restored in the Switch Port, all subordinate Switch Ports and Bridges, and in the Type 1 Configuration Space and any subordinate Type 1 Configuration Spaces.

Device Type	Port Direction (non-Crosslink)	Link Disable/Enable	Secondary Bus Reset	Function Level Reset
PCI Express Endpoints	Upstream Port	Supported + Default	Supported	Supported (if Function Level Reset Capability = 1) Supported as no-op (if Function Level Reset Capability = 0)
Legacy Endpoints	Upstream Port	Supported + Default	Supported	Supported (if Function Level Reset Capability = 1) Supported as no-op (if Function Level Reset Capability = 0)
Root Ports	Downstream Port	Supported	Supported + Default	Supported as no-op
Switch Upstream Ports	Upstream Port	Supported + Default	Supported	Supported as no-op
Switch Downstream Ports	Downstream Port	Supported + Default (applied at Switch Upstream Port)	Supported	Supported as no-op
PCI Express to PCI/PCI-X Bridges	Upstream Port	Supported + Default	Supported	Supported as no-op
PCI/PCI-X to PCI Express Bridges	Downstream Port	Supported	Supported + Default	Supported as no-op
Root Complex Integrated Endpoints	None	Supported as no-op	Supported as no-op	Supported + Default
Root Complex Event Collectors	None	Supported as no-op	Supported as no-op	Supported + Default

Table 2.1: Reset Type for Different Device Types

2.1.1.2 D0–Uninitialized State

1. The appropriate Reset Sequence (described in Section 2.1.1.1) is executed, to put the function under test into its initial state.
2. Test software waits for 100 ms.

3. (This step only applies to a function under test that connects to a PCI Express link and if Base 2.x or later testing is being done.) If necessary, the Target Link Speed field is set to the target speed for the test (one of: 2.5 GT/s; 5.0 GT/s; 8.0 GT/s; 16.0 GT/s), per the steps described in Sections 2.1.2.12 to 2.1.2.15. (The test initiates the link speed change from the immediate downstream port connected to the function under test, but only if that downstream port supports selecting that link speed using the Target Link Speed field.)

 Note that the packets (TLP/DLLP/Training Sets) from the downstream port may have any bits set that are newly defined in the latest *PCI Express Base Specification* but were reserved in previous revisions of the specification.

4. (This step only applies to a function under test that connects to a PCI Express link.) (In the interest of saving time, this step may be skipped if the function under test does not support 8.0 GT/s or greater.) The immediate downstream port connected to the function under test is checked to see if it has completed training. Firstly, the Data Link Layer Link Active Reporting Capable field in the Link Capabilities register is read and if it returns 0, then go on to the next step. If the Data Link Layer Link Active Reporting Capable field returned 1, then continuously read the Data Link Layer Link Active field in the Link Status register, and when it returns 1, go on to the next step. If the Data Link Layer Link Active field does not return 1 within 1 second, then report this as a link training failure, and skip the remaining steps.
5. Test software waits for 100 ms.
6. (This step only applies to a function that is not a VF and not an RCRB.) Read from the function under test, a WORD at location 00h (Vendor ID register) in Configuration Space and if it returns either 0001h (CRS Software Visibility notification) or FFFFh, then the read is repeated, until a different value is returned. If the different value is not returned within 1 second, then report a function not detected failure, and skip the remaining steps.
7. (This step only applies to a function under test that connects to a PCI Express link and is not an RCRB.) Autonomous speed and bandwidth changes are disabled for all test cases unless explicitly noted. This is done by setting Hardware Autonomous Width Disable field to 1 in the Link Control register (if supported) and the Hardware Autonomous Speed Disable field to 1 in the Link Control 2 register (if supported). This is done on both upstream and downstream ports of the function under test's link. If the function under test is part of a multi-function device, then for the function under test's upstream port, this is done in function 0 of the function under test's device. If the function under test is a VF, then this is programmed in its associated PF.
8. At this point, the DUT has reached the D0-Uninitialized State. If this is the desired test state, then go to section to set the ASPM Settings. Otherwise continue with the steps in the appropriate Dx State section.

2.1.1.3 D0-Initialized State

This state begins with the DUT already programmed according to all the steps in the D0-Uninitialized State section.

1. (This step only applies to a function that is not a VF and not an RCRB.) Function BAR registers (if present) are configured to valid regions available in the test system.
 Note: Bus Mastering, Interrupts, and PME are not enabled as part of the default configuration procedure.

2. (This step only applies to a function that is not a VF and not an RCRB.) Memory Space Enable and I/O Space Enable are set to 1 as appropriate, transitioning the function to D0-Initialized State.
3. At this point, the DUT has reached the D0-Initialized State. If this is the desired test state, then go to section to set the ASPM Settings. Otherwise continue with the steps in the Device State Settings section.

2.1.1.4 D1 State

This state begins with the DUT already programmed according to all the steps in the D0-Uninitialized State section.

1. For the function, read the D1 Support field (Power Management Capabilities register) and if it is 0, skip to step 4 (this is not a reported error).
2. For the function, the Power State field (Power Management Status and Control register) is set to 1.
3. For the function, the Power State field (Power Management Status and Control register) is polled repeatedly until it returns 1. If it does not return 1 within 1 second the polling stops (this is not a reported error).
4. Go to section to set the ASPM Settings.

2.1.1.5 D2 State

This state begins with the DUT already programmed according to all the steps in the D0-Uninitialized State section.

1. For the function, read the D2 Support field (Power Management Capabilities register) and if it is 0, skip to step 4 (this is not a reported error).
2. For the function, the Power State (Power Management Status and Control register) is set to 2.
3. For the function, the Power State (Power Management Status and Control register) is polled repeatedly until it returns 2. If it does not return 2 within 1 second the polling stops (this is not a reported error).
4. Go to section to set the ASPM Settings.

2.1.1.6 D3 (hot) State

This state begins with the DUT already programmed according to all the steps in the D0-Uninitialized State section.

1. For the function, the Power State (Power Management Status and Control register) is set to 3.
2. For the function, the Power State (Power Management Status and Control register) is polled repeatedly until it returns 3. If it does not return 3 within 1 second the polling stops (this is not a reported error).
3. Go to section to set the ASPM Settings.

2.1.1.7 Device State Settings

Device State: Some tests vary the starting power state of the device under test to be a non-D0 state. In those tests Device State is set at this stage in the initialization process. For a multi-function device under test, the setting is made in all functions of the device under test. Before these settings are made, the device under test is checked to ensure that the power state settings are supported by each function. If not supported by a function, the setting is skipped for that function only.

DUT: The Power State field (Power Management Control/Status register) is set as appropriate, for each supported function. Go to the section to set the ASPM Settings.

2.1.1.8 ASPM Settings

Active State Power Management (ASPM): Some tests vary the ASPM state of the upstream port of the device under test and the downstream port it is connected to. In those tests ASPM is set at this stage in the initialization process. For a multi-function device under test, the setting is made in all functions of the device under test. If the function under test is a VF, then this is programmed only in its associated PF. If the function under test is part of an internal link this is applied to both sides of the internal link. Before these settings are made, both the upstream port and the downstream port of the device under test's link are checked to ensure that the ASPM settings are supported. If not supported by either port, the setting is skipped.

Downstream Port: The Active State Power Management (ASPM) Control field (Link Control register for external links, Root Complex Link Control register for internal links) is set as appropriate.

Upstream Port: The Active State Power Management (ASPM) Control field (Link Control register for external links, Root Complex Link Control register for internal links) is set as appropriate.

2.1.2. Standard Register Field Characteristic Test Routines

The tests in this specification cover multiple PCI and PCI Express Configuration Space registers and Capability structures. A common part of many of these tests is to check register field characteristics of each field in the register or Capability structure under test. General procedures for testing all Configuration Space register field characteristics are given in this section. Individual test descriptions refer to this section.

The tests described below can be performed using accesses of different sizes. The smallest access that can be performed (read/write) is one byte (BYTE). Two byte (WORD) and four byte (DWORD) accesses can also be performed. The tests will use all accesses that can contain the full width of the field being tested. For example, if a 3 bit field is being tested, the test could use one, two, or four byte accesses in performing the test. If a 19 bit field is being tested, the test could use only four byte accesses in performing the test. The test can also use accesses that are not DWORD aligned as long as they do not cross a DWORD boundary and they contain the full width of the field being tested.

The following example is for illustrative purposes.

Bit 31 … Bit 24 Bit 23 … Bit 16 Bit 15 … Bit 8 Bit 7 … Bit 0

[Byte 3] [Byte 2] [Byte 1] [Byte 0]

[	Word 1	]	[	Word 0	]
[	DWord 0				]

X X X X X X X X

In this example, the field being tested is bits 15 to 8 (denoted by X), the test could use a four byte access aligned to byte 0 (denoted by DWord 0), a two byte access aligned to byte 0 (denoted by Byte 1 to Byte 0), a two byte access aligned to byte 1 (denoted by Byte 2 to Byte 1), or a one byte access aligned to byte 1 (denoted by Byte 1).

The following attribute options shall be supported by the test program: RO; RW; RW1C; ROS; RWS; RW1CS; RO-Zero; RO-Ones; HwInit. The specific test descriptions will mention which attribute options are used in testing each individual field.

Note: Some fields may be implemented as HwInit for Root Complex devices, and system-integrated devices. A test program that will execute on these devices before all system firmware has run on system startup must allow for these fields to be writable once (that is be HwInit).

2.1.2.1 Read Only (RO) Register Field Testing

1. The initial value is read from the field under test.
2. The inverse of the value read is written to the field under test. The field under test is inverted, while all other values are preserved if the register is a capabilities or a control register (RsvdP), or zeroed if the register is a status register (RsvdZ). No check is done to ensure that the write succeeds and no check is done to see if the request produced an error response from the function under test.
3. The field value is read. The value must be unchanged from the value read in step 1.
4. If the inverse value for the field under test used in step 2, was equivalent to a binary value of all 1's, then the remaining steps are skipped.
5. A binary value of all 1's is written to the field under test, while any other remaining field values are preserved if the register is a capabilities or a control register (RsvdP), or zeroed if the register is a status register (RsvdZ).
6. The field value is read. The value must be unchanged from the value read in step 1.

2.1.2.2 Read Write (RW) Register Field Testing

There are two types of RW register field testing. The first type of testing involves writing all valid values to each RW register field and verifying that the value written is read back. These cases are documented in individual test descriptions. The second type of testing involves writing illegal values to RW register fields and monitoring hardware behavior. These cases are documented in individual test descriptions. The following description describes the illegal value RW register procedure that is performed on all RW register fields.

1. The function is placed in the D0-Uninitialized state. (BARs are not configured.)

 Note: This test only applies with the function is in the D0-Uninitialized state and its BAR registers have not been configured.

2. Any test-specific register field is restored to its described value in the test description (e.g., if the field under test is part of an indexed register, then the index is restored first before accessing the field under test).
3. The initial value is read from the field under test.
4. Any illegal value is written to the field under test, while any other remaining field values are preserved if the register is a capabilities or a control register (RsvdP), or zeroed if the register is a status register (RsvdZ).

 Note: The test does not check that the illegal value is latched by the field under test. This is not a requirement.
5. Steps 3-4 are repeated for each illegal value specified.
6. The original value read in the initial step 3 is written to the device.
7. The function is configured to the D0-Initialized state following the procedure in Section 2.1.1.3. The configuration process must still work correctly.

2.1.2.3 Read Write 1 Clear (RW1C) Register Field Testing

1. The initial value is read from the field under test.
2. Test software writes all 0's to the field under test, while any other remaining field values are preserved if the register is a capabilities or a control register (RsvdP), or zeroed if the register is a status register (RsvdZ).
3. Test software reads the field under test. The value read must be unchanged from the value read in step 1.
4. Test software writes all 1's to the field under test while any other remaining field values are preserved if the register is a capabilities or a control register (RsvdP), or zeroed if the register is a status register (RsvdZ).
5. Test software reads the field under test. The value read must be all 0's.

2.1.2.4 Read Only Sticky (ROS) Register Field Testing

The tests in Section 2.1.2.1 for a RO register field are repeated. The following additional tests are then performed:

1. The value is read from the field under test.
2. The appropriate Reset Sequence (described in Section 2.1.1.1) is executed, to put the function under test into its initial state.
3. Any test-specific register field is restored to its described value in the test description (e.g., if the field under test is part of an indexed register, then the index is restored first before accessing the field under test).
4. The field under test is read. The value must be unchanged from the value read in step 1.

Note: Special cases where values need to be maintained/cleared through the Reset Sequence are called out specifically in individual test descriptions later in this specification.

2.1.2.5 Read Write Sticky (RWS) Register Field Testing

The RW tests for a register field described in Section 2.1.2.2 are performed normally. The following additional testing is performed to verify the sticky nature of the register:

1. The value is read from the field under test.
2. Any legal value is written to the field under test, while any other remaining field values are preserved if the register is a capabilities or a control register (RsvdP), or zeroed if the register is a status register (RsvdZ).
3. The field under test is read. The value read must match the value written in step 2.
4. The appropriate Reset Sequence (described in Section 2.1.1.1) is executed, to put the function under test into its initial state.
5. Any test-specific register field is restored to its described value in the test description (e.g., if the field under test is part of an indexed register, then the index is restored first before accessing the field under test).
6. The field under test is read. The value must match the value read in step 3.

Note: Special cases where values need to be maintained/cleared through the Reset Sequence are called out specifically in individual test descriptions later in this specification.

2.1.2.6 Read Write 1 Clear Sticky (RW1CS) Register Field Testing

The following steps are performed in addition to the testing in Section 2.1.2.3 for a RW1C register:

1. The value is read from the field under test.
2. The appropriate Reset Sequence (described in Section 2.1.1.1) is executed, to put the function under test into its initial state.
3. Any test-specific register field is restored to its described value in the test description (e.g., if the field under test is part of an indexed register, then the index is restored first before accessing the field under test).
4. The field under test is read. It must match the value read in step 1.

Note: Special cases where values need to be maintained/cleared through the Reset Sequence are called out specifically in individual test descriptions later in this specification.

2.1.2.7 Hardware Initialized (HwInit) Register Field Testing

1. The value is read from the field under test.
2. The inverse of the value read and if necessary converted to a legal value and then is written to the field under test. The field under test is inverted while all other values are preserved if the register is a capabilities or a control register (RsvdP), or zeroed if the register is a status register (RsvdZ). No check is done to ensure that the write succeeds and no check is done to see if the request produced an error response from the function under test.
3. The value of the field under test is read. If the value is unchanged from the value read in step 1, continue to the next step. If the value is changed then steps 1-3 are repeated just once more. The value is only allowed to change once, if it changes again, then the test fails.

4. If the inverse value for the field under test used in step 2, was equivalent to a binary value of all 1's, then the remaining steps are skipped.
5. A binary value of all 1's is written to the field under test, while any other remaining field values are preserved if the register is a capabilities or a control register (RsvdP), or zeroed if the register is a status register (RsvdZ).
6. The field under test is read. The value must be unchanged from the value read in step 3. If the value has changed the test fails.

2.1.2.8 RO-Zero Register Field Testing

RO-Zero register fields are tested with the same requirements as Read Only (RO) register fields except that every read must return all bits in the field under test as 0. The software requirement to preserve the existing bits in an RsvdP field is ignored by test software. The software requirement to only write 0's to an RsvdZ field is ignored by the test program.

2.1.2.9 RO-Ones Register Field Testing

RO-Ones register fields are tested with the same requirements as Read Only register fields except that every read must return all bits in the field under test as 1.

2.1.2.10 Default Value Register Field Testing

Default value register field testing can only be executed on those device types that support a Reset Sequence that can be used to return the function under test to its default state. Devices with only a downstream (e.g., a Root Port or a PCI/PCI-X to PCI Express Bridge), cannot be reset by any of the Reset Sequences defined in this test document. Therefore, any function under test that is a Root Port or a PCI/PCI-X to PCI Express Bridge will skip the default value register field part of the test descriptions. Root Complex internal components (e.g., a Root Complex Integrated Endpoint, a Root Complex Event Collector, or an RCRB), similarly cannot be reset by any of the Reset Sequences defined in this test document, except in the case that they support Function Level Reset. Therefore, any function under test that is a Root Complex Integrated Endpoint without FLR support, a Root Complex Event Collector, or an RCRB will skip the default value register field part of the test descriptions.

Base Specification rules for default value register fields do not apply to Root Complexes and system-integrated devices. As such these devices may return any default value. Test software has no way to determine if the function under test is a system-integrated device, so it treats all functions under test as if they were not system-integrated devices. For system-integrated devices other than those listed in the preceding two paragraphs, the test results for default value register field testing, may require the user to manually review the results in order to determine if the default value register field failure is valid.

The register attribute tables indicate those register fields that behave differently for FLR versus non-FLR Reset Sequences. When using a non-FLR Reset Sequence any listed non-FLR testing attribute should be used.

1. If the field under test is RW1C or RW1CS, the default value listed in the test description is written to the field under test, while any other remaining field values are preserved if the register is a capabilities or a control register (RsvdP), or zeroed if the register is a status register (RsvdZ).

If the field under test is not RW1C and not RW1CS, the inverse of the default value listed in the test description is written to the field under test, while any other remaining field values are preserved if the register is a capabilities or a control register (RsvdP), or zeroed if the register is a status register (RsvdZ). No check is done to ensure that the write succeeds and no check is done to see if the request produced an error response from the function under test. (Note: Since a RW1C or RW1CS field is cleared by writing a 1, and it is not changed by writing a 0, it behaves in an inverse way to a RW or RWS field. Therefore, to test the default value for a RW1C or RW1CS field, the value written must be one that tries to have the field contain the opposite value specified as its default value. Examples: If the field is RW1C defaulting to 0 and it currently has a 1 in it, then to test for default value, write it with a 0, so it retains the 1, and then initiate the Reset Sequence to cause the field to reset to 0. If the field is RW1C defaulting to 1 and it currently has a 1 in it, then to test for default value, write it with a 1, so it clears to 0, and then initiate the Reset Sequence to cause the field to reset to 1.)

2. The value in the field under test is read.
3. The appropriate Reset Sequence (described in Section 2.1.1.1) is executed, to put the function under test into its initial state.
4. Any test-specific register field is restored to its described value in the test description (e.g., if the field under test is part of an indexed register, then the index is restored first before accessing the field under test).
5. The value in the field under test is read.
 a. For a sticky field, it must match the value read in step 2.
 b. For a non-sticky field, it must match the default value listed in the test description for that field.

2.1.2.11 Function Level Reset Testing

For a function or PF that supports Function Level Reset (as determined by checking the Function Level Reset Capability field in the Device Capabilities register) all register fields default value tests that did not use a FLR Reset Sequence may be repeated using a FLR Reset Sequence (described in Section 2.1.1.1.3).

The register attribute tables indicate those register fields that behave differently for FLR versus non-FLR Reset Sequences. When using the FLR Reset Sequence any listed FLR testing attribute should be used.

2.1.2.12 2.5 GT/s Support Detection and Testing

The following applies to Base 1.x or later testing. All links are assumed to support 2.5 GT/s and only this link speed will be tested. No specific algorithm is needed to detect the supported link speed, and no attempt is made to change the current link speed. The test assumes that the hardware will automatically train the link to 2.5 GT/s, if that is the only supported link speed, whenever the link is enabled or reset.

The following only applies to Base 2.x or later testing.

For a function under test that supports greater than 2.5 GT/s, test software will need to limit the link speed to 2.5 GT/s using the Target Link Speed field in the Link Control 2 register, in order to test at this speed.

In order to configure the function under test's external PCI Express link to 2.5 GT/s the following steps are done if the function under test contains an upstream port (e.g., Endpoint, Switch Upstream Port, PCI Express to PCI/PCI-X Bridge):

1. Read the function under test's Link Capabilities register bits 3-0 value and if it returns 0000b (no link supported) or 0001b (only 2.5 GT/s supported), then no further attempt is made to change the link speed to 2.5 GT/s.
2. Read the immediate downstream port's (the port connected to the function under test) Link Capabilities register bits 3-0 value and if it returns 0000b (no link supported) or 0001b (only 2.5 GT/s supported), then no further attempt is made to change the link speed to 2.5 GT/s.
3. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is set to 0001b (2.5 GT/s) on function 0 of the device containing the function under test. For this write the following fields are also set as follows:
 a. Enter Compliance (bit 4) is set to 0
 b. Hardware Autonomous Speed Disable (bit 5) is set to 1
 c. Transmit Margin (bits 9-7) is set to 000b
 d. Enter Modified Compliance (bit 10) is set to 0
 e. Compliance SOS (bit 11) is set to 0
 f. Compliance Preset/De-emphasis (bits 15-12) is set to 0000b.
4. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is read back and if it does not return 0001b (2.5 GT/s) or 0000b (reserved) on function 0 of the device containing the function under test then no further attempt is made to change the link speed to 2.5 GT/s. This is reported as a test failure.
5. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is set to 0001b (2.5 GT/s) on the immediate downstream port (the port connected to the function under test). This port will be referred to as the downstream port of the link. For this write the following fields are also set as follows:
 a. Enter Compliance (bit 4) is set to 0
 b. Hardware Autonomous Speed Disable (bit 5) is set to 1
 c. Transmit Margin (bits 9-7) is set to 000b
 d. Enter Modified Compliance (bit 10) is set to 0
 e. Compliance SOS (bit 11) is set to 0
 f. Compliance Preset/De-emphasis (bits 15-12) is set to 0000b.
6. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is read back and if it does not return 0001b (2.5 GT/s) or 0000b (reserved) on the downstream port of the link, then no further attempt is made to change the link speed to 2.5 GT/s (this is not a failure, but the test result for 2.5 GT/s is reported as skipped).
7. Read the downstream port's Link Capabilities register bits 3-0 value and if it returns 0011b (8.0 GT/s supported) or greater, then:
 a. The Perform Equalization field (Link Control 3 register) is set to 0 on the downstream port of the link.

8. Test software reads the Link Training field (Link Status register) on the downstream port of the link until it reads 0. If the Link Training field does not return 0 within 1 second, then report this as a link training failure, and skip the remaining steps. (Note: This step is needed to ensure that the next retrain will use the settings programmed by the preceding steps.)
9. Test software writes 1 to the Retrain Link field (Link Control register) on the downstream port of the link using a WORD access, while preserving all the other fields in this register.
10. Test software reads the Link Training field (Link Status register) on the downstream port of the link until it reads 0. If the Link Training field does not return 0 within 1 second, then report this as a link training failure, and skip the remaining steps.
11. Test software reads the Current Link Speed field (Link Status register) in the downstream port of the link. The value must return 0001b (2.5 GT/s). If it does not, then the attempt fails and is reported as a link speed failure.

In order to configure the function under test's external PCI Express link to 2.5 GT/s the following steps are done if the function under test contains a downstream port (e.g., Root Port, Switch Downstream Port, PCI/PCI-X to PCI Express Bridge):

1. Read the function under test's Link Capabilities register bits 3-0 value and if it returns 0000b (no link supported) or 0001b (only 2.5 GT/s supported), then no further attempt is made to change the link speed to 2.5 GT/s.
2. Read the immediate upstream port's (connected to the function under test) Link Capabilities register bits 3-0 value and if it returns 0000b (no link supported) or 0001b (only 2.5 GT/s supported), then no further attempt is made to change the link speed to 2.5 GT/s.
3. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is set to 0001b (2.5 GT/s) on function 0 of the immediate upstream port (connected to the function under test). For this write the following fields are also set as follows:
 a. Enter Compliance (bit 4) is set to 0
 b. Hardware Autonomous Speed Disable (bit 5) is set to 1
 c. Transmit Margin (bits 9-7) is set to 000b
 d. Enter Modified Compliance (bit 10) is set to 0
 e. Compliance SOS (bit 11) is set to 0
 f. Compliance Preset/De-emphasis (bits 15-12) is set to 0000b.
4. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is read back and if it does not return 0001b (2.5 GT/s) or 0000b (reserved) on function 0 of the immediate upstream port (connected to the function under test) then no further attempt is made to change the link speed to 2.5 GT/s (this is not a failure, but the test result for 2.5 GT/s is reported as skipped).

5. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is set to 0001b (2.5 GT/s) on the function under test. For this write the following fields are also set as follows:
 a. Enter Compliance (bit 4) is set to 0
 b. Hardware Autonomous Speed Disable (bit 5) is set to 1
 c. Transmit Margin (bits 9-7) is set to 000b
 d. Enter Modified Compliance (bit 10) is set to 0

e. Compliance SOS (bit 11) is set to 0
f. Compliance Preset/De-emphasis (bits 15-12) is set to 0000b.

6. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is read back and if it does not return 0001b (2.5 GT/s) or 0000b (reserved) on the function under test then no further attempt is made to change the link speed to 2.5 GT/s. This is reported as a test failure.
7. Read the function under test's Link Capabilities register bits 3-0 value and if it returns 0011b (8.0 GT/s supported) or greater, then:
 a. The Perform Equalization field (Link Control 3 register) is set to 0 on the function under test.
8. Test software reads the Link Training field (Link Status register) on the function under test until it reads 0. If the Link Training field does not return 0 within 1 second, then report this as a link training failure, and skip the remaining steps. (Note: This step is needed to ensure that the next retrain will use the settings programmed by the preceding steps.)
9. Test software writes 1 to the Retrain Link field (Link Control register) on the function under test using a WORD access, while preserving all the other fields in this register.
10. Test software reads the Link Training field (Link Status register) on the function under test until it reads 0. If the Link Training field does not return 0 within 1 second, then report this as a link training failure, and skip the remaining steps.
11. Test software reads the Current Link Speed field (Link Status register) in the function under test and it must return 0001b (2.5 GT/s). If it does not, then the attempt fails and is reported as a link speed failure.

Test software cannot control the link speed of Root Complex internal device links (e.g., Root Complex Integrated Endpoints or Root Complex Event Collectors). When a function under test is of this device type, no attempt is made to control the link speed and the test is run only once at whatever link speed the internal link runs at. In addition, some Root Ports may connect to internal links (rather than external links). Test software will only try to change the link speed on such a Root Port's external link (if it has one). It is not currently possible to configure the speed of Root Complex internal links, so there is currently no support in test software to do so.

2.1.2.13 5.0 GT/s Support Detection and Testing

The following only applies to Base 2.x or later testing. The test assumes that all links support at least 2.5 GT/s.

For a function under test that supports 5.0 GT/s, test software will attempt to test it once at 2.5 GT/s (which all PCI Express devices with external links must support), and again at 5.0 GT/s (which is an optional feature starting with Base 2.0).

For a function under test that supports greater than 5.0 GT/s, test software will need to limit the link speed to 5.0 GT/s using the Target Link Speed field in the Link Control 2 register, in order to test at this speed.

In order to configure the function under test's external PCI Express link to 5.0 GT/s the following steps are done if the function under test contains an upstream port (e.g., Endpoint, Switch Upstream Port, or PCI Express to PCI/PCI-X Bridge):

1. Read the function under test's Link Capabilities register bits 3-0 value and if it returns 0000b (no link supported) or 0001b (only 2.5 GT/s supported), then no further attempt is made to change the link speed to 5.0 GT/s.
2. Read the immediate downstream port's (the port connected to the function under test) Link Capabilities register bits 3-0 value and if it returns 0000b (no link supported) or 0001b (only 2.5 GT/s supported), then no further attempt is made to change the link speed to 5.0 GT/s.
3. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is set to 0010b (5.0 GT/s) on function 0 of the device containing the function under test. For this write the following fields are also set as follows:
 a. Enter Compliance (bit 4) is set to 0
 b. Hardware Autonomous Speed Disable (bit 5) is set to 1
 c. Transmit Margin (bits 9-7) is set to 000b
 d. Enter Modified Compliance (bit 10) is set to 0
 e. Compliance SOS (bit 11) is set to 0
 f. Compliance Preset/De-emphasis (bits 15-12) is set to 0000b.
4. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is read back and if it does not return 0010b (5.0 GT/s) on function 0 of the device containing the function under test then no further attempt is made to change the link speed to 5.0 GT/s. This is reported as a test failure.
5. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is set to 0010b (5.0 GT/s) on the immediate downstream port (the port connected to the function under test). This port will be referred to as the downstream port of the link. For this write the following fields are also set as follows:
 a. Enter Compliance (bit 4) is set to 0
 b. Hardware Autonomous Speed Disable (bit 5) is set to 1
 c. Transmit Margin (bits 9-7) is set to 000b
 d. Enter Modified Compliance (bit 10) is set to 0
 e. Compliance SOS (bit 11) is set to 0
 f. Compliance Preset/De-emphasis (bits 15-12) is set to 0000b.
6. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is read back and if it does not return 0010b (5.0 GT/s) on the downstream port of the link, then no further attempt is made to change the link speed to 5.0 GT/s (this is not a failure, but the test result for 5.0 GT/s is reported as skipped).
7. Read the downstream port's Link Capabilities register bits 3-0 value and if it returns 0011b (8.0 GT/s supported) or greater, then:
 a. The Perform Equalization field (Link Control 3 register) is set to 0 on the downstream port of the link.
8. Test software reads the Link Training field (Link Status register) on the downstream port of the link until it reads 0. If the Link Training field does not return 0 within 1 second, then report this as a link training failure, and skip the remaining steps. (Note: This step is needed to ensure that the next retrain will use the settings programmed by the preceding steps.)
9. Test software writes 1 to the Retrain Link field (Link Control register) on the downstream port of the link using a WORD access, while preserving all the other fields in this register.

10. Test software reads the Link Training field (Link Status register) on the downstream port of the link until it reads 0. If the Link Training field does not return 0 within 1 second, then report this as a link training failure, and skip the remaining steps.
11. Test software reads the Current Link Speed field (Link Status register) in the downstream port of the link. If the value returns 0010b (5.0 GT/s), then skip the remaining steps.
12. Test software writes 1 to the Retrain Link field (Link Control register) on the downstream port of the link using a WORD access, while preserving all the other fields in this register.
13. Test software reads the Link Training field (Link Status register) on the downstream port of the link until it reads 0. If the Link Training field does not return 0 within 1 second, then report this as a link training failure, and skip the remaining steps.
14. Test software reads the Current Link Speed field (Link Status register) in the downstream port of the link. The value must return 0010b (5.0 GT/s). If it does not, then the attempt fails and is reported as a link speed failure.

In order to configure the function under test's external PCI Express link to 5.0 GT/s the following steps are done if the function under test contains a downstream port (e.g., Root Port, Switch Downstream Port, or PCI/PCI-X to PCI Express Bridge):

1. Read the function under test's Link Capabilities register bits 3-0 value and if it returns 0000b (no link supported) or 0001b (only 2.5 GT/s supported), then no further attempt is made to change the link speed to 5.0 GT/s.
2. Read the immediate upstream port's (connected to the function under test) Link Capabilities register bits 3-0 value and if it returns 0000b (no link supported) or 0001b (only 2.5 GT/s supported), then no further attempt is made to change the link speed to 5.0 GT/s.
3. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is set to 0010b (5.0 GT/s) on function 0 of the immediate upstream port (connected to the function under test). For this write the following fields are also set as follows:
 a. Enter Compliance (bit 4) is set to 0
 b. Hardware Autonomous Speed Disable (bit 5) is set to 1
 c. Transmit Margin (bits 9-7) is set to 000b
 d. Enter Modified Compliance (bit 10) is set to 0
 e. Compliance SOS (bit 11) is set to 0
 f. Compliance Preset/De-emphasis (bits 15-12) is set to 0000b.
4. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is read back and if it does not return 0010b (5.0 GT/s) on function 0 of the immediate upstream port (connected to the function under test) then no further attempt is made to change the link speed to 5.0 GT/s (this is not a failure, but the test result for 5.0 GT/s is reported as skipped).
5. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is set to 0010b (5.0 GT/s) on the function under test. For this write the following fields are also set as follows:
 a. Enter Compliance (bit 4) is set to 0
 b. Hardware Autonomous Speed Disable (bit 5) is set to 1
 c. Transmit Margin (bits 9-7) is set to 000b

 d. Enter Modified Compliance (bit 10) is set to 0
 e. Compliance SOS (bit 11) is set to 0
 f. Compliance Preset/De-emphasis (bits 15-12) is set to 0000b.

6. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is read back and if it does not return 0010b (5.0 GT/s) on the function under test then no further attempt is made to change the link speed to 5.0 GT/s. This is reported as a test failure.
7. Read the function under test's Link Capabilities register bits 3-0 value and if it returns 0011b (8.0 GT/s supported) or greater, then:
 a. The Perform Equalization field (Link Control 3 register) is set to 0 on the function under test.
8. Test software reads the Link Training field (Link Status register) on the function under test until it reads 0. If the Link Training field does not return 0 within 1 second, then report this as a link training failure, and skip the remaining steps. (Note: This step is needed to ensure that the next retrain will use the settings programmed by the preceding steps.)
9. Test software writes 1 to the Retrain Link field (Link Control register) on the function under test using a WORD access, while preserving all the other fields in this register.
10. Test software reads the Link Training field (Link Status register) on the function under test until it reads 0. If the Link Training field does not return 0 within 1 second, then report this as a link training failure, and skip the remaining steps.
11. Test software reads the Current Link Speed field (Link Status register) in the function under test and if it returns 0010b (5.0 GT/s), then skip the remaining steps.
12. Test software writes 1 to the Retrain Link field (Link Control register) on the downstream port of the link using a WORD access, while preserving all the other fields in this register.
13. Test software reads the Link Training field (Link Status register) on the downstream port of the link until it reads 0. If the Link Training field does not return 0 within 1 second, then report this as a link training failure, and skip the remaining steps.
14. Test software reads the Current Link Speed field (Link Status register) in the function under test and it must return 0010b (5.0 GT/s). If it does not, then the attempt fails and is reported as a link speed failure.

Test software cannot control the link speed of Root Complex internal device links (e.g., Root Complex Integrated Endpoints or Root Complex Event Collectors). When a function under test is of this device type, no attempt is made to control the link speed and the test is run only once at whatever link speed the internal link runs at. In addition, some Root Ports may connect to internal links (rather than external links). Test software will only try to change the link speed on such a Root Port's external link (if it has one). It is not currently possible to configure the speed of Root Complex internal links, so there is currently no support in test software to do so.

2.1.2.14 8.0 GT/s Support Detection and Testing

The following only applies to Base 3.x or later testing. The test assumes that all links support at least 2.5 GT/s.

For a function under test that supports 8.0 GT/s, test software will attempt to test it once at 2.5 GT/s (which all PCI Express devices with external links, must support), again at 5.0 GT/s (which is an optional feature starting with Base 2.0), and again at 8.0 GT/s (which is an optional feature starting with Base 3.0).

For a function under test that supports greater than 8.0 GT/s, test software will need to limit the link speed to 8.0 GT/s using the Target Link Speed field in the Link Control 2 register, in order to test at this speed.

In order to configure the function under test's external PCI Express link to 8.0 GT/s the following steps are done if the function under test contains an upstream port (e.g., Endpoint, Switch Upstream Port, or PCI Express to PCI/PCI-X Bridge):

1. Read the function under test's Link Capabilities register bits 3-0 value and if it returns 0000b (no link supported), or 0001b (only 2.5 GT/s supported), or 0010b (only 2.5 GT/s and 5.0 GT/s supported), then no further attempt is made to change the link speed to 8.0 GT/s.
2. Read the immediate downstream port's (the port connected to the function under test) Link Capabilities register bits 3-0 value and if it returns 0000b (no link supported), or 0001b (only 2.5 GT/s supported), or 0010b (only 2.5 GT/s and 5.0 GT/s supported), then no further attempt is made to change the link speed to 8.0 GT/s.
3. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is set to 0011b (8.0 GT/s) on function 0 of the device containing the function under test. For this write the following fields are also set as follows:
 a. Enter Compliance (bit 4) is set to 0
 b. Hardware Autonomous Speed Disable (bit 5) is set to 1
 c. Transmit Margin (bits 9-7) is set to 000b
 d. Enter Modified Compliance (bit 10) is set to 0
 e. Compliance SOS (bit 11) is set to 0
 f. Compliance Preset/De-emphasis (bits 15-12) is set to 0000b.
4. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is read back and if it does not return 0011b (8.0 GT/s) on function 0 of the device containing the function under test then no further attempt is made to change the link speed to 8.0 GT/s. This is reported as a test failure.
5. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is set to 0011b (8.0 GT/s) on the immediate downstream port (the port connected to the function under test). This port will be referred to as the downstream port of the link. For this write the following fields are also set as follows:
 a. Enter Compliance (bit 4) is set to 0
 b. Hardware Autonomous Speed Disable (bit 5) is set to 1
 c. Transmit Margin (bits 9-7) is set to 000b
 d. Enter Modified Compliance (bit 10) is set to 0
 e. Compliance SOS (bit 11) is set to 0
 f. Compliance Preset/De-emphasis (bits 15-12) is set to 0000b.
6. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is read back and if it does not return 0011b (8.0 GT/s) on the downstream port of the link, then no further attempt is made to change the link speed to 8.0 GT/s (this is not a failure, but the test result for 8.0 GT/s is reported as skipped).

7. The Perform Equalization field (Link Control 3 register) is set to 0 on the downstream port of the link.
8. Test software reads the Link Training field (Link Status register) on the downstream port of the link until it reads 0. If the Link Training field does not return 0 within 1 second, then report this as a link training failure, and skip the remaining steps. (Note: This step is needed to ensure that the next retrain will use the settings programmed by the preceding steps.)
9. Test software writes 1 to the Retrain Link field (Link Control register) on the downstream port of the link using a WORD access, while preserving all the other fields in this register.
10. Test software reads the Link Training field (Link Status register) on the downstream port of the link until it reads 0. If the Link Training field does not return 0 within 1 second, then report this as a link training failure, and skip the remaining steps.
11. Test software reads the Current Link Speed field (Link Status register) in the downstream port of the link. If the value returns 0011b (8.0 GT/s), then skip the remaining steps.
12. Test software writes 1 to the Retrain Link field (Link Control register) on the downstream port of the link using a WORD access, while preserving all the other fields in this register.
13. Test software reads the Link Training field (Link Status register) on the downstream port of the link until it reads 0. If the Link Training field does not return 0 within 1 second, then report this as a link training failure, and skip the remaining steps.
14. Test software reads the Current Link Speed field (Link Status register) in the downstream port of the link. The value must return 0011b (8.0 GT/s). If it does not, then the attempt fails and is reported as a link speed failure.

In order to configure the function under test's external PCI Express link to 8.0 GT/s the following steps are done if the function under test contains a downstream port (e.g., Root Port, Switch Downstream Port, or PCI/PCI-X to PCI Express Bridge):

1. Read the function under test's Link Capabilities register bits 3-0 value and if it returns 0000b (no link supported), or 0001b (only 2.5 GT/s supported), or 0010b (only 2.5 GT/s and 5.0 GT/s supported), then no further attempt is made to change the link speed to 8.0 GT/s.
2. Read the immediate upstream port's (connected to the function under test) Link Capabilities register bits 3-0 value and if it returns 0000b (no link supported), or 0001b (only 2.5 GT/s supported), or 0010b (only 2.5 GT/s and 5.0 GT/s supported), then no further attempt is made to change the link speed to 8.0 GT/s.
3. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is set to 0011b (8.0 GT/s) on function 0 of the immediate upstream port (connected to the function under test). For this write the following fields are also set as follows:
 a. Enter Compliance (bit 4) is set to 0
 b. Hardware Autonomous Speed Disable (bit 5) is set to 1
 c. Transmit Margin (bits 9-7) is set to 000b
 d. Enter Modified Compliance (bit 10) is set to 0
 e. Compliance SOS (bit 11) is set to 0
 f. Compliance Preset/De-emphasis (bits 15-12) is set to 0000b.

4. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is read back and if it does not return 0011b (8.0 GT/s) on function 0 of the immediate upstream port (connected to the function under test) then no further attempt is made to change the link speed to 8.0 GT/s (this is not a failure, but the test result for 8.0 GT/s is reported as skipped).
5. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is set to 0011b (8.0 GT/s) on the function under test. For this write the following fields are also set as follows:
 a. Enter Compliance (bit 4) is set to 0
 b. Hardware Autonomous Speed Disable (bit 5) is set to 1
 c. Transmit Margin (bits 9-7) is set to 000b
 d. Enter Modified Compliance (bit 10) is set to 0
 e. Compliance SOS (bit 11) is set to 0
 f. Compliance Preset/De-emphasis (bits 15-12) is set to 0000b.
6. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is read back and if it does not return 0011b (8.0 GT/s) on the function under test then no further attempt is made to change the link speed to 8.0 GT/s. This is reported as a test failure.
7. The Perform Equalization field (Link Control 3 register) is set to 0 on the function under test.
8. Test software reads the Link Training field (Link Status register) on the function under test until it reads 0. If the Link Training field does not return 0 within 1 second, then report this as a link training failure, and skip the remaining steps. (Note: This step is needed to ensure that the next retrain will use the settings programmed by the preceding steps.)
9. Test software writes 1 to the Retrain Link field (Link Control register) on the function under test using a WORD access, while preserving all the other fields in this register.
10. Test software reads the Link Training field (Link Status register) on the function under test until it reads 0. If the Link Training field does not return 0 within 1 second, then report this as a link training failure, and skip the remaining steps.
11. Test software reads the Current Link Speed field (Link Status register) in the function under test and if it returns 0011b (8.0 GT/s), then skip the remaining steps.
12. Test software writes 1 to the Retrain Link field (Link Control register) on the function under test using a WORD access, while preserving all the other fields in this register.
13. Test software reads the Link Training field (Link Status register) on the function under test until it reads 0. If the Link Training field does not return 0 within 1 second, then report this as a link training failure, and skip the remaining steps.
14. Test software reads the Current Link Speed field (Link Status register) in the function under test and it must return 0011b (8.0 GT/s). If it does not, then the attempt fails and is reported as a link speed failure.

Note: For the purposes of setting the link speed, test software assumes that for 8.0 GT/s, Link Equalization has already been performed (following reset of the function under test).

Test software cannot control the link speed of Root Complex internal device links (e.g., Root Complex Integrated Endpoints or Root Complex Event Collectors). When a function under test is

of this device type, no attempt is made to control the link speed and the test is run only once at whatever link speed the internal link runs at. In addition, some Root Ports may connect to internal links (rather than external links). Test software must only try to change the link speed on such a Root Port's external link (if it has one). It is not currently possible to configure the speed of Root Complex internal links, so there is currently no support in test software to do so.

2.1.2.15 16.0 GT/s Support Detection and Testing

The following only applies to Base 4.x or later testing. The test assumes that all links support at least 2.5 GT/s.

For a function under test that supports 16.0 GT/s, test software will attempt to test it once at 2.5 GT/s (which all PCI Express devices with external links, must support), again at 5.0 GT/s (which is an optional feature starting with Base 2.0), again at 8.0 GT/s (which is an optional feature starting with Base 3.0), and again at 16.0 GT/s (which is an optional feature starting with Base 4.0).

For a function under test that supports greater than 16.0 GT/s, test software will need to limit the link speed to 16.0 GT/s using the Target Link Speed field in the Link Control 2 register, in order to test at this speed.

In order to configure the function under test's external PCI Express link to 16.0 GT/s the following steps are done if the function under test contains an upstream port (e.g., Endpoint, Switch Upstream Port, or PCI Express to PCI/PCI-X Bridge):

1. Read the function under test's Link Capabilities register bits 3-0 value and if it returns 0000b (no link supported), or 0001b (only 2.5 GT/s supported), or 0010b (only 2.5 GT/s and 5.0 GT/s supported), or 0011b (only 2.5 GT/s, 5.0 GT/s, and 8.0 GT/s supported), then no further attempt is made to change the link speed to 16.0 GT/s.
2. Read the immediate downstream port's (the port connected to the function under test) Link Capabilities register bits 3-0 value and if it returns 0000b (no link supported), or 0001b (only 2.5 GT/s supported), or 0010b (only 2.5 GT/s and 5.0 GT/s supported), or 0011b (only 2.5 GT/s, 5.0 GT/s, and 8.0 GT/s supported), then no further attempt is made to change the link speed to 16.0 GT/s.
3. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is set to 0100b (16.0 GT/s) on function 0 of the device containing the function under test. For this write the following fields are also set as follows:
 a. Enter Compliance (bit 4) is set to 0
 b. Hardware Autonomous Speed Disable (bit 5) is set to 1
 c. Transmit Margin (bits 9-7) is set to 000b
 d. Enter Modified Compliance (bit 10) is set to 0
 e. Compliance SOS (bit 11) is set to 0
 f. Compliance Preset/De-emphasis (bits 15-12) is set to 0000b.
4. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is read back and if it does not return 0100b (16.0 GT/s) on function 0 of the device containing the function under test then no further attempt is made to change the link speed to 16.0 GT/s. This is reported as a test failure.

5. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is set to 0100b (16.0 GT/s) on the immediate downstream port (the port connected to the function under test). This port will be referred to as the downstream port of the link. For this write the following fields are also set as follows:
 a. Enter Compliance (bit 4) is set to 0
 b. Hardware Autonomous Speed Disable (bit 5) is set to 1
 c. Transmit Margin (bits 9-7) is set to 000b
 d. Enter Modified Compliance (bit 10) is set to 0
 e. Compliance SOS (bit 11) is set to 0
 f. Compliance Preset/De-emphasis (bits 15-12) is set to 0000b.
6. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is read back and if it does not return 0100b (16.0 GT/s) on the downstream port of the link, then no further attempt is made to change the link speed to 16.0 GT/s (this is not a failure, but the test result for 16.0 GT/s is reported as skipped).
7. The Perform Equalization field (Link Control 3 register) is set to 0 on the downstream port of the link.
8. Test software reads the Link Training field (Link Status register) on the downstream port of the link until it reads 0. If the Link Training field does not return 0 within 1 second, then report this as a link training failure, and skip the remaining steps. (Note: This step is needed to ensure that the next retrain will use the settings programmed by the preceding steps.)
9. Test software writes 1 to the Retrain Link field (Link Control register) on the downstream port of the link using a WORD access, while preserving all the other fields in this register.
10. Test software reads the Link Training field (Link Status register) on the downstream port of the link until it reads 0. If the Link Training field does not return 0 within 1 second, then report this as a link training failure, and skip the remaining steps.
11. Test software reads the Current Link Speed field (Link Status register) in the downstream port of the link. If the value returns 0100b (16.0 GT/s), then skip the remaining steps.
12. Test software writes 1 to the Retrain Link field (Link Control register) on the downstream port of the link using a WORD access, while preserving all the other fields in this register.
13. Test software reads the Link Training field (Link Status register) on the downstream port of the link until it reads 0. If the Link Training field does not return 0 within 1 second, then report this as a link training failure, and skip the remaining steps.
14. Test software reads the Current Link Speed field (Link Status register) in the downstream port of the link. The value must return 0100b (16.0 GT/s). If it does not, then the attempt fails and is reported as a link speed failure.

In order to configure the function under test's external PCI Express link to 16.0 GT/s the following steps are done if the function under test contains a downstream port (e.g., Root Port, Switch Downstream Port, or PCI/PCI-X to PCI Express Bridge):

1. Read the function under test's Link Capabilities register bits 3-0 value and if it returns 0000b (no link supported), or 0001b (only 2.5 GT/s supported), or 0010b (only 2.5 GT/s and 5.0 GT/s

supported), or 0011b (only 2.5 GT/s, 5.0 GT/s, and 8.0 GT/s supported), then no further attempt is made to change the link speed to 16.0 GT/s.

2. Read the immediate upstream port's (connected to the function under test) Link Capabilities register bits 3-0 value and if it returns 0000b (no link supported), or 0001b (only 2.5 GT/s supported), or 0010b (only 2.5 GT/s and 5.0 GT/s supported), or 0011b (only 2.5 GT/s, 5.0 GT/s and 8.0 GT/s supported), then no further attempt is made to change the link speed to 16.0 GT/s.
3. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is set to 0100b (16.0 GT/s) on function 0 of the immediate upstream port (connected to the function under test). For this write the following fields are also set as follows:
 a. Enter Compliance (bit 4) is set to 0
 b. Hardware Autonomous Speed Disable (bit 5) is set to 1
 c. Transmit Margin (bits 9-7) is set to 000b
 d. Enter Modified Compliance (bit 10) is set to 0
 e. Compliance SOS (bit 11) is set to 0
 f. Compliance Preset/De-emphasis (bits 15-12) is set to 0000b.
4. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is read back and if it does not return 0100b (16.0 GT/s) on function 0 of the immediate upstream port (connected to the function under test) then no further attempt is made to change the link speed to 16.0 GT/s (this is not a failure, but the test result for 16.0 GT/s is reported as skipped).
5. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is set to 0100b (16.0 GT/s) on the function under test. For this write the following fields are also set as follows:
 a. Enter Compliance (bit 4) is set to 0
 b. Hardware Autonomous Speed Disable (bit 5) is set to 1
 c. Transmit Margin (bits 9-7) is set to 000b
 d. Enter Modified Compliance (bit 10) is set to 0
 e. Compliance SOS (bit 11) is set to 0
 f. Compliance Preset/De-emphasis (bits 15-12) is set to 0000b.
6. If the Capability Version field (PCI Express Capabilities register) is 2h or greater: the Target Link Speed field (Link Control 2 register) is read back and if it does not return 0100b (16.0 GT/s) on the function under test then no further attempt is made to change the link speed to 16.0 GT/s. This is reported as a test failure.
7. The Perform Equalization field (Link Control 3 register) is set to 0 on the function under test.
8. Test software reads the Link Training field (Link Status register) on the function under test until it reads 0. If the Link Training field does not return 0 within 1 second, then report this as a link training failure, and skip the remaining steps. (Note: This step is needed to ensure that the next retrain will use the settings programmed by the preceding steps.)
9. Test software writes 1 to the Retrain Link field (Link Control register) on the function under test using a WORD access, while preserving all the other fields in this register.

10. Test software reads the Link Training field (Link Status register) on the function under test until it reads 0. If the Link Training field does not return 0 within 1 second, then report this as a link training failure, and skip the remaining steps.
11. Test software reads the Current Link Speed field (Link Status register) in the function under test and if it returns 0100b (16.0 GT/s), then skip the remaining steps.
12. Test software writes 1 to the Retrain Link field (Link Control register) on the function under test using a WORD access, while preserving all the other fields in this register.
13. Test software reads the Link Training field (Link Status register) on the function under test until it reads 0. If the Link Training field does not return 0 within 1 second, then report this as a link training failure, and skip the remaining steps.
14. Test software reads the Current Link Speed field (Link Status register) in the function under test and it must return 0100b (16.0 GT/s). If it does not, then the attempt fails and is reported as a link speed failure.

Note: For the purposes of setting the link speed, test software assumes that for 16.0 GT/s, Link Equalization has already been performed (following reset of the function under test).

Test software cannot control the link speed of Root Complex internal device links (e.g., Root Complex Integrated Endpoints or Root Complex Event Collectors). When a function under test is of this device type, no attempt is made to control the link speed and the test is run only once at whatever link speed the internal link runs at. In addition, some Root Ports may connect to internal links (rather than external links). Test software must only try to change the link speed on such a Root Port's external link (if it has one). It is not currently possible to configure the speed of Root Complex internal links, so there is currently no support in test software to do so.

2.1.2.16 Capability Header Detection

Each implemented function will respond to Configuration Space accesses for addresses 00h to FFh. These functions may optionally implement a Capabilities List containing specific Capability structures. To detect the presence of a specific Capability structure, the following procedure is done.

1. Set the Capability Instances [CAPIN] to 0.
2. Read back a WORD at location 06h (Status register) and if bit 4 is 0, then skip to step 8 as this Bus Number/Device Number/Function Number location does not contain any Capability structures.
3. Read back a byte at location 34h (Capabilities Pointer register) and if 00h is found, then skip to step 8 as this Bus Number/Device Number/Function Number location does not contain any capability structures.
4. Read back a WORD at the address location contained in Capabilities Pointer and record the value in Capability Header [CAPHDR].
5. For [CAPHDR], if bits 7-0 (Capability ID) match the requested Capability ID, increment [CAPIN] by 1, and set the value in the Capability Base address array [CAPBASE(n)] (where n is the value in [CAPIN]) to the address of the last read of [CAPHDR].

6. For [CAPHDR], if bits 15-8 (Next Capability Pointer) are 00h, then skip to step 8 as this Bus Number/Device Number/Function Number location does not contain any more Capability structures.
7. For [CAPHDR], if bits 15-8 are non-zero, read back a WORD at the address location contained in [CAPHDR] bits 15-8 and record the new value in [CAPHDR]. Repeat steps 4-7. There must be a limit of 64 repetitions of this step per function, so that a function that incorrectly implements an infinite loop of Capabilities Pointers will not cause the test to hang. If this limit is reached skip to step 8.
8. Return the Capability base address value array [CAPBASE (n)]. This is the starting address of each instance of the requested Capability ID. Return the number of instances value [CAPIN].

2.1.2.17 Extended Capability Header Detection

Each implemented PCI Express function will respond to Configuration Space accesses for addresses 100h to FFFh. These functions may optionally implement an Extended Capabilities List containing specific Extended Capability structures. To detect the presence of a specific Extended Capability structure, the following procedure is done.

1. Set the Extended Capability Instances [ECAPIN] to 0.
2. Read back a DWORD at the address location 100h and record the value in Extended Capability Header [ECAPHDR].
3. For [ECAPHDR], if bits 15-0 (Extended Capability ID) match the requested Extended Capability ID, increment [ECAPIN] by 1, and set the value in the Extended Capability Base address array [ECAPBASE (n)] (where n is the value in [ECAPIN]) to the address of the last read of [ECAPHDR].
4. For [ECAPHDR], if bits 31-20 (Next Capability Offset) are 000h, then skip to step 6 as this Bus Number/Device Number/Function Number location does not contain any more Extended Capability structures.
5. For [ECAPHDR], if bits 31-20 are non-zero, read back a DWORD at the address location contained in [ECAPHDR] bits 31-20 and record the new value in [ECAPHDR]. Repeat steps 3-5. There must be a limit of 1024 repetitions of this step per function, so that a function that incorrectly implements an infinite loop of Extended Capabilities Pointers will not cause the test to hang. If this limit is reached skip to step 6.
6. Return the Extended Capability base address value array [ECAPBASE (n)]. This is the starting address of each instance of the requested Extended Capability ID. Return the number of instances value [ECAPIN].

2.1.2.18 Trusted Configuration Space Header Detection

Support for Trusted Configuration Space has been removed starting at Base 2.0. Therefore, the test no longer supports Trusted Configuration Space.

2.1.2.19 RCRB Detection and Testing

For a function within a Root Complex, a Root Complex Register Block (RCRB) can be associated with the function. An RCRB can also be associated with another RCRB. The RCRB can be used to

control multiple functions within the Root Complex. An RCRB contains registers that are similar to the registers normally defined to occupy extended configuration space in a PCI Express function, except for the following differences:

- An RCRB always resides in Memory Space.
- An RCRB's base address is given by a Link Address in a valid Link Entry of the appropriate Element Type.
- Offset 000h in the RCRB contains either an Extended Capability structure header, or else it contains 000x FFFFh (where x means bits 19-16 are don't cares), indicating the RCRB is empty.
- Only a sub-set of Extended Capability structures are allowed to be implemented in an RCRB.

To detect an RCRB, the following steps are done by test software:

1. For the function under test, check the Device/Port Type field (PCI Express Capabilities register) and see that it is either a Root Port or a Root Complex Integrated Endpoint. Otherwise there is no RCRB associated with it.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0005h (Root Complex Link Declaration Extended Capability) are found. If only one is found, then an RCRB may be present. Otherwise there is no RCRB present.
3. Check the Number of Link Entries (Element Self Description register) in the Root Complex Link Declaration Extended Capability and record the number (this indicates how many Link Entries must be scanned).
4. Check each Link Entry in the Root Complex Link Declaration Extended Capability (up to the Number of Link Entries value). Each Link Entry is checked for all the following:
 a. Either Link Valid (Link Description register) returns 1 or Associate RCRB Header (Link Description register) returns 1 (both may return 1 as well).
 b. Link Type (Link Description register) indicates Memory Space (returns 0).

 If a Link Entry contains all of these, it is one that identifies the base address of a potential RCRB. The Link Address registers (bits 63-0) is recorded as a potential RCRB base address. Once every one of the Link Entries are checked, every individual entry in the list of potential RCRB base addresses is used to perform step 5.
5. Read the memory space address location given by the potential RCRB base address and if it returns 000x FFFFh (where x means bits 19-16 are don't cares) then this RCRB is empty. Otherwise, this is the base address of an RCRB. Repeat this step until each potential RCRB base address has been checked.
6. Repeat steps 2-5, using each discovered RCRB, to see if the RCRB is associated with another RCRB. Since association is bi-directional, each individual association will have a reciprocal association in the target, therefore each individual associated RCRB should only be counted once during the association parsing process. However, all RCRB associations must be parsed in order to determine the total number of RCRBs associated with the function under test.
7. Any function that contains a link to a valid RCRB should be tested more than once, for any test that checks PCI Express Extended Configuration Space capabilities. Such a function should be first tested using only its Extended Configuration space area, and then the test case should be

re-run using every RCRB (memory space) area associated with the function, or associated with other RCRBs that are themselves associated with the function.

8. Any function that is associated with a valid RCRB is only tested once, for any test that checks PCI Configuration Space capabilities. Such a function should be tested once using only its PCI Configuration space area.

2.1.2.20 Determination of Function, Base Function, Physical Function, or Virtual Function

An Endpoint function may be defined as a Function, a Base Function (BF), a Physical Function (PF), or a Virtual Function (VF). The characteristics of each function type are as follows:

- A Function returns a Vendor ID that is not FFFFh and not 0001h (CRS Software Visibility notification), and does not contain a SR-IOV Extended Capability.
- A BF returns a Vendor IF that is not FFFFh and not 0001h (CRS Software Visibility notification), and contains a MR-IOV Extended Capability.
- A PF returns a Vendor ID that is not FFFFh and not 0001h (CRS Software Visibility notification), and contains a SR-IOV Extended Capability.
- A VF returns a Vendor ID that is FFFFh (at a Bus/Device/Function address where a VF is indicated to be at).

In order for the test case to determine what type of Endpoint function the function under test is, the following sequence is followed:

1. Examine the Capability ID field for each of the function's Capability structures. Determine how many instances of the Capability ID of 10h (PCI Express Capability) are found. If none are found, this is not a Function, BF, PF, or VF so return this and stop further evaluation.
2. Having found the PCI Express Capability in this function under test, read a DWORD at offset 02h (PCI Express Capabilities register) in the PCI Express Capability structure and check the Device/Port Type to see that it is a PCI Express Endpoint, a Legacy Endpoint or a Root Complex Integrated Endpoint. If it is not one of these, then this is not a Function, BF, PF, or VF so return this and stop further evaluation.
3. Read back a WORD at location 00h (Vendor ID register) in Configuration Space and if FFFFh is found, this is a VF so return this and stop further evaluation.
4. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0011h (MR-IOV Extended Capability) are found. If none are found this function is not a BF, so continue with further evaluation.
5. If a MR-IOV Extended Capability was found this function is a BF, so return this and stop further evaluation.
6. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0010h (SR-IOV Extended Capability) are found. If none are found this function is a Function, so return this and stop further evaluation.

7. If a SR-IOV Extended Capability was found this function is a PF, so return this and stop further evaluation.

2.1.2.21 ASPM Testing Tables

For tests that enable ASPM, the different testing levels use different interpretations of the Active State Power Management (ASPM) Support field in the Link Capabilities register. Prior to the ASPM Optionality ECN to the Base 2.1 Specification, RxL0s support was mandatory and this field only had three settings: No ASPM; TxL0s Supported; L1+TxL0s Supported. After this ECN, the field had four settings: No ASPM; TxL0s+RxL0s Supported; L1 Supported; L1+TxL0s+RxL0s Supported. This difference in interpretations means that the different ASPM test combinations are defined, depending on the implementation of the port on each side of the link. The test combinations are listed in the following tables and are referenced by the applicable test descriptions.

The tables use two values for the Active State Power Management (ASPM) Control field in the Link Control register: Upstream ASPM Control [UASPMC] which is the value returned by the upstream port of the link and Downstream ASPM Control [DASPMC] which is the value returned by the downstream port of the link. The tables use two values for the Active State Power Management (ASPM) Support field in the Link Capabilities register: Upstream ASPM Support [UASPMS] which is the value returned by the upstream port of the link and Downstream ASPM Support [DASPMS] which is the value returned by the downstream port of the link.

2.1.2.21.1 Table 1 – Neither Port Supports ASPM Optionality

This table lists the combinations of ASPM settings that will be tested when the ports on both sides of the link do not support ASPM Optionality (ASPM Optionality Compliance field in Link Capabilities register reports 0).

Test Setting	Upstream Port of Link	Downstream Port of Link
1	[UASPMC] = 00b (Disabled)	[DASPMC] = 00b (Disabled)
2	[UASPMC] = 00b (Disabled)	[DASPMC] = 01b (L0s only) (Setting valid only if [DASPMS] = 01b or 11b)
3	[UASPMC] = 01b (L0s only) (Setting valid only if [UASPMS] = 01b or 11b)	[DASPMC] = 00b (Disabled)
4	[UASPMC] = 01b (L0s only) (Setting valid only if [UASPMS] = 01b or 11b)	[DASPMC] = 01b (L0s only) (Setting valid only if [DASPMS] = 01b or 11b)
5	[UASPMC] = 10b (L1 only) (Setting valid only if [UASPMS] = 11b)	[DASPMC] = 00b (Disabled)
6	[UASPMC] = 10b (L1 only) (Setting valid only if [UASPMS] = 11b)	[DASPMC] = 01b (L0s only) (Setting valid only if [DASPMS] = 01b or 11b)
7	[UASPMC] = 10b (L1 only) (Setting valid only if [UASPMS] = 11b)	[DASPMC] = 10b (L1 only) (Setting valid only if [DASPMS] = 11b)
8	[UASPMC] = 10b (L1 only) (Setting valid only if [UASPMS] = 11b)	[DASPMC] = 11b (L0s and L1) (Setting valid only if [DASPMS] = 11b)
9	[UASPMC] = 11b (L0s and L1) (Setting valid only if [UASPMS] = 11b)	[DASPMC] = 00b (Disabled)
10	[UASPMC] = 11b (L0s and L1) (Setting valid only if [UASPMS] = 11b)	[DASPMC] = 01b (L0s only) (Setting valid only if [DASPMS] = 01b or 11b)
11	[UASPMC] = 11b (L0s and L1) (Setting valid only if [UASPMS] = 11b)	[DASPMC] = 10b (L1 only) (Setting valid only if [DASPMS] = 11b)
12	[UASPMC] = 11b (L0s and L1) (Setting valid only if [UASPMS] = 11b)	[DASPMC] = 11b (L0s and L1) (Setting valid only if [DASPMS] = 11b)

Table 2: Neither Port Supports ASPM Optionality

2.1.2.21.2 Table 2 – Only Upstream Port Supports ASPM Optionality

This table lists the combinations of ASPM settings that will be tested when the upstream port on the link supports ASPM Optionality (ASPM Optionality Compliance field in Link Capabilities register reports 1), but the downstream port of the link does not.

Test Setting	Upstream Port of Link	Downstream Port of Link
1	[UASPMC] = 00b (Disabled)	[DASPMC] = 00b (Disabled)
2	[UASPMC] = 00b (Disabled)	[DASPMC] = 01b (L0s only) (Setting valid only if [DASPMS] = 01b or 11b)
3	[UASPMC] = 01b (L0s only) (Setting valid only if ([UASPMS] = 01b or 11b) and ([DASPMS] = 01b or 11b))	[DASPMC] = 00b (Disabled)
4	[UASPMC] = 01b (L0s only) (Setting valid only if ([UASPMS] = 01b or 11b) and ([DASPMS] = 01b or 11b))	[DASPMC] = 01b (L0s only) (Setting valid only if [DASPMS] = 01b or 11b)
5	[UASPMC] = 10b (L1 only) (Setting valid only if [UASPMS] = 10b or 11b)	[DASPMC] = 00b (Disabled)
6	[UASPMC] = 10b (L1 only) (Setting valid only if [UASPMS] = 10b or 11b)	[DASPMC] = 01b (L0s only) (Setting valid only if [DASPMS] = 01b or 11b)
7	[UASPMC] = 10b (L1 only) (Setting valid only if [UASPMS] = 10b or 11b)	[DASPMC] = 10b (L1 only) (Setting valid only if [DASPMS] = 11b)
8	[UASPMC] = 10b (L1 only) (Setting valid only if [UASPMS] = 10b or 11b)	[DASPMC] = 11b (L0s and L1) (Setting valid only if [DASPMS] = 11b)
9	[UASPMC] = 11b (L0s and L1) (Setting valid only if ([UASPMS] = 11b) and ([DASPMS] = 01b or 11b))	[DASPMC] = 00b (Disabled)
10	[UASPMC] = 11b (L0s and L1) (Setting valid only if ([UASPMS] = 11b) and ([DASPMS] = 01b or 11b))	[DASPMC] = 01b (L0s only) (Setting valid only if [DASPMS] = 01b or 11b)
11	[UASPMC] = 11b (L0s and L1) (Setting valid only if ([UASPMS] = 11b) and ([DASPMS] = 01b or 11b))	[DASPMC] = 10b (L1 only) (Setting valid only if [DASPMS] = 11b)
12	[UASPMC] = 11b (L0s and L1) (Setting valid only if ([UASPMS] = 11b) and ([DASPMS] = 01b or 11b))	[DASPMC] = 11b (L0s and L1) (Setting valid only if [DASPMS] = 11b)

Table 3: Only Upstream Port Supports ASPM Optionality

2.1.2.21.3 Table 3 – Only Downstream Port Supports ASPM Optionality

This table lists the combinations of ASPM settings that will be tested when the downstream port on the link supports ASPM Optionality (ASPM Optionality Compliance field in Link Capabilities register reports 1), but the upstream port of the link does not.

Test Setting	Upstream Port of Link	Downstream Port of link
1	[UASPMC] = 00b (Disabled)	[DASPMC] = 00b (Disabled)
2	[UASPMC] = 00b (Disabled)	[DASPMC] = 01b (L0s only) (Setting valid only if ([DASPMS] = 01b or 11b) and ([UASPMS] = 01b or 11b))
3	[UASPMC] = 01b (L0s only) (Setting valid only if [UASPMS] = 01b or 11b)	[DASPMC] = 00b (Disabled)
4	[UASPMC] = 01b (L0s only) (Setting valid only if [UASPMS] = 01b or 11b)	[DASPMC] = 01b (L0s only) (Setting valid only if ([DASPMS] = 01b or 11b) and ([UASPMS] = 01b or 11b))
5	[UASPMC] = 10b (L1 only) (Setting valid only if [UASPMS] = 11b)	[DASPMC] = 00b (Disabled)
6	[UASPMC] = 10b (L1 only) (Setting valid only if [UASPMS] = 11b)	[DASPMC] = 01b (L0s only) (Setting valid only if ([DASPMS] = 01b or 11b) and ([UASPMS] = 01b or 11b))
7	[UASPMC] = 10b (L1 only) (Setting valid only if [UASPMS] = 11b)	[DASPMC] = 10b (L1 only) (Setting valid only if [DASPMS] = 10b or 11b)
8	[UASPMC] = 10b (L1 only) (Setting valid only if [UASPMS] = 11b)	[DASPMC] = 11b (L0s and L1) (Setting valid only if ([DASPMS] = 11b) and ([UASPMS] = 01b or 11b))
9	[UASPMC] = 11b (L0s and L1) (Setting valid only if [UASPMS] = 11b)	[DASPMC] = 00b (Disabled)
10	[UASPMC] = 11b (L0s and L1) (Setting valid only if [UASPMS] = 11b)	[DASPMC] = 01b (L0s only) (Setting valid only if ([DASPMS] = 01b or 11b) and ([UASPMS] = 01b or 11b))
11	[UASPMC] = 11b (L0s and L1) (Setting valid only if [UASPMS] = 11b)	[DASPMC] = 10b (L1 only) (Setting valid only if [DASPMS] = 10b or 11b)
12	[UASPMC] = 11b (L0s and L1) (Setting valid only if [UASPMS] = 11b)	[DASPMC] = 11b (L0s and L1) (Setting valid only if ([DASPMS] = 11b) and ([UASPMS] = 01b or 11b))

Table 4: Only Downstream Port Supports ASPM Optionality

2.1.2.21.4 Table 4 – Both Ports Support ASPM Optionality

This table lists the combinations of ASPM settings that will be tested when both of the ports on the link support ASPM Optionality (ASPM Optionality Compliance field in Link Capabilities register reports 1).

Test Setting	Upstream Port of Link	Downstream Port of Link
1	[UASPMC] = 00b (Disabled)	[DASPMC] = 00b (Disabled)
2	[UASPMC] = 00b (Disabled)	[DASPMC] = 01b (L0s only) (Setting valid only if ([DASPMS] = 01b or 11b) and ([UASPMS] = 01b or 11b))
3	[UASPMC] = 01b (L0s only) (Setting valid only if ([UASPMS] = 01b or 11b) and ([DASPMS] = 01b or 11b))	[DASPMC] = 00b (Disabled)
4	[UASPMC] = 01b (L0s only) (Setting valid only if ([UASPMS] = 01b or 11b) and ([DASPMS] = 01b or 11b))	[DASPMC] = 01b (L0s only) (Setting valid only if ([DASPMS] = 01b or 11b) and ([UASPMS] = 01b or 11b))
5	[UASPMC] = 10b (L1 only) (Setting valid only if [UASPMS] = 10b or 11b)	[DASPMC] = 00b (Disabled)
6	[UASPMC] = 10b (L1 only) (Setting valid only if [UASPMS] = 10b or 11b)	[DASPMC] = 01b (L0s only) (Setting valid only if ([DASPMS] = 01b or 11b) and ([UASPMS] = 01b or 11b))
7	[UASPMC] = 10b (L1 only) (Setting valid only if [UASPMS] = 10b or 11b)	[DASPMC] = 10b (L1 only) (Setting valid only if [DASPMS] = 10b or 11b)
8	[UASPMC] = 10b (L1 only) (Setting valid only if [UASPMS] = 10b or 11b)	[DASPMC] = 11b (L0s and L1) (Setting valid only if ([DASPMS] = 11b) and ([UASPMS] = 01b or 11b))
9	[UASPMC] = 11b (L0s and L1) (Setting valid only if ([UASPMS] = 11b) and ([DASPMS] = 01b or 11b))	[DASPMC] = 00b (Disabled)
10	[UASPMC] = 11b (L0s and L1) (Setting valid only if ([UASPMS] = 11b) and ([DASPMS] = 01b or 11b))	[DASPMC] = 01b (L0s only) (Setting valid only if ([DASPMS] = 01b or 11b) and ([UASPMS] = 01b or 11b))
11	[UASPMC] = 11b (L0s and L1) (Setting valid only if ([UASPMS] = 11b) and ([DASPMS] = 01b or 11b))	[DASPMC] = 10b (L1 only) (Setting valid only if [DASPMS] = 10b or 11b)
12	[UASPMC] = 11b (L0s and L1) (Setting valid only if ([UASPMS] = 11b) and ([DASPMS] = 01b or 11b))	[DASPMC] = 11b (L0s and L1) (Setting valid only if ([DASPMS] = 11b) and ([UASPMS] = 01b or 11b))

Table 5: Both Ports Support ASPM Optionality

2.2. Configuration Register Tests (All Devices)

2.2.1. TD_1_1 user-specified PCI Register (Debug Mode only)

The test is intended for debug mode use only. It will run a user-supplied file (1_01.ini in the ini folder) that can be modified by the user to verify any register field or fields in Configuration Space. This provides a means for the user to test fields that are either vendor-specific, or are newly defined and not yet supported by the current program release.

This test is not part of a normal test run and it can only be run using the "Run Register and Capability Tests in Debug Mode" selection.

Note: The ini folder contains a file called sample.ini, which documents the syntax required for .ini files.

Relevant Specifications

- *user-specific*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. The following register field characteristic checks are performed:

 user-specified PCI Register (user-specified Offset) – user-specified size
 a. user-specified
3. The following default value checks are performed:

 user-specified PCI Register Default Value (user-specified Offset) – user-specified size
 a. user-specified

 Note: The "user-specified Offset" starts at 000h (the starting address of a function's Configuration Space) and can range up to FFFh (the highest address of a function's Configuration Space). The "user-specified size" are the standard sizes for Configurations Space registers (BYTE, WORD, DWORD).

4. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.

c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- Any of the user-specified register field characteristic tests fail.
- Any of the user-specified default value tests fail.

2.2.2. TD_1_2 PCI Express Capability Structure

The test verifies that if the function under test reports a PCI Express Capability structure, it implements the required registers for the device/port type and capability version as defined in the relevant specifications. (The individual register field contents are not checked, they will be checked by other tests.)

Relevant Specifications

- *PCI Express Base Specification*
- *ECN PCI Express Capability Structure Expansion (to Base 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Capability ID field for each of the function's Capability structures. Determine how many instances of the Capability ID of 10h (PCI Express Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Capability ID of 10h is not found in a Capability structure, the test terminates with a failure.
4. If the Capability ID of 10h is found in a Capability structure, read the DWORD at offset 00h, and use the contents of the PCI Express Capabilities register (Capability Version field, Device/Port Type field, and Slot Implemented field) to determine the total size of the PCI Express Capability structure.
5. Attempt to read the indicated size from each of the following additional offsets (test software records if any of these read attempts fail to complete, but does not check the value returned):
 a. If the Capability Version field is 0h, this is recorded as a failure and the test terminates.
 b. If the Capability Version field is 1h:
 i. If the Device/Port Type field is 0h (Endpoint), or 01h (Legacy Endpoint), or 05h (Switch Upstream Port), or 07h (PCI Express to PCI/PCI-X Bridge): 04h (DWORD); 08h (WORD); 0Ah (WORD); 0Ch (DWORD); 10h (WORD).

ii. If the Device/Port Type field is 4h (Root Port) and Slot Implemented is 0: 04h (DWORD); 08h (WORD); 0Ah (WORD); 0Ch (DWORD); 10h (WORD); 1Ch (WORD); 1Eh (WORD); 20h (DWORD).
iii. If the Device/Port Type field is 4h (Root Port) and Slot Implemented is 1: 04h (DWORD); 08h (WORD); 0Ah (WORD); 0Ch (DWORD); 10h (WORD); 14h (DWORD); 18h (WORD); 1Ah (WORD); 1Ch (WORD); 1Eh (WORD); 20h (DWORD).
iv. If the Device/Port Type field is 6h (Switch Downstream Port) and Slot Implemented is 0, or 8h (PCI/PCI-X to PCI Express Bridge) and Slot Implemented is 0: 04h (DWORD); 08h (WORD); 0Ah (WORD); 0Ch (DWORD); 10h (WORD).
v. If the Device/Port Type field is 6h (Switch Downstream Port) and Slot Implemented is 1, or 8h (PCI/PCI-X to PCI Express Bridge) and Slot Implemented is 1: 04h (DWORD); 08h (WORD); 0Ah (WORD); 0Ch (DWORD); 10h (WORD); 14h (DWORD); 18h (WORD); 1Ah (WORD).
vi. If the Device/Port Type field is 9h (Root Complex Integrated Endpoint): 04h (DWORD); 08h (WORD); 0Ah (WORD).
vii. If the Device/Port Type field is Ah (Root Complex Event Collector): 04h (DWORD); 08h (WORD); 0Ah (WORD); 1Ch (WORD); 1Eh (WORD); 20h (DWORD).

c. If the Capability Version field is 2h or greater: 00h (DWORD); 04h (DWORD); 08h (WORD); 0Ah (WORD); 0Ch (DWORD); 10h (WORD); 12h (WORD); 14h (DWORD); 18h (WORD); 1Ah (WORD); 1Ch (WORD); 1Eh (WORD); 20h (DWORD); 24h (DWORD); 28h (WORD); 2Ah (WORD); 2Ch (DWORD); 30h (WORD); 32h (WORD); 34h (DWORD); 38h (WORD); 3Ah (WORD).

6. The Next Capability Pointer field must be 00h or greater than 3Fh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.

7. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- A PCI Express Capability structure is not present.
- More than one PCI Express Capability structure is present.
- A non-zero Next Capability Pointer is less than or equal to 3Fh, or the lower 2 bits are non-zero.
- A valid register access within the PCI Express Capability structure fails to complete.

2.2.3. TD_1_3 PCI Express Capabilities Register

The test verifies that the function under test implements the PCI Express Capabilities register as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *ECN Trusted Configuration Space (to Base 1.1)*

- *PCI Local Bus Specification, Revision 3.0 (Base 3.x or earlier only)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Capability ID field for each of the function's Capability structures. Determine how many instances of the Capability ID of 10h (PCI Express Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Capability ID of 10h is not found in a Capability structure, the test terminates with a failure.
4. If the Capability ID of 10h is found in a Capability structure, the following tests are performed on that Capability structure:
5. Read a WORD located at offset 02h in the PCI Express Capability structure.
6. Perform each of the following checks on the fields of the WORD read:
 a. For Base 1.x testing: the Capability Version field must be 1h or 2h. If not, this is recorded as a failure, and the test terminates.
 b. For Base 2.x or later testing: the Capability Version field must be 2h. Any other value is processed as follows:
 i. If the value is 0h, then this is recorded as a failure and the test terminates.
 ii. If the value is 1h, then this is recorded as a failure, but the test continues.
 iii. If the value is greater than 2h, then this is recorded as a failure, but the test continues.
 c. The Device/Port Type field must be 0000b, 0001b, 0100b, 0101b, 0110b, 0111b, 1000b, 1001b, or 1010b. All other encodings are reserved and are recorded as a failure, but the test continues.
7. Read a byte at location 0Eh (Header Type register) and check that the value in bits 6-0 is either 000 0000b (Type 0 Configuration Space Header) or 000 0001b (Type 1 Configuration Space Header). All other encodings are reserved and are recorded as a failure, but the test continues. If the device implements a valid Configuration Space Header type the following checks are performed and if any are not as stated, this is recorded as a failure, but the test continues:
 a. For Type 0 Configuration Space Header, the Device/Port Type field must be 0000b (Endpoint), 0001b (Legacy Endpoint), 1001b (Root Complex Integrated Endpoint), or 1010b (Root Complex Event Collector).
 b. For Type 1 Configuration Space Header, the Device/Port Type field must be 0100b (Root Port), 0101b (Switch Upstream Port), 0110b (Switch Downstream Port), 0111b (PCI Express to PCI/PCI-X Bridge), or 1000b (PCI/PCI-X to PCI Express Bridge).

8. If the Slot Implemented field returns 1, the Device/Port Type field must be 0100b (Root Port), 0110b (Switch Downstream Port), or 1000b (PCI/PCI-X to PCI Express Bridge). If not, this is recorded as a failure, but the test continues.
9. The following register field characteristic checks are performed:

PCI Express Capability Header (Offset 00h) — WORD

a. Capability ID	RO
b. Next Capability Pointer	RO

PCI Express Capabilities Register (Offset 02h) — DWORD

a. Capability Version	RO
b. Device/Port Type	RO
c. Slot Implemented	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
d. Interrupt Message Number	RO
e. Undefined_14	RO
Note: This was once TCS Routing Supported.	
f. RsvdP_15	RO-Zero

10. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- ❑ A PCI Express Capability structure is not present.
- ❑ More than one PCI Express Capability structure is present.
- ❑ The Capability Version field is not 1h or 2h (for a Base 1.x compliant test).
- ❑ The Capability Version field is not 2h (for a Base 2.x or later compliant test).
- ❑ The Device/Port Type field is not one of the defined values.
- ❑ The Header Layout field is neither a Type 0 nor a Type 1 Configuration Space Header type.
- ❑ The PCI Configuration Space Header type does not match the requirements of the Device/Port Type.
- ❑ The Slot Implemented field is 1 and the Device/Port Type field is not one of the following: 0100b (Root Port); 0110b (Switch Downstream Port); 1000b (PCI/PCI-X to PCI Express Bridge).
- ❑ Any of the register field characteristic tests fail.

2.2.4. TD_1_4 Device Capabilities, Device Control, and Device Status Registers

The test verifies that the function under test implements the PCI Express Device Capabilities, Device Control, and Device Status registers as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *ECN Function Level Reset (to Base 1.1)*
- *ECN Alternate Routing-ID Interpretation (to Base 2.0 and Base 1.1)*
- *ECN Extended Tag Enable Default (to Base 2.0)*
- *Single Root I/O Virtualization and Sharing Specification (Base 3.x or earlier only)*
- *Multi-Root I/O Virtualization and Sharing Specification Revision 1.0*
- *ECN Emergency Power Reduction mechanism with PWRBRK signal (to Base 3.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Capability ID field for each of the function's Capability structures. Determine how many instances of the Capability ID of 10h (PCI Express Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Capability ID of 10h is not found in a Capability structure, the test terminates with a failure.
4. If the Capability ID of 10h is found in a Capability, the following tests are performed on that Capability structure:
5. Read a DWORD located at offset 04h (Device Capabilities register) in the PCI Express Capability structure.
6. Perform each of the following checks on the fields of the DWORD read:
7. The Max_Payload_Size Supported field must not return 110b or 111b (Reserved), if it does this is recorded as a failure, but the test continues. Test software writes the value read from the Max_Payload_Size Supported field into the Max_Payload_Size field. Test software then reads back the Max_Payload_Size field and ensures that the written value is returned. If not, this is recorded as a failure, but the test continues. This test is repeated for each value (including 0) less than the value read from the Max_Payload_Size Supported field.

8. The following checks are performed on the Phantom Functions Supported field and if any are not as stated, this is recorded as a failure, but the test continues:
 a. Returned value is 01b:
 i. The function must not be part of a multi-function device using functions 4, 5, 6, or 7.
 ii. The function must not be a function of an ARI device.
 iii. The function must not be a VF.
 b. Returned value is 10b:
 i. The function must not be part of a multi-function device using functions 2, 3, 4, 5, 6, or 7.
 ii. The function must not be a function of an ARI device.
 iii. The function must not be a VF.
 c. Returned value is 11b:
 i. The function must not be part of a multi-function device.
 ii. The function must not be a function of an ARI device.
 iii. The function must not be a VF.
9. For Base 4.x or later testing: if the Extended Tag Field Supported field returns 0, the 10-Bit Tag Requester Supported field (Device Capabilities 2 register) must be 0. If not, this is recorded as a failure, but the test continues.
10. If the Function Level Reset Capability field returns 1, the Device/Port Type field (PCI Express Capabilities register) must be 0000b (Endpoint), 0001b (Legacy Endpoint), or 1001b (Root Complex Integrated Endpoint). If not, this is recorded as a failure, but the test continues.
11. If the Device/Port Type field (PCI Express Capabilities register) is 0000b (Endpoint), 0001b (Legacy Endpoint), or 1001b (Root Complex Integrated Endpoint), the following tests are performed:
 a. If the function is not a VF and if the function implements a SR-IOV Extended Capability structure or a MR-IOV Extended Capability structure, the Function Level Reset Capability field must return 1. If it does not this is recorded as a failure, but the test continues.
 b. If the function is not a VF and if the function does not implement either a SR-IOV Extended Capability structure or a MR-IOV Extended Capability structure, then the Function Level Reset Capability field should return 1. If it does not a warning message is issued, but this is not treated in itself as a failure.
12. The following register field characteristic checks are performed:

Device Capabilities Register (Offset 04h) — DWORD

a. Max_Payload_Size Supported	RO
b. Phantom Functions Supported	
(for VFs and ARI functions)	RO-Zero
(otherwise)	RO
c. Extended Tag Field Supported	RO
d. Endpoint L0s Acceptable Latency	
(for Endpoints)	RO
(for non-Endpoints)	RO-Zero
e. Endpoint L1 Acceptable Latency	
(for Endpoints)	RO
(for non-Endpoints)	RO-Zero
f. Undefined_12	RO

Note: This was once Attention Button Present.

g. Undefined_13 — RO

Note: This was once Attention Indicator Present.

h. Undefined_14 — RO

Note: This was once Power Indicator Present.

i. Role-Based Error Reporting — RO-Ones

j. RsvdP_17-16 — RO-Zero

k. Captured Slot Power Limit Value
(for Endpoints excluding VFs, Switch Upstream Ports, or PCI Express to PCI/PCI-X Bridges)
(for non-FLR testing) — RO
(for FLR testing) — ROS

l. Captured Slot Power Limit Scale
(for Endpoints excluding VFs, Switch Upstream Ports, or PCI Express to PCI/PCI-X Bridges)
(for non-FLR testing) — RO
(for FLR testing) — ROS

m. Function Level Reset Capability
(for VFs) — RO-Ones
(for Endpoints excluding VFs) — RO
(for non-Endpoints) — RO-Zero

n. RsvdP_31-29 — RO-Zero

Device Control Register (Offset 08h) — WORD

a. Correctable Error Reporting Enable
(for RC Integrated Endpoints) — RW or RO-Zero
(for VFs) — RO-Zero
(for all others) — RW

b. Non-Fatal Error Reporting Enable
(for RC Integrated Endpoints) — RW or RO-Zero
(for VFs) — RO-Zero
(for all others) — RW

c. Fatal Error Reporting Enable
(for RC Integrated Endpoints) — RW or RO-Zero
(for VFs) — RO-Zero
(for all others) — RW

d. Unsupported Request Reporting Enable
(for RC Integrated Endpoints) — RW or RO-Zero
(for VFs) — RO-Zero
(for all others — RW

e. Enable Relaxed Ordering
(for VFs) — RO-Zero
(otherwise) — RW or RO-Zero

f. Max_Payload_Size
 (for VFs) RO-Zero
 (otherwise)
 (if Max_Payload_Size Supported is 000b)
 (for non-FLR testing) RW or RO-Zero
 (for FLR testing) RWS or RO-Zero
 (if Max_Payload_Size Supported is non-zero)
 (for non-FLR testing) RW
 (for FLR testing) RWS
g. Extended Tag Field Enable
 (if Extended Tag Field Supported is 1) RW
 (if Extended Tag Field Supported is 0) RO-Zero
h. Phantom Functions Enable
 (if Phantom Functions Supported is non-zero) RW
 (if Phantom Functions Supported is 0) RO-Zero
i. Aux Power PM Enable
 (for VFs) RO-Zero
 (otherwise)
 (if Aux Current is non-zero in PM Capability) RWS
 (if Aux Current is 000b in PM Capability) RWS or RO-Zero
j. Enable No Snoop
 (for VFs) RO-Zero
 (otherwise) RW or RO-Zero
k. Max_Read_Request_Size
 (for VFs) RO-Zero
 (otherwise) RW or RO-Zero
l. Bridge Configuration Retry Enable
 /Initiate Function Level Reset
 (for PCI Express to PCI/PCI-X Bridge) RW
 (for Endpoints with Function Level Reset Capability as 1) RO-Zero
 Note: For Endpoints, writing the Initiate Function Level Reset field causes the function to reset to its default state if supported (the Function Level Reset Capability field returns 1). Test software must wait 100 ms after writing this field to 1 (if the Function Level Reset Capability field returns 1), before reading any register in this function. The Initiate Function Level Reset field always returns 0 when read.
m. RsvdP_15
 (for Endpoints with Function Level Reset Capability as 0) RO-Zero
 (for non-Endpoints and non-PCI Express to PCI/PCI-X Bridges) RO-Zero

Device Status Register (Offset 0Ah) — WORD

a. Correctable Error Detected RW1C
b. Non-Fatal Error Detected RW1C
c. Fatal Error Detected RW1C

d. Unsupported Request Detected	RW1C
e. AUX Power Detected	
(for VFs)	RO-Zero
(otherwise)	RO
f. Transactions Pending	RO
g. Emergency Power Reduction Detected	
(For Base 3.1 or later testing)	
(for VFs)	RO-Zero
(for RC Integrated Endpoints, RC Event Collectors, or Downstream Ports)	RO-Zero
(for Upstream Ports excluding VFs, if Emergency Power Reduction Supported is not 00b)	RW1C
(for Upstream Ports excluding VFs, if Emergency Power Reduction Supported is 00b)	RO-Zero
h. RsvdZ_15-7	
(For Base 3.1 or later testing)	RO-Zero
i. RsvdZ_15-6	
(For Base 3.0 or earlier testing)	RO-Zero

13. The following default value checks are performed:

Device Control Register Default Value (Offset 08h) –– WORD

a. Correctable Error Reporting Enable	0
b. Non-Fatal Error Reporting Enable	0
c. Fatal Error Reporting Enable	0
d. Unsupported Request Reporting Enable	0
e. Enable Relaxed Ordering	
(for non-VFs with Enable Relaxed Ordering as RW)	1
f. Max_Payload_Size	
(for functions with a link)	000b
g. Extended Tag Field Enable	
(if Extended Tag Field Supported is 1)	1 or 0 (Based on design)
h. Phantom Functions Enable	0
i. Enable No Snoop	
(for non-VFs with Enable No Snoop as RW)	1
j. Max_Read_Request_Size	
(for non-VFs with Max_Read_Request_Size as RW)	010b
k. Bridge Configuration Retry Enable/Initiate Function Level Reset	
(for PCI Express to PCI/PCI-X Bridge)	0

Device Status Register Default Value (Offset 0Ah) –– WORD

a. Correctable Error Detected	0
b. Non-Fatal Error Detected	0
c. Fatal Error Detected	0
d. Unsupported Request Detected	0
e. Transactions Pending	0
f. Emergency Power Reduction Detected	
(For Base 3.1 or later testing)	0

14. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- A PCI Express Capability structure is not present.
- More than one PCI Express Capability structure is present.
- A supported value written to the Max_Payload_Size control field is not read back.
- A reserved value is read from the Max_Payload_Size Supported field.
- The function under test is part of an ARI device, a VF function, or is part of a multi-function device that makes the reported non-zero value in the Phantom Functions Supported field invalid.
- The Extended Tag Field Supported field is not set in any function that has the 10-Bit Tag Requester Supported field set (for Base 4.x or later testing only).
- The Function Level Reset Capable field is set in any function other than the following: Endpoint; Legacy Endpoint; Root Complex Integrated Endpoint.
- For an Endpoint, Legacy Endpoint, or Root Complex Integrated Endpoint, that implements either a SR-IOV Extended Capability structure or a MR-IOV Extended Capability structure, the Function Level Reset Capable field is not set.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

The test *warns* if:

- For an Endpoint, Legacy Endpoint, or Root Complex Integrated Endpoint, that implements neither a SR-IOV Extended Capability structure nor a MR-IOV Extended Capability structure, the Function Level Reset Capable field is not set.

2.2.5. TD_1_40 Device Capabilities 2, Device Control 2, and Device Status 2 Registers (PCIe Cap Ver = 2)

The test verifies that the function under test implements the PCI Express Device Capabilities 2, Device Control 2 and Device Status 2 registers as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *ECN PCI Express Capability Structure Expansion (to Base 1.1)*
- *ECN Completion Timeout Control Capability (to Base 1.1)*
- *ECN Alternate Routing-ID Interpretation (to Base 2.0 and Base 1.1)*
- *ECN Atomic Operations (to Base 2.0)*

- *ECN ID-Based Ordering (to Base 2.0)*
- *ECN Latency Tolerance Reporting (to Base 2.0)*
- *ECN TLP Prefix (to Base 2.0)*
- *ECN TLP Processing Hints (to Base 2.0)*
- *ECN Optimized Buffer Flush/Fill (to Base 2.0 and Base 2.1)*
- *Single Root I/O Virtualization and Sharing Specification (Base 3.x or earlier only)*
- *ECN Lightweight Notification (LN) Protocol (to Base 3.0)*
- *ECN Readiness Notifications (RN) (to Base 3.0)*
- *ECN Emergency Power Reduction mechanism with PWRBRK signal (to Base 3.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Capability ID field for each of the function's Capability structures. Determine how many instances of the Capability ID of 10h (PCI Express Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Capability ID of 10h is not found in a Capability structure, the test terminates with a failure.
4. If the Capability ID of 10h is found in a Capability structure, read a WORD located at offset 02h in the PCI Express Capability structure and if the Capability Version field is equal or less than 1h, the test terminates. (For Base 2.x or later testing, this is a failure. For Base 1.x testing this is not a failure and the test result is reported as skipped.)
5. If the Capability ID of 10h is found in a Capability structure and if the Capability Version field is equal or greater than 2h, the following tests are performed on that Capability structure:
6. Read a DWORD located at offset 24h (Device Capabilities 2 register) in the PCI Express Capability structure.
7. Perform each of the following checks on the fields of the DWORD read:
 a. The Completion Timeout Ranges Supported field must be a valid value (0000b, 0001b, 0010b, 0011b, 0110b, 0111b, 1110b, or 1111b). All other encodings are reserved and are recorded as a failure, but the test continues.

b. For Base 2.x or later testing: if the device type is a Root Port, if the 32-bit AtomicOp Completer Supported field returns 1, then the 64-bit AtomicOp Completer Supported field must return 1. If not, this is recorded as a failure, but the test continues.
c. For Base 2.x or later testing: if the device type is a Root Port, if the 64-bit AtomicOp Completer Supported field returns 1, then the 32-bit AtomicOp Completer Supported field must return 1. If not, this is recorded as a failure, but the test continues.
d. For Base 2.x or later testing: if the device type is a Root Port, if the 128-bit CAS Completer Supported field returns 1, then both the 32-bit AtomicOp Completer Supported field and the 64-bit AtomicOp Completer Supported field must return 1. If not, this is recorded as a failure, but the test continues.
e. For Base 3.x or later testing: if the device type is a Root Port, then the LN System CLS field must be a valid value (00b, 01b, 10b). All other encodings are reserved and are recorded as a failure, but the test continues.
f. For Base 2.x or later testing: if the End-End TLP Prefix Supported field returns 1, then the Extended Fmt Field Supported field must return 1. If not, this is recorded as a failure, but the test continues.
g. For Base 3.x or later testing: the Extended Fmt Field Supported field should return 1. If it does not, a warning message is issued, but this is not treated in itself as a failure.
h. For Base 4.x or later testing: if the Device/Port Type field (PCI Express Capabilities register) is 0111b (PCI Express to PCI/PCI-X Bridge) or 1000b (PCI/PCI-X to PCI Express Bridge), then the 10-Bit Tag Completer Supported field must return 0. If not, this is recorded as a failure, but the test continues.
i. For Base 4.x or later testing, and the Max Link Speed/Supported Link Speeds field is 0100b or greater: if the Device/Port Type field (PCI Express Capabilities register) is not 0111b (PCI Express to PCI/PCI-X Bridge) and not 1000b (PCI/PCI-X to PCI Express Bridge), then the 10-Bit Tag Completer Supported field must return 1. If not, this is recorded as a failure, but the test continues.
j. For Base 4.x or later testing: if Device/Port Type field (PCI Express Capabilities register) is not 0111b (PCI Express to PCI/PCI-X Bridge) and not 1000b (PCI/PCI-X to PCI Express Bridge), then the 10-Bit Tag Completer Supported field should return 1. If it does not, a warning message is issued, but this is not treated in itself as a failure.
k. For Base 4.x or later testing: if the 10-Bit Tag Completer Supported field returns 0, then the 10-Bit Tag Requester Supported field must return 0. If not, this is recorded as a failure, but the test continues.

8. The following register field characteristic checks are performed:

Device Capabilities 2 Register (Offset 24h) — DWORD

a. Completion Timeout Ranges Supported

(for Switch Ports, RC Event Collectors, or PCI/PCI-X to PCI Express Bridges)	RO-Zero
(otherwise)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO

b. Completion Timeout Disable Supported

(for Switch Ports, RC Event Collectors, or PCI/PCI-X to PCI Express Bridges)	RO-Zero
(otherwise)	RO

c. ARI Forwarding Supported
(for Switch Downstream Ports or Root Ports) RO
(otherwise) RO-Zero
d. AtomicOp Routing Supported
(For Base 2.x or later testing)
(for Switch Upstream Ports, Switch Downstream Ports, or Root Ports) RO
(otherwise) RO-Zero
e. 32-bit AtomicOp Completer Supported
(For Base 2.x or later testing)
(for Endpoints, Switch Ports, or Root Ports) RO
(otherwise) RO-Zero
f. 64-bit AtomicOp Completer Supported
(For Base 2.x or later testing)
(for Endpoints, Switch Ports, or Root Ports) RO
(otherwise) RO-Zero
g. 128-bit CAS Completer Supported
(For Base 2.x or later testing)
(for Endpoints, Switch Ports, or Root Ports) RO
(otherwise) RO-Zero
h. No RO-enabled PR-PR Passing
(For Base 2.x or later testing)
(for all except for Switch Ports and Root Ports) RO-Zero
(for Switch Ports or Root Ports) HwInit
i. LTR Mechanism Supported
(For Base 2.x or later testing)
(for PCI Express to PCI/PCI-X Bridges
or PCI/PCI-X to PCI Express Bridges) RO-Zero
(otherwise) RO
j. TPH Completer Supported
(For Base 2.x or later testing)
(for Endpoints or Root Ports) RO
(otherwise) RO-Zero
k. RsvdP_17-14
(For Base 2.x testing) RO-Zero
l. LN System CLS
(For Base 3.x or later testing)
(for Root Ports) HwInit
(otherwise) RO-Zero
m. 10-Bit Tag Completer Supported
(For Base 4.x or later testing)
(for non-FLR testing) HwInit
(for FLR testing) RO
n. 10-Bit Tag Requester Supported
(For Base 4.x or later testing)
(for non-FLR testing) HwInit
(for FLR testing) RO
o. RsvdP_17-16
(For Base 3.x or earlier testing) RO-Zero

p. OBFF Supported
(For Base 2.x or later testing)
(for all except for Root Ports, Switch Ports, and Endpoints) RO-Zero
(for Root Ports, Switch Ports, or Endpoints)
(for non-FLR testing) HwInit
(for FLR testing) RO

q. Extended Fmt Field Supported
(For Base 2.x or later testing) RO

r. End-End TLP Prefix Supported
(For Base 2.x or later testing)
(for non-FLR testing) HwInit
(for FLR testing) RO

s. Max End-End TLP Prefixes
(For Base 2.x or later testing)
(for Switch Ports) RO-Zero
(for non-Switch Ports with End-End TLP Prefix Supported as 0) RO-Zero
(for Root Ports with End-End TLP Prefix Supported as 1) HwInit
(for non-Switch Ports and non-Root Ports,
with End-End TLP Prefix Supported as 1) RO

t. Emergency Power Reduction Supported
(For Base 3.1 or later testing)
(for RC Integrated Endpoints, RC Event Collectors, or Downstream Ports) RO-Zero
(for Upstream Ports, for non-FLR testing) HwInit
(for Upstream Ports, for FLR testing) RO

u. Emergency Power Reduction Initialization Required
(For Base 3.1 or later testing)
(for RC Integrated Endpoints, RC Event Collectors, or Downstream Ports) RO-Zero
(for Upstream Ports, for non-FLR testing) HwInit
(for Upstream Ports, for FLR testing) RO

v. RsvdP_30-27
(For Base 3.1 or later testing) RO-Zero

w. RsvdP_30-24
(For Base 3.0 testing) RO-Zero

x. FRS Supported
(For Base 3.x or later testing)
(for non-FLR testing) HwInit
(for FLR testing) RO

y. RsvdP_31-24
(For Base 2.x testing) RO-Zero

z. RsvdP_31-6
(For Base 1.x testing) RO-Zero

Device Control 2 Register (Offset 28h) –– WORD

a. Completion Timeout Value
(for VFs, Switch Ports, RC Event Collectors,
or PCI/PCI-X to PCI Express Bridges) RO-Zero
(for Root Ports, Endpoints excluding VFs,

or PCI Express to PCI/PCI-X Bridges)	RO-Zero or RW
b. Completion Timeout Disable	
(for VFs, Switch Ports, RC Event Collectors,	
or PCI/PCI-X to PCI Express Bridges)	RO-Zero
(for Root Ports, Endpoints excluding VFs,	
or PCI Express to PCI/PCI-X Bridges)	RO-Zero or RW
c. ARI Forwarding Enable	
(for Switch Downstream Ports with ARI Forwarding Supported as 1,	
or Root Ports with ARI Forwarding Supported as 1)	RW
(otherwise)	RO-Zero
d. AtomicOp Requester Enable	
(For Base 2.x or later testing)	
(for Endpoints excluding VFs or Root Ports)	RW or RO-Zero
(otherwise)	RO-Zero
e. AtomicOp Egress Blocking	
(For Base 2.x or later testing)	
(for Switch Ports with AtomicOp Routing Supported as 1,	
or Root Ports with AtomicOp Routing Supported as 1)	RW
(otherwise)	RO-Zero
f. IDO Request Enable	
(For Base 2.x or later testing)	
(for Endpoints excluding VFs or Root Ports)	RW or RO-Zero
(otherwise)	RO-Zero
g. IDO Completion Enable	
(For Base 2.x or later testing)	
(for Endpoints excluding VFs or Root Ports)	RW or RO-Zero
(otherwise)	RO-Zero
h. LTR Mechanism Enable	
(For Base 2.x or later testing)	
(for PCI Express to PCI/PCI-X Bridges	
or PCI/PCI-X to PCI Express Bridges)	RO-Zero
(for Endpoints in single function device	
with LTR Mechanism Supported as 1)	RW
(for Endpoints in multi-function device that is function 0	
with LTR Mechanism Supported as 1)	RW
(for Endpoints in multi-function device that is not function 0)	RO-Zero
(for Endpoints in single function device	
with LTR Mechanism Supported as 0)	RW or RO-Zero
(for Endpoints in multi-function device that is function 0	
with LTR Mechanism Supported as 0)	RW or RO-Zero
(for Root Ports or Switch Ports with LTR Mechanism Supported as 1)	RW

(for Root Ports or Switch Ports with LTR Mechanism Supported as 0) RW or RO-Zero

i. Emergency Power Reduction Request
(For Base 3.1 or later testing)
(for VFs) RO-Zero
(for RC Integrated Endpoints, RC Event Collectors, or Downstream Ports) RO-Zero
(for Upstream Ports)
(for lowest numbered function in the device,
with Emergency Power Reduction Supported not 00b) RW
(otherwise) RO-Zero

j. 10-Bit Tag Requester Enable
(For Base 4.x or later testing)
(for VFs) RO-Zero
(for non-VFs)
(with 10-Bit Tag Requester Supported as 1) RW
(with 10-Bit Tag Requester Supported as 0) RW or RO-Zero

k. RsvdP_12
(For Base 3.1 testing) RO-Zero

l. RsvdP_12-11
(For Base 3.0 or Base 2.x testing) RO-Zero

m. OBFF Enable
(For Base 2.x or later testing)
(for Root Ports, Switch Downstream Ports, and RC Integrated Endpoints
with OBFF Supported as non-zero) RW
(for Switch Upstream Ports and Endpoints in single function device
with OBFF Supported as non-zero) RW
(for Switch Upstream Ports and Endpoints in multi-function device
with OBFF Supported as non-zero
that is function 0) RW
(for Switch Upstream Ports and Endpoints in multi-function device
with OBFF Supported as non-zero that is not function 0) RO-Zero
(otherwise) RW or RO-Zero

n. End-End TLP Prefix Blocking
(For Base 2.x or later testing)
(for Switch Ports with End-End TLP Prefix Supported as 1) RW
(for Root Ports with End-End TLP Prefix Supported as 1) RW or RO-Ones
(otherwise) RO-Zero

o. RsvdP_15-6
(For Base 1.x testing: bits 15-6) RO-Zero

Device Status 2 Register (Offset 2Ah) — WORD

a. RsvdZ_15-0 RO-Zero

9. The following default value checks are performed:

Device Control 2 Register Default Value (Offset 28h) — WORD

a. Completion Timeout Value	0000b
b. Completion Timeout Disable	0
c. ARI Forwarding Enable	0
d. AtomicOp Requester Enable (For Base 2.x or later testing)	0
e. AtomicOp Egress Blocking (For Base 2.x or later testing)	0
f. IDO Request Enable (For Base 2.x or later testing)	0
g. IDO Completion Enable (For Base 2.x or later testing)	0
h. LTR Mechanism Enable (For Base 2.x or later testing)	0
i. Emergency Power Reduction Request (For Base 3.1 or later testing)	0
j. 10-Bit Tag Requester Enable (For Base 4.x or later testing)	0
k. OBFF Enable (For Base 2.x or later testing)	00b
l. End-End TLP Prefix Blocking (For Base 2.x or later testing) (for non-Root Ports)	0

10. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- ❑ A PCI Express Capability structure is not present.
- ❑ More than one PCI Express Capability structure is present.
- ❑ A reserved value is read from the Completion Timeout Ranges Supported field.
- ❑ A Root Port reports the 32-bit AtomicOp Completer Supported field as 1, but the 64-bit AtomicOp Completer Supported field as 0 (for Base 2.x or later testing only).
- ❑ A Root Port reports the 64-bit AtomicOp Completer Supported field as 1, but the 32-bit AtomicOp Completer Supported as 0 (for Base 2.x or later testing only).
- ❑ A Root Port reports the 128-bit CAS Completer Supported field as 1, but either or both the 32-bit AtomicOp Completer Supported field as 0 or the 64-bit AtomicOp Completer Supported field as 0 (for Base 2.x or later testing only).
- ❑ A Root Port reports a reserved value in the LN System CLS field (for Base 3.x or later testing only).

- The End-End TLP Prefix Supported field reports 1, but the Extended Fmt Field Supported field reports 0 (for Base 2.x or later testing only).
- For devices which are either PCI/PCI-X to PCI Express Bridge or PCI Express to PCI/PCI-X Bridge, the 10-Bit Tag Completer Supported field reports 1 (for Base 4.x or later testing only).
- For devices other than PCI/PCI-X to PCI Express Bridge and PCI Express to PCI/PCI-X Bridge, in a port supporting 16.0 GT/s or higher, the 10-Bit Tag Completer Supported field reports 0 (for Base 4.x or later testing only).
- The 10-Bit Tag Completer Supported field reports 0, but the 10-Bit Tag Requester Supported reports 1 (for Base 4.x or later testing only).
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

The test *warns* if:

- The Extended Fmt Field Supported field reports 0 (for Base 3.x or later testing only).
- For devices other than PCI/PCI-X to PCI Express Bridge and PCI Express to PCI/PCI-X Bridge, the 10-Bit Tag Completer Supported field reports 0 (for Base 4.x or later testing only).

2.2.6. TD_1_5 Link Capabilities, Link Control, and Link Status Registers

The test verifies that the function under test implements the PCI Express Link Capabilities, Link Control, and Link Status registers as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *ECN Link Bandwidth Notification (to Base 1.1)*
- *ECN ASPM Optionality (to Base 2.1)*
- *Single Root I/O Virtualization and Sharing Specification (Base 3.x or earlier only)*
- *ECN Downstream Port Containment (DPC) (to Base 3.0)*
- *M-PCIe ECN (to Base 3.0)*
- *ECN Readiness Notifications (RN) (to Base 3.0)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Capability ID field for each of the function's Capability structures. Determine how many instances of the Capability ID of 10h (PCI Express Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Capability ID of 10h is not found in a Capability structure, the test terminates with a failure.
4. If the Capability ID of 10h is found in a Capability structure, the following tests are performed on that Capability structure:
5. Read a DWORD located at offset 0Ch (Link Capabilities register) in the PCI Express Capability structure.
6. If the device is neither a Root Complex Integrated Endpoint nor a Root Complex Event Collector, perform each of the following checks on the fields of the DWORD read:
 a. For Base 1.x testing: the Max Link Speed/Supported Link Speeds field must be 0001b. All other encodings are reserved and are recorded as a failure, but the test continues.
 b. For Base 2.x testing: the Max Link Speed/Supported Link Speeds field must be 0001b or 0010b. All other encodings are reserved and are recorded as a failure, but the test continues.
 c. For Base 3.x testing: the Max Link Speed/Supported Link Speeds field must be 0001b, 0010b, or 0011b. All other encodings are reserved and are recorded as a failure, but the test continues.
 d. For Base 4.x testing: the Max Link Speed/Supported Link Speeds field must be 0001b, 0010b, 0011b, or 0100b. All other encodings are reserved and are recorded as a failure, but the test continues.
 e. The Maximum Link Width field must be 00 0001b, 00 0010b, 00 0100b, 00 1000b, 00 1100b, 01 0000b, or 10 0000b. All other encodings are reserved and are recorded as a failure, but the test continues.
 f. If the ASPM Optionality Compliance field is 0, then the Active State Power Management (ASPM) Support field must be 01b or 11b. All other encodings are reserved and are recorded as a failure, but the test continues.
 g. For Base 3.x or later testing: the ASPM Optionality Compliance field must be 1. If not, this is recorded as a failure, but the test continues.
 h. For Base 3.x or later testing, if the ASPM Optionality Compliance field returns 1, the following tests are performed:
 i. If the Active State Power Management (ASPM) Support field returns 00b or 10b, then the L0s Exit Latency field should return 111b. If it does not a warning message is issued, but this is not treated in itself as a failure.
 i. The Port Number field must return:
 i. For Switch Downstream Ports: all downstream ports in a Switch must have unique Port Numbers. If not, this is recorded as a failure, but the test continues.
7. For Downstream Ports with a DPC Extended Capability, the Data Link Layer Link Active Reporting Capable field must report 1. If not, this is recorded as a failure, but the test continues.
8. For Downstream Ports that have the Max Link Speed/Supported Link Speeds field return 0010b or greater, or that have the Hot-Plug Capable field return 1, the Data Link Layer Link

Active Reporting Capable field must report 1. If not, this is recorded as a failure, but the test continues.

9. For Downstream Ports that have the Max Link Speed/Supported Link Speeds field return 0010b or greater, or that have the Maximum Link Width field return greater than 000 0001b, the Link Bandwidth Notification Capability field must report 1. If not, this is recorded as a failure, but the test continues.
10. Read a WORD located at offset 10h (Link Control register).
11. If the device is not a Root Complex Integrated Endpoint, not a Root Complex Event Collector, and not a VF, the Active State Power Management (ASPM) Control field may return 00b, 01b, 10b, or 11b. Test software writes each of the allowed data values to this field (00b, 01b, 10b, and 11b) and makes sure that the same value is read back. If not, this is recorded as a failure, but the test continues.
12. Read a WORD from offset 12h (Link Status register).
13. If the device is not a Root Complex Integrated Endpoint, not a Root Complex Event Collector, and not a VF, perform each of the following checks on the fields of the WORD read:
 a. For Base 1.x testing: the Current Link Speed field must be 0001b for 2.5 GT/s test cases. All other encodings are reserved and are recorded as a failure, but the test continues.
 b. For Base 2.x testing: the Current Link Speed field must be 0001b for 2.5 GT/s test cases and must be 0010b for 5.0 GT/s test cases. All other encodings are reserved and are recorded as a failure, but the test continues.
 c. For Base 3.x testing: the Current Link Speed field must be 0001b for 2.5 GT/s test cases, must be 0010b for 5.0 GT/s test cases, and must be 0011b for 8.0 GT/s test cases. All other encodings are reserved and are recorded as a failure, but the test continues.
 d. For Base 4.x testing: the Current Link Speed field must be 0001b for 2.5 GT/s test cases, must be 0010b for 5.0 GT/s test cases, must be 0011b for 8.0 GT/s test cases, and must be 0100b for 16.0 GT/s test cases. All other encodings are reserved and are recorded as a failure, but the test continues.
 e. The Current Link Speed field must be equal or less than the Max Link Speed/Supported Link Speeds field value. If not, this is recorded as a failure, but the test continues.
 f. The Negotiated Link Width field must be 00 0001b, 00 0010b, 00 0100b, 00 1000b, 00 1100b, 01 0000b, or 10 0000b. All other encodings are reserved and are recorded as a failure, but the test continues.
 g. The Negotiated Link Width field must be equal or less than the Maximum Link Width field value.
 h. For downstream ports, the Link Training field must be 0. If not, this is recorded as a failure, but the test continues.
 i. For downstream ports with the Data Link Layer Link Active Reporting Capable field value as 1, the Data Link Layer Link Active field must be 1. If not, this is recorded as a failure, but the test continues.
14. The following register field characteristic checks are performed:

 Link Capabilities Register (Offset 0Ch) — DWORD
 (for all except for RC Integrated Endpoint and RC Event Collector)
 a. Max Link Speed/Supported Link Speeds RO
 b. Maximum Link Width RO

c. Active State Power Management (ASPM) Support	RO
d. L0s Exit Latency	RO
e. L1 Exit Latency	RO
f. Clock Power Management	
(for Upstream Ports)	RO
(for Downstream Ports)	RO-Zero
g. Surprise Down Error Reporting Capable	
(for Downstream Ports)	RO
(for Upstream Ports)	RO-Zero
h. Data Link Layer Link Active Reporting Capable	
(for Downstream Ports)	RO
(for Upstream Ports)	RO-Zero
i. Link Bandwidth Notification Capability	
(for Downstream Ports)	RO
(for Upstream Ports)	RO-Zero
j. ASPM Optionality Compliance	
(For Base 2.x or later testing)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO-Ones
k. RsvdP_23	
(For Base 2.x or later testing)	RO-Zero
l. RsvdP_23-22	
(For Base 1.x testing)	RO-Zero
m. Port Number	
(for non-FLR testing)	HwInit
(for FLR testing)	RO

Link Capabilities Register (Offset 0Ch) — DWORD

(for RC Integrated Endpoint and RC Event Collector)	
a. RsvdP_31-0	RO-Zero

Link Control Register (Offset 10h) — WORD

(for all except for RC Integrated Endpoint and RC Event Collector)	
a. Active State Power Management (ASPM) Control	
(for VFs)	RO-Zero
(for non-VFs)	
(for non-FLR testing)	RW
(for FLR testing)	RWS
b. RsvdP_2	RO-Zero
c. Read Completion Boundary (RCB)	
(for VFs)	RO-Zero
(for Root Ports)	RO
(for Endpoints excluding VFs, PCI Express to PCI/PCI-X Bridges, or PCI/PCI-X to PCI Express Bridges)	
(for non-FLR testing)	RW or RO-Zero
(for FLR testing)	RWS or RO-Zero
(for Switch Ports)	RO-Zero

d. Link Disable
 (for Downstream Ports) RW
 (for Upstream Ports) RO-Zero
 Note: Writing Link Disable with 1 in a Downstream Port causes the link to go down. The test should restore this field to 0 when completing testing of this register.
e. Retrain Link
 (for Downstream Ports) RO-Zero
 (for Upstream Ports) RO-Zero
f. Common Clock Configuration
 (for VFs) RO-Zero
 (for non-VFs)
 (for non-FLR testing) RW
 (for FLR testing) RWS
g. Extended Synch
 (for VFs) RO-Zero
 (for non-VFs with M-PCIe Extended Capability)
 (for non-FLR testing) RW or RO-Zero
 (for FLR testing) RWS or RO-Zero
 (for non-VFs without M-PCIe Extended Capability)
 (for non-FLR testing) RW
 (for FLR testing) RWS
h. Enable Clock Power Management
 (for Downstream Ports) RO-Zero
 (for Upstream Ports excluding VFs, with Clock Power Management as 1)
 (for non-FLR testing) RW
 (for FLR testing) RWS
 (for Upstream Ports with Clock Power Management as 0, or VFs) RO-Zero
i. Hardware Autonomous Width Disable
 (for Upstream Ports whose function number is non-zero, or VFs) RO-Zero
 (otherwise)
 (for non-FLR testing) RW or RO-Zero
 (for FLR testing) RWS or RO-Zero
j. Link Bandwidth Management Interrupt Enable
 (for Downstream Ports with Link Bandwidth Notification Capability as 1) RW
 (for Downstream Ports with Link Bandwidth Notification Capability as 0) RO-Zero
 (for Upstream Ports) RO-Zero
k. Link Autonomous Bandwidth Interrupt Enable
 (for Downstream Ports with Link Bandwidth Notification Capability as 1) RW
 (for Downstream Ports with Link Bandwidth Notification Capability as 0) RO-Zero
 (for Upstream Ports) RO-Zero
l. RsvdP_15-12
 (For Base 2.x or earlier testing) RO-Zero
m. RsvdP_13-12
 (For Base 3.x or later testing) RO-Zero

n. DRS Signaling Control
(For Base 3.x or later testing)
(for Downstream Ports with DRS Supported as 1) RW
(for Downstream Ports with DRS Supported as 0) RO-Zero
(for Upstream Ports) RO-Zero

Link Control Register (Offset 10h) — WORD
(for RC Integrated Endpoint and RC Event Collector)
a. RsvdP_15-0 RO-Zero

Link Status Register (Offset 12h) — WORD
(for all except for RC Integrated Endpoint and RC Event Collector and VF)
a. Current Link Speed RO
b. Negotiated Link Width RO
c. Undefined_10 RO
Note: This was once Link Training Error.
d. Link Training
(for Downstream Ports) RO
(for Upstream Ports) RO-Zero
e. Slot Clock Configuration
(for non-FLR testing) HwInit
(for FLR testing) RO
f. Data Link Layer Link Active
(for Downstream Ports with Data Link Active Reporting Capable as 1) RO
(for Downstream Ports with Data Link Active Reporting Capable as 0) RO-Zero
(for Upstream Ports) RO-Zero
g. Link Bandwidth Management Status
(for Downstream Ports with Link Bandwidth Notification Capability as 1) RW1C
(for Downstream Ports with Link Bandwidth Notification Capability as 0) RO-Zero
(for Upstream Ports) RO-Zero
h. Link Autonomous Bandwidth Status
(for Downstream Ports with Link Bandwidth Notification Capability as 1) RW1C
(for Downstream Ports with Link Bandwidth Notification Capability as 0) RO-Zero
(for Upstream Ports) RO-Zero

Link Status Register (Offset 12h) — WORD
(for RC Integrated Endpoint and RC Event Collector and VF)
a. RsvdZ_15-0 RO-Zero

15. The following default value checks are performed:

Link Capabilities Register Default Value (Offset 0Ch) — WORD
a. ASPM Optionality Compliance
(For Base 2.x or later testing) 1

Link Control Register Default Value (Offset 10h) — WORD
(for all except for RC Integrated Endpoint and RC Event Collector)
a. Read Completion Boundary (RCB)
(for Endpoints, PCI Express to PCI/PCI-X Bridges,
or PCI/PCI-X to PCI Express Bridges) 0
b. Link Disable

(for Downstream Ports) 0
c. Common Clock Configuration 0
d. Extended Synch 0
e. Enable Clock Power Management
(for Upstream Ports) 0
f. Hardware Autonomous Width Disable 0
g. Link Bandwidth Management Interrupt Enable
(for Downstream Ports) 0
h. Link Autonomous Bandwidth Interrupt Enable
(for Downstream Ports) 0
i. DRS Signaling Control
(For Base 3.x or later testing)
(for Downstream Ports) 00b

16. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- ❑ A PCI Express Capability structure is not present.
- ❑ More than one PCI Express Capability structure is present.
- ❑ The Max Link Speed/Supported Link Speeds field has an invalid value.
- ❑ The Maximum Link Width field has an invalid value.
- ❑ The ASPM Optionality Compliance field is 0 and the Active State Power Management (ASPM) Support field is not 01b or 11b.
- ❑ The ASPM Optionality Compliance field is 0 (for Base 3.x or later testing only).
- ❑ For a Switch, all downstream ports do not each have a unique value in the Port Number field
- ❑ For Downstream Ports, that support DPC, the Data Link Layer Link Active Reporting Capable field is 0.
- ❑ For Downstream Ports, that support greater than 5.0 GT/s or that support Hot-Plug, the Data Link Layer Link Active Reporting Capable field is 0.
- ❑ For Downstream Ports, that support greater than 2.5 GT/s or greater than x1, the Link Bandwidth Notification Capability field is 0.
- ❑ The Active State Power Management (ASPM) Control field does not accept writing all values (00b, 01b, 10b, 11b).
- ❑ The Current Link Speed field is not one of the defined values.
- ❑ The Current Link Speed field is not correct for the level of testing
- ❑ The Current Link Speed field is not equal or less than the reported Max Link Speed/Supported Link Speed field.

- The Negotiated Link Width field is not one of the defined values.
- The Negotiated Link Width field is not equal or less than the reported Maximum Link Width field.
- For a downstream port, the Link Training field is not 0.
- For a downstream port that supports Data Link Layer Link Active reporting, the Data Link Layer Active field is not 1.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

The test *warns* if:

- When the ASPM Optionality Compliance field returns 1 (for Base 3.x or later testing only) and the Active State Power Management (ASPM) Support field returns 00b or 10b (meaning L0s is not supported), the L0s Exit Latency field returns any value other than 111b.

2.2.7. TD_1_41 Link Capabilities 2, Link Control 2, and Link Status 2 Registers (PCIe Cap Ver = 2)

The test verifies that the function under test implements PCI Express Link Capabilities 2, Link Control 2, and Link Status 2 registers as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *ECN PCI Express Capability Structure Expansion (to Base 1.1)*
- *Single Root I/O Virtualization and Sharing Specification (Base 3.x or earlier only)*
- *ECN Separate Refclk Independent SSC Architecture (SRIS) (to Base 3.0)*
- *M-PCIe ECN (to Base 3.0)*
- *ECN Readiness Notifications (RN) (to Base 3.0)*
- *ECN Extension Devices (to Base 3.0)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.

2. Examine the Capability ID field for each of the function's Capability structures. Determine how many instances of the Capability ID of 10h (PCI Express Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Capability ID of 10h is not found in a Capability structure, the test terminates with a failure.
4. If the Capability ID of 10h is found in a Capability structure, read a WORD located at offset 02h in the PCI Express Capability structure and if the Capability Version field is equal or less than 1h, the test terminates. (For Base 2.x or later testing, this is a failure. For Base 1.x testing, this is not a failure and the test result is reported as skipped.)
5. If the Capability ID of 10h is found in a Capability structure and if the Capability Version field is equal or greater than 2h, the following tests are performed on that Capability structure:
6. For Base 3.x or later testing: read a DWORD located at offset 2Ch (Link Capabilities 2 register).
7. If the device is neither a Root Complex Integrated Endpoint nor a Root Complex Event Collector, perform each of the following checks on the fields of the DWORD read:
 a. For Base 3.x testing: the Supported Link Speeds Vector field must be 000 0000b, 000 0001b, 000 0010b, 000 0011b, 000 0100b, 000 0101b, 000 0110b, or 000 0111b. All other encodings are reserved and are recorded as a failure, but the test continues.
 b. For Base 4.x testing: the Supported Link Speeds Vector field must be 000 0000b, 000 0001b, 000 0010b, 000 0011b, 000 0100b, 000 0101b, 000 0110b, 000 0111b, 000 1000b, 000 1001b, 000 1010b, 000 1011b, 000 1100b, 000 1101b, 000 1110b, or 000 1111b. All other encodings are reserved and are recorded as a failure, but the test continues.
 c. For Base 3.x testing: for the Supported Link Speeds Vector field, determine the most significant bit value that is set to 1 and record it in Most Significant Bit [MSB]. All bits from [MSB] to 0 must also be 1. If not, this is recorded as a failure, but the test continues.
 d. For Base 3.x testing: the Lower SKP OS Generation Supported Speeds Vector field must be 000 0000b, 000 0001b, 000 0010b, 000 0011b, 000 0100b, 000 0101b, 000 0110b, or 000 0111b. All other encodings are reserved and are recorded as a failure, but the test continues.
 e. For Base 4.x testing: the Lower SKP OS Generation Supported Speeds Vector field must be 000 0000b, 000 0001b, 000 0010b, 000 0011b, 000 0100b, 000 0101b, 000 0110b, 000 0111b, 000 1000b, 000 1001b, 000 1010b, 000 1011b, 000 1100b, 000 1101b, 000 1110b, or 000 1111b. All other encodings are reserved and are recorded as a failure, but the test continues.
 f. For Base 3.x testing: the Lower SKP OS Reception Supported Speeds Vector field must be 000 0000b, 000 0001b, 000 0010b, 000 0011b, 000 0100b, 000 0101b, 000 0110b, or 000 0111b. All other encodings are reserved and are recorded as a failure, but the test continues.
 g. For Base 4.x testing: the Lower SKP OS Reception Supported Speeds Vector field must be 000 0000b, 000 0001b, 000 0010b, 000 0011b, 000 0100b, 000 0101b, 000 0110b, 000 0111b, 000 1000b, 000 1001b, 000 1010b, 000 1011b, 000 1100b, 000 1101b, 000 1110b, or 000 1111b. All other encodings are reserved and are recorded as a failure, but the test continues.
 h. For Base 4.x or later, and the Max Link Speed/Supported Link Speeds field is 0100b or greater: the Retimer Presence Detect Supported field must be 1. If not, this is recorded as a failure, but the test continues.
 i. For Base 4.x or later, and the Max Link Speed/Supported Link Speeds field is 0100b or greater: the Two Retimers Presence Detect Supported field must be 1. If not, this is recorded as a failure, but the test continues.

j. For Base 4.x or later: if the Retimer Presence Detect Supported field returns 0, then the Two Retimers Presence Detect Supported field must be 0. If not, this is recorded as a failure, but the test continues.
k. For Base 3.x or later testing: for Downstream Ports that report the FRS Supported field as 1, the DRS Supported field must be 1. If not, this is recorded as a failure, but the test continues.

8. For Base 2.x or later testing: read a WORD located at offset 30h (Link Control 2 register).
9. If the device is neither a Root Complex Integrated Endpoint nor a Root Complex Event Collector, perform each of the following checks on the fields of the WORD read:
 a. For Base 2.x or later, if the function under test is associated with an Upstream Port and is not function 0, then the Target Link Speed field must be 0000b. If not, this is recorded as a failure, but the test continues.
 b. If the function under test is associated with an Upstream Port and is function 0, or if the function under test is associated with a Downstream Port then:
 i. For Base 2.x or later, and the Max Link Speed/Supported Link Speeds field is less than 0010b: the Target Link Speed field must be 0000b or 0001b. All other encodings are reserved and are recorded as a failure, but the test continues.
 ii. For Base 2.x or later, and the Max Link Speed/Supported Link Speeds field is 0010b: the Target Link Speed field must be 0001b or 0010b. All other encodings are reserved and are recorded as a failure, but the test continues.
 iii. For Base 3.x or later, and the Max Link Speed/Supported Link Speeds field is 0011b: the Target Link Speed field must be 0001b, 0010b, or 0011b. All other encodings are reserved and are recorded as a failure, but the test continues.
 iv. For Base 4.x or later, and the Max Link Speed/Supported Link Speeds field is 0100b: the Target Link Speed field must be 0001b, 0010b, 0011b, or 0100b. All other encodings are reserved and are recorded as a failure, but the test continues.
10. For Base 2.x or later testing: read a WORD located at offset 32h (Link Status 2 register).
11. If the device type is not a Root Complex Integrated Endpoint, not a Root Complex Event Collector, and not a VF, perform each of the following checks on the fields of the WORD read:
 a. For Base 2.x or later testing: the Current De-emphasis Level field must reflect the expected level when the function under test's link is operating at 5.0 GT/s. If not, this is recorded as a failure, but the test continues. The expected level is determined by the system specific settings for the system used to perform the test. When the function under test's link is not operating at 5.0 GT/s, or the function under test has no link, this value is not checked.
 b. For Base 4.x or later, and the Max Link Speed/Supported Link Speeds field is 0100b, and Crosslink Supported field is 1: the Crosslink Resolution field must not be 00b. If it is this is recorded as a failure, but the test continues.
 c. For Base 4.x or later, and the Max Link Speed/Supported Link Speeds field is 0100b, and Crosslink Supported field is 0: the Crosslink Resolution field must not be 11b. If it is this is recorded as a failure, but the test continues.
12. The following register field characteristic checks are performed:

Link Capabilities 2 Register (Offset 2Ch) — DWORD

(for all except for RC Integrated Endpoint and RC Event Collector)

a. RsvdP_0
 (For Base 3.x or later testing) RO-Zero

b. Supported Link Speeds Vector
(For Base 3.x or later testing) RO
c. Crosslink Supported
(For Base 3.x or later testing) RO
d. Lower SKP OS Generation Supported Speeds Vector
(For Base 3.x or later testing)
(for non-FLR testing) HwInit
(for FLR testing) RO
e. Lower SKP OS Reception Supported Speeds Vector
(For Base 3.x or later testing)
(for non-FLR testing) HwInit
(for FLR testing) RO
f. Retimer Presence Detect Supported
(For Base 4.x or later testing)
(for non-FLR testing) HwInit
(for FLR testing) RO
(For Base 3.x testing)
(for Downstream Ports) HwInit
(for Upstream Ports) RO-Zero
g. Two Retimers Presence Detect Supported
(For Base 4.x or later testing)
(for non-FLR testing) HwInit
(for FLR testing) RO
h. RsvdP_30-25
(For Base 4.x or later testing) RO-Zero
i. RsvdP_30-24
(For Base 3.x testing) RO-Zero
j. DRS Supported
(For Base 3.x or later testing)
(for Downstream Ports) HwInit
(for Upstream Ports whose function number is zero)
(for non-FLR testing) HwInit
(for FLR testing) RO
(for Upstream Ports whose function number is non-zero) RO-Zero
k. RsvdP_31-0
(For Base 2.x or earlier testing) RO-Zero

Link Capabilities 2 Register (Offset 2Ch) — DWORD
(for RC Integrated Endpoint and RC Event Collector)
a. RsvdP_31-0 RO-Zero

Link Control 2 Register (Offset 30h) — WORD
(for all except for RC Integrated Endpoint and RC Event Collector)
a. Target Link Speed
(For Base 2.x or later testing)
(for Upstream Ports whose function number is non-zero) RO-Zero

(otherwise)
(if Max Link Speed/Supported Link Speeds is 0001b) RWS or RO-Zero
(if Max Link Speed/Supported Link Speeds is 0010b or greater) RWS
Note: This test must only write supported values as reported in the Max Link Speed/Supported Link Speeds field.

b. Enter Compliance
(For Base 2.x or later testing)
(for Upstream Ports whose function number is non-zero) RO-Zero
(otherwise)
(if Max Link Speed/Supported Link Speeds is 0001b)
(for non-FLR testing) RW or RO-Zero
(for FLR testing) RWS or RO-Zero
(if Max Link Speed/Supported Link Speeds is 0010b or greater)
(for non-FLR testing) RW
(for FLR testing) RWS
Note: During non-FLR testing, the Enter Compliance field cannot be tested for stickiness even though its specified register field attribute is RWS because this field is reset to zero (upon exiting Polling.Compliance) during successful link training.
Note: The Enter Compliance field cannot be tested for default value, as setting it to 1 and then doing a Hot Reset (secondary bus reset) or DL_Down (link disable/enable), will cause the link to go to Compliance Pattern state and it may not return to L0 again.

c. Hardware Autonomous Speed Disable
(For Base 2.x or later testing)
(for Upstream Ports whose function number is non-zero) RO-Zero
(otherwise) RWS or RO-Zero

d. Selectable De-emphasis
(For Base 2.x or later testing)
(for Upstream Ports) RO-Zero
(for Downstream Ports) HwInit

e. Transmit Margin
(For Base 2.x or later testing)
(for Upstream Ports whose function number is non-zero) RO-Zero
(otherwise)
(any function with M-PCIe Extended Capability, or any function without M-PCIe Extended Capability and with Max Link Speed/Supported Link Speeds as 0001b)
(for non-FLR testing) RW or RO-Zero
(for FLR testing) RWS or RO-Zero
(any function without M-PCIe Extended Capability and with Max Link Speed/Supported Link Speeds as 0010b or greater)
(for non-FLR testing RW
(for FLR testing RWS

Note: During non-FLR testing, the Transmit margin field cannot be tested for stickiness for non-FLR even though its specified register field attribute is RWS because this field is reset to zero (in Polling.Configuration) during successful link training.

f. Enter Modified Compliance
(For Base 2.x or later testing)
(for Upstream Ports whose function number is non-zero) RO-Zero
(otherwise)
(any function with M-PCIe Extended Capability,
or any function without M-PCIe Extended Capability
and with Max Link Speed/Supported Link Speeds as 0001b)
RWS or
RO-Zero
(any function without M-PCIe Extended Capability
and with Max Link Speed/Supported Link Speeds as 0010b or greater)
RWS

g. Compliance SOS
(For Base 2.x or later testing)
(for Upstream Ports whose function number is non-zero) RO-Zero
(otherwise)
(any function with M-PCIe Extended Capability,
or any function without M-PCIe Extended Capability
and with Max Link Speed/Supported Link Speeds as 0001b)
RWS or
RO-Zero
(any function without M-PCIe Extended Capability
and with Max Link Speed/Supported Link Speeds as 0010b or greater)
RWS

h. Compliance Preset/De-emphasis
(For Base 3.x or later testing)
(for Upstream Ports whose function number is non-zero) RO-Zero
(otherwise)
(any function with M-PCIe Extended Capability,
or any function without M-PCIe Extended Capability
and with Max Link Speed/Supported Link Speeds as 0001b)
RWS or
RO-Zero
(any function without M-PCIe Extended Capability
and with Max Link Speed/Supported Link Speeds as 0010b or greater)
RWS

Note: For Base 3.x or later, this field consists of bits 15-12 of this register.

i. Compliance De-emphasis
(For Base 2.x testing)
(for Upstream Ports whose function number is non-zero) RO-Zero
(otherwise)
(if Max Link Speed/Supported Link Speeds is 0001b) RWS or
RO-Zero
(if Max Link Speed/Supported Link Speeds is 0010b or greater) RWS
Note: For Base 2.x, this field consists of bit 12 of this register.

j. RsvdP_15-13
(For Base 2.x testing) RO-Zero
k. RsvdP_15-0
(For Base 1.x testing) RO-Zero

Link Control 2 Register (Offset 30h) — WORD

(for RC Integrated Endpoint and RC Event Collector)
a. RsvdP_15-0 RO-Zero

Link Status 2 Register (Offset 32h) — WORD

(for all except for RC Integrated Endpoint and RC Event Collector)
a. Current De-emphasis Level
(For Base 2.x or later testing)
(for VFs) RO-Zero
(for non-VFs) RO
b. Equalization 8.0 GT/s Complete
(For Base 3.x or later testing)
(for Upstream Ports whose function number is non-zero, or VFs) RO-Zero
(otherwise)
(for non-FLR testing) RO
(for FLR testing) ROS
Note: During non-FLR testing, the Equalization 8.0 GT/s Complete field cannot be tested for stickiness even though its specified register field attribute is ROS because this field is reset to zero on link down, and is then again updated during link equalization.
c. Equalization 8.0 GT/s Phase 1 Successful
(For Base 3.x or later testing)
(for Upstream Ports whose function number is non-zero, or VFs) RO-Zero
(otherwise)
(for non-FLR testing) RO
(for FLR testing) ROS
Note: During non-FLR testing, the Equalization 8.0 GT/s Phase 1 Successful field cannot be tested for stickiness even though its specified register field attribute is ROS because this field is reset to zero on link down, and is then again updated during link equalization.
d. Equalization 8.0 GT/s Phase 2 Successful
(For Base 3.x or later testing)
(for Upstream Ports whose function number is non-zero, or VFs) RO-Zero
(otherwise)
(for non-FLR testing) RO
(for FLR testing) ROS
Note: During non-FLR testing, the Equalization 8.0 GT/s Phase 2 Successful field cannot be tested for stickiness even though its specified register field attribute is ROS because this field is reset to zero on link down, and is then again updated during link equalization.
e. Equalization 8.0 GT/s Phase 3 Successful
(For Base 3.x or later testing)
(for Upstream Ports whose function number is non-zero, or VFs) RO-Zero
(otherwise)
(for non-FLR testing) RO
(for FLR testing) ROS

Note: During non-FLR testing, the Equalization 8.0 GT/s Phase 3 Successful field cannot be tested for stickiness even though its specified register field attribute is ROS because this field is reset to zero on link down, and is then again updated during link equalization.

f. Link Equalization Request 8.0 GT/s

(For Base 3.x or later testing)	
(for Upstream Ports whose function number is non-zero, or VFs)	RO-Zero
(otherwise)	
(any function with M-PCIe Extended Capability)	
(for non-FLR testing)	RW1C or RO-Zero
(for FLR testing)	RW1CS or RO-Zero
(for any function without M-PCIe Extended Capability and Max Link Speed/Supported Link Speeds is 0011b or greater)	
(for non-FLR testing)	RW1C
(for FLR testing)	RW1CS
(for any function without M-PCIe Extended Capability and Max Link Speed/Supported Link Speeds is less than 0011b)	
(for non-FLR testing)	RW1C or RO-Zero
(for FLR testing)	RW1CS or RO-Zero

Note: During non-FLR testing, the Link Equalization Request 8.0 GT/s field cannot be tested for stickiness even though its specified register field attribute is RW1CS because this field is updated during link equalization.

g. Retimer Presence Detected

(For Base 4.x or later testing)	
(for non-FLR testing)	RO
(for FLR testing)	ROS
(For Base 3.x testing)	
(for Downstream Ports)	RO
(for Upstream Ports)	RO-Zero

Note: During non-FLR testing, the Retimer Presence Detected field cannot be tested for stickiness even though its specified register field attribute is ROS because this field is updated during link training.

h. Two Retimers Presence Detected

(For Base 4.x or later testing)	
(for non-FLR testing)	RO
(for FLR testing)	ROS

Note: During non-FLR testing, the Two Retimers Presence Detected field cannot be tested for stickiness even though its specified register field attribute is ROS because this field is updated during link training.

i. Crosslink Resolution

(For Base 4.x or later testing)	RO

j. RsvdZ_11-10

(For Base 4.x or later testing)	RO-Zero

k. RsvdZ_11-7

(For Base 3.x testing) RO-Zero

l. Downstream Component Presence
(For Base 3.x or later testing)
(for Downstream Ports with DRS Supported as 1) RO
(for Downstream Ports with DRS Supported as 0) RO-Zero
(for Upstream Ports) RO-Zero

m. DRS Message Received
(For Base 3.x or later testing)
(for Downstream Ports with DRS Supported as 1) RW1C
(for Downstream Ports with DRS Supported as 0) RO-Zero
(for Upstream Ports) RO-Zero

n. RsvdZ_15-1
(For Base 2.x testing) RO-Zero

o. RsvdZ_15-0
(For Base 1.x testing) RO-Zero

Link Status 2 Register (Offset 32h) — WORD
(for RC Integrated Endpoint and RC Event Collector)

a. RsvdZ_15-0 RO-Zero

13. The following default value checks are performed:

Link Control 2 Register Default Value (Offset 30h) — WORD
(for all except for RC Integrated Endpoint and RC Event Collector)

a. Target Link Speed
(For Base 2.x or later testing)
(for all single function devices) [HLS] see Note below
(for all devices associated with a Downstream Port) [HLS] see Note below
(for function 0 of a multi-function device associated with an Upstream Port) [HLS] see Note below
(for not function 0 of a multi-function device associated with an Upstream Port) 0
Note: The Highest supported Link Speed [HLS] is the value returned in the Max Link Speed/Supported Link Speeds field (Link Control register). [HLS] may also be 0000b if the Max Link Speed/Supported Link Speeds field returns 0001b (2.5 GT/s only).
Note: This test must only write supported values as reported in the Max Link Speed/Supported Link Speeds field.

b. Hardware Autonomous Speed Disable
(For Base 2.x or later testing) 0

c. Transmit Margin
(For Base 2.x or later testing) 000b

d. Enter Modified Compliance
(For Base 2.x or later testing) 0

e. Compliance SOS
(For Base 2.x or later testing) 0

f. Compliance Preset/De-emphasis
(For Base 3.x or later testing) 0000b
Note: For Base 3.x or later, this field consists of bits 15-12 of this register.

g. Compliance De-emphasis
(For Base 2.x testing) 0
Note: For Base 2.x, this field consists of bit 12 of this register.

Note: The Enter Compliance field cannot be tested for default value, as setting it to 1 and then doing a Hot Reset (secondary bus reset) or DL_Down (link disable/enable), will cause the link to go to Compliance Pattern state and it may not return to L0 again.

Link Status 2 Register Default Value (Offset 32h) — WORD
(for all except for RC Integrated Endpoint and RC Event Collector)

a. Link Equalization Request 8.0 GT/s
(For Base 3.x or later testing:
if Max Link Speed/Supported Link Speeds is 0010b or less) 0
Note: A function under test that supports 8.0 GT/s will participate in Link Equalization, so the default values of the 8.0 GT/s equalization status fields cannot be tested on an 8.0 GT/s capable device.

Note: The DRS Message Received field cannot be tested for default value, even though it will clear in a Downstream Port on DL_Down, because when the link retrains, new DRS Messages may be received.

14. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- ❑ A PCI Express Capability structure is not present.
- ❑ More than one PCI Express Capability structure is present.
- ❑ The Supported Link Speeds Vector field is not one of the allowed values.
- ❑ The Supported Link Speeds Vector field does not also support all lower speeds.
- ❑ The Lower SKP OS Generation Supported Speeds Vector field is not one of the allowed values.
- ❑ The Lower SKP OS Reception Supported Speeds Vector field is not one of the allowed values.
- ❑ In port supporting 16.0 GT/s or higher, the Retimer Presence Detect Supported field reports 0 (for Base 4.x or later testing only).
- ❑ In port supporting 16.0 GT/s or higher, the Two Retimers Presence Detect Supported field reports 0 (for Base 4.x or later testing only).
- ❑ The Retimer Presence Detect Supported field reports 0, but the Two Retimers Presence Detect Supported field reports 1 (for Base 4.x or later testing only).
- ❑ In a downstream port where the FRS Supported field reports 1, the DRS Supported field reports 0.
- ❑ The Target Link Speed field is not one of the allowed values.
- ❑ For function 0 only, the Target Link Speed field is not the highest supported link speed.

- When operating at 5.0 GT/s, the Current De-emphasis Level field does not match the expected setting of the specific test system.
- In port supporting 16.0 GT/s or higher, the Crosslink Supported field reports 1, but the Crosslink Resolution field reports 00b (for Base 4.x or later testing only).
- In port supporting 16.0 GT/s or higher, the Crosslink Supported field reports 0, but the Crosslink Resolution field reports 11b (for Base 4.x or later testing only).
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

2.2.8. TD_1_49 Slot Capabilities, Slot Control, and Slot Status Registers (PCIe Cap Ver = 2)

The test verifies that if the function under test reports support for a Slot Connector, it implements the Slot Capabilities, Slot Control, and Slot Status registers as defined in the relevant specifications. For upstream ports, and for functions not associated with a port, the Slot Capabilities, Slot Control, and Slot Status registers must be hardwired to zero. For downstream ports, if the Slot Implemented field is 1 or if the Data Link Layer Link Active Reporting Capable field is 1, the Slot Capabilities, Slot Control, and Slot Status registers must be implemented. For downstream ports, if the Slot Implemented field is 0 and if the Data Link Layer Link Active Reporting Capable field is 0, the Slot Capabilities, Slot Control, and Slot Status registers may be hardwired to zero (except for the Presence Detect State field in the Slot Status register which must be hardwired to 1).

Relevant Specifications

- *PCI Express Base Specification*
- *ECN Downstream Port Containment (DPC) (to Base 3.0)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Capability ID field for each of the function's Capability structures. Determine how many instances of the Capability ID of 10h (PCI Express Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Capability ID of 10h is not found in a Capability structure, the test terminates with a failure.

4. If the Capability ID of 10h is found in a Capability structure, read a WORD located at offset 02h in the PCI Express Capability structure and if the Capability Version field is equal or less than 1h, the test terminates (this is not a failure and the test result is reported as skipped).
5. If the Capability ID of 10h is found in a Capability structure and if the Capability Version field is equal or greater than 2h, the following tests are performed on that Capability structure:
6. If any of the following are true, then skip to step 11:
 a. If the function under test is associated with an Upstream Port.
 b. If the function under test is not associated with a Port.
 c. If the function under test is associated with a Downstream Port and the Slot Implemented field is 0.
7. Read the DWORD located at offset 14h (Slot Capabilities register) in the PCI Express Capability structure.
8. If the Attention Indicator Present field returns 1, then the following tests are performed:
 a. Test software writes the Attention Indicator Control field with 01b.
 b. If the No Command Completed Support field (Slot Capabilities register) is 0:
 i. Test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then steps a-b are repeated. If this still does not occur after 10 repeats, this part of the test terminates with a test failure and the test continues at step 9. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status).
 c. Test software reads the Attention Indicator Control field and checks that it returns the value previously written. If not, then this part of the test terminates with a test failure and the test continues at step 9.
 d. Repeat steps a-c using the Attention Indicator Control field data values as follows: 10b; 11b.
 e. Perform a default value check on the Attention Indicator Control field and confirm that it returns one of the allowed default values (01b, 10b, or 11b). If not, this is recorded as a failure, but the test continues.
9. If the Power Indicator Present field returns 1, then the following tests are performed:
 a. Test software writes the Power Indicator Control field with 01b.
 b. If the No Command Completed Support field (Slot Capabilities register) is 0:
 i. Test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then steps a-b are repeated. If this still does not occur after 10 repeats, this part of the test terminates with a test failure and the test continues at step 10. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status).
 c. Test software reads the Power Indicator Control field and checks that it returns the value previously written. If not, then this part of the test terminates with a test failure and the test continues at step 10.
 d. Repeat steps a-c using the Power Indicator Control field data values as follows: 10b; 11b.
 e. Perform a default value check on the Power Indicator Control field and confirm that it returns one of the allowed default values (01b, 10b, or 11b). If not, this is recorded as a failure, but the test continues.
10. If the Power Controller Implemented field returns 1, then the following tests are performed:

a. Test software writes the Power Controller Control field with 0.
b. If the No Command Completed Support field (Slot Capabilities register) is 0:
 i. Test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then steps a-b are repeated. If this still does not occur after 10 repeats, this part of the test terminates with a test failure and the test continues at step 11. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status).
c. Test software reads the Power Controller Control field and checks that it returns the value previously written. If not, this part of the test terminates with a test failure and the test continues at step 11.
d. Test software reads the Power Fault Detected field (Slot Status register) and checks that it returns 0. If not, then this part of the test terminates with a test failure and the test continues at step 11.
 (Note: Power Controller Control field data value 1 is not tested, as this would power down the hot-plug slot. There is no intention in this test to remove power from any card in any slot.)

11. The following register field characteristic checks are performed:

Slot Capabilities Register (Offset 14h) – DWORD

a. (for Downstream Ports)Attention Button Present — HwInit
b. Power Controller Present — HwInit
c. MRL Sensor Present — HwInit
d. Attention Indicator Present — HwInit
e. Power Indicator Present — HwInit
f. Hot-Plug Surprise — HwInit
g. Hot-Plug Capable — HwInit
h. Slot Power Limit Value — HwInit
i. Slot Power Limit Scale — HwInit
j. Electromechanical Interlock Present — HwInit
k. No Command Completed Support — HwInit
l. Physical Slot Number — HwInit

Slot Capabilities Register (Offset 14h) — DWORD

(for all functions other than Downstream Ports)

a. RsvdP_31-0 — RO-Zero

Slot Control Register (Offset 18h) — WORD

(for Downstream Ports)

a. Attention Button Pressed Enable
 (if Attention Button Present is 1) — RW
 (if Attention Button Present is 0) — RW or RO-Zero
b. Power Fault Detected Enable — RW or RO-Zero
c. MRL Sensor Changed Enable
 (if MRL Sensor Present is 1) — RW

(if MRL Sensor Present is 0) RW or RO-Zero

d. Presence Detect Changed Enable
(if Hot-Plug Capable is 1) RW
(if Hot-Plug Capable is 0) RW or RO-Zero

e. Command Completed Interrupt Enable
(if No Command Completed Support is 0) RW
(if No Command Completed Support is 1) RO-Zero

f. Hot-Plug Interrupt Enable
(if Hot-Plug Capable is 1) RW
(if Hot-Plug Capable is 0) RW or RO-Zero

g. Attention Indicator Control
(if Attention Indicator Present is 1 and No Command Completed Support is 1) RW
(if Attention Indicator Present is 0) RW or RO-Zero

h. Power Indicator Control
(if Power Indicator Present is 1 and No Command Completed Support is 1) RW
(if Power Indicator Present is 0) RW or RO-Zero

i. Power Controller Control
(if Power Controller Present is 1 and No Command Completed Support is 1) RW
Note: Writing Power Controller Control with 1 in a Downstream Port with a slot causes the slot to power off. The test should restore this field to 0 when completing testing of this register.

j. Electromechanical Interlock Control RO-Zero
Note: The Electromechanical Interlock Control field always returns 0 when read.

k. Data Link Layer State Changed Enable
(if Data Link Layer Link Active Reporting Capable is 1) RW
(if Data Link Layer Link Active Reporting Capable is 0) RW or RO-Zero

l. RsvdP_15-13
(For Base 2.x or earlier testing) RO-Zero

m. Auto Slot Power Limit Disable
(For Base 3.x or later testing)
(for Root Ports and Switch Downstream Ports, with DPC Extended Capability present) RW
(for Root Ports and Switch Downstream Ports, without DPC Extended Capability) RW or RO-Zero
(otherwise) RO-Zero

n. RsvdP_15-14
(For Base 3.x or later testing) RO-Zero

Slot Control Register (Offset 18h) — WORD
(for all functions other than Downstream Ports)

a. RsvdP_15-0 RO-Zero

Slot Status Register (Offset 1Ah) — WORD
(for Downstream Ports)

a. Attention Button Pressed
 (if Attention Button Present is 1) RW1C
 (if Attention Button Present is 0) RO-Zero
b. Power Fault Detected
 (if Power Controller Present is 1) RW1C
 (if Power Controller Present is 0) RO-Zero
c. MRL Sensor Changed
 (if MRL Sensor Present is 1) RW1C
 (if MRL Sensor Present is 0) RO-Zero
d. Presence Detect Changed RW1C
 Note: The Presence Detect Changed field cannot be tested for default value on form factors that don't provide an out-of-band presence signal, as the in-band presence will be cleared upon entry to Detect state, and will be updated with a fresh value upon exit from Detect state, which can result in a presence change.
e. Command Completed
 (if No Command Completed Support is 0) RW1C
 (if No Command Completed Support is 1) RO-Zero
f. MRL Sensor State RO
g. Presence Detect State
 (if Slot Implemented is 1) RO
 (if Slot Implemented is 0) RO-Ones
h. Electromechanical Interlock Status RO
i. Data Link Layer State Changed RW1C
j. RsvdZ_15-9 RO-Zero

Slot Status Register (Offset 1Ah) — WORD
(for all functions other than Downstream Ports)

a. RsvdZ_15-0 RO-Zero

12. The following default value checks are performed:

Slot Control Register Default Value (Offset 18h) — WORD
(for Downstream Ports)

a. Attention Button Pressed Enable 0
b. Power Fault Detected Enable 0
c. MRL Sensor Changed Enable 0
d. Presence Detect Changed Enable 0
e. Command Completed Interrupt Enable 0
f. Hot-Plug Interrupt Enable 0
g. Data Link Layer State Changed Enable 0

Slot Status Register Default Value (Offset 1Ah) — WORD
(for Downstream Ports)

a. Attention Button Pressed 0
b. Power Fault Detected 0

c. MRL Sensor Changed 0
d. Command Completed 0

13. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- A PCI Express Capability structure is not present.
- More than one PCI Express Capability structure is present.
- The No Command Completed Support field is 0, but the Command Completed field status does not return 1 within the time allowance after initiating a command.
- The Attention Indicator Present field is 1, but the Power Indicator Control field cannot be written with one of the valid values.
- The Power Indicator Present field is 1, but the Power Indicator Control field cannot be written with one of the valid values.
- The Power Controller Implemented field is 1, but the Power Controller Control field cannot be written with the ON value (0), or the Power Fault Detected field status returns 1.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

2.2.9. TD_1_50 Slot Capabilities 2, Slot Control 2, and Slot Status 2 Registers (PCIe Cap Ver = 2)

The test verifies that if the function under test reports support for a Slot Connector, it implements the Slot Capabilities 2, Slot Control 2, and Slot Status 2 registers as defined in the relevant specifications. For upstream ports, and for functions not associated with a port, the Slot Capabilities 2, Slot Control 2, and Slot Status 2 registers must be hardwired to zero. For downstream ports, if the Slot Implemented field is 1, the Slot Capabilities 2, Slot Control 2, and Slot Status 2 registers may be implemented. For downstream ports, if the Slot Implemented field is 0 the Slot Capabilities 2, Slot Control 2, and Slot Status 2 registers may be hardwired to zero.

Relevant Specifications

- *PCI Express Base Specification*
- *ECN PCI Express Capability Structure Expansion (to Base 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Capability ID field for each of the function's Capability structures. Determine how many instances of the Capability ID of 10h (PCI Express Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Capability ID of 10h is not found in a Capability structure, the test terminates with a failure.
4. If the Capability ID of 10h is found in a Capability structure, read a WORD located at offset 02h in the PCI Express Capability structure and if the Capability Version field is equal or less than 1h, the test terminates. (For Base 2.x or later testing, this is a failure. For Base 1.x testing, this is not a failure and the test result is reported as skipped.)
5. If the Capability ID of 10h is found in a Capability structure and if the Capability Version field is equal or greater than 2h, the following register field characteristic checks are performed on that Capability structure:

 Slot Capabilities 2 Register (Offset 34h) –– DWORD
 a. RsvdP_31-0 RO-Zero

 Slot Control 2 Register (Offset 38h) –– WORD
 a. RsvdP_15-0 RO-Zero

 Slot Status 2 Register (Offset 3Ah) –– WORD
 a. RsvdZ_15-0 RO-Zero

6. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- A PCI Express Capability structure is not present.
- More than one PCI Express Capability structure is present.
- Any of the register field characteristic tests fail.

2.2.10. TD_1_51 Root Capabilities, Root Control, and Root Status Registers (PCIe Cap Ver = 2)

The test verifies that if the function under test is a Root Port or a Root Complex Event Collector, it implements the Root Capabilities, Root Control, and Root Status registers as defined in the relevant

specifications. For other device types the Root Capabilities, Root Control, and Root Status registers must be hardwired to zero.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Capability ID field for each of the function's Capability structures. Determine how many instances of the Capability ID of 10h (PCI Express Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Capability ID of 10h is not found in a Capability structure, the test terminates with a failure.
4. If the Capability ID of 10h is found in a Capability structure, read a WORD located at offset 02h in the PCI Express Capability structure and if the Capability Version field is equal or less than 1h, the test terminates (this is not a failure and the test result is reported as skipped).
5. If the Capability ID of 10h is found in a Capability structure and if the Capability Version field is equal or greater than 2h, the following register field characteristic checks are performed on that Capability structure:

 Root Control Register (Offset 1Ch) — WORD
 (for Root Port or RC Event Collector)

a. System Error on Correctable Error Enable	RW
b. System Error on Non-Fatal Error Enable	RW
c. System Error on Fatal Error Enable	RW
d. PME Interrupt Enable	RW
e. CRS Software Visibility Enable	
(for Root Ports with CRS Software Visibility as 1)	RW
(for Root Ports with CRS Software Visibility as 0)	RO-Zero
(for RC Event Collectors)	RO-Zero
f. RsvdP_15-5	RO-Zero

 Root Control Register (Offset 1Ch) — WORD
 (for all except Root Port and RC Event Collector)

a. RsvdP_15-0	RO-Zero

 Root Capabilities Register (Offset 1Eh) — WORD
 (for Root Port or RC Event Collector)

a. CRS Software Visibility
 (for Root Ports) RO
 (for RC Event Collectors) RO-Zero
b. RsvdP_15-1 RO-Zero

Root Capabilities Register (Offset 1Eh) — WORD
(for all except Root Port and RC Event Collector)
a. RsvdP_15-0 RO-Zero

Root Status Register (Offset 20h) — DWORD
(for Root Port or RC Event Collector)
a. PME Requester ID RO
b. PME Status RW1C
c. PME Pending RO
d. RsvdZ_31-18 RO-Zero

Root Status Register (Offset 20h) — DWORD
(for all except Root Port and RC Event Collector)
a. RsvdZ_31-0 RO-Zero

6. If the Capability ID of 10h is found in a Capability structure and if the Capability Version field is equal or greater than 2h, the following default value checks are performed on that Capability structure:

Root Control Register (Offset 1Ch) — WORD
(for Root Port or RC Event Collector)
a. System Error on Correctable Error Enable 0
b. System Error on Non-Fatal Error Enable 0
c. System Error on Fatal Error Enable 0
d. PME Interrupt Enable 0
e. CRS Software Visibility Enable
 (for Root Ports) 0

Root Status Register (Offset 20h) — DWORD
(for Root Port or RC Event Collector)
a. PME Status 0

7. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- ❑ A PCI Express Capability structure is not present.
- ❑ More than one PCI Express Capability structure is present.
- ❑ Any of the register field characteristic tests fail.
- ❑ Any of the default value tests fail.

2.2.11. TD_1_6 MSI Capability Structure

The test verifies that if the function under test reports a MSI Capability structure, it is implemented as defined in the relevant specifications. (If support for specific features is indicated, the function must implement at least either a MSI or a MSI-X Capability structure. The MSI-X Capability structure is tested elsewhere.)

Relevant Specifications

- *PCI Express Base Specification*
- *PCI Local Bus Specification, Revision 3.0 (Base 3.x or earlier only)*
- *Single Root I/O Virtualization and Sharing Specification (Base 3.x or earlier only)*
- *ECN Extended Message Data for MSI (to Base 3.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Capability ID field for each of the function's Capability structures. If the Capability ID of 05h is not found in a Capability structure, the following tests are performed on that function:
 a. Examine the Capability ID field for each of the function's Capability structures. If the Capability ID of 11h (MSI-X Capability) is not found in a Capability structure, all of the following are checked. If any of these are not true, the test fails and this is recorded as a failure, while the test continues at the next step.
 i. The Interrupt Pin register (location 3Dh) value is zero.
 ii. The function under test is not a Root Port.
 iii. The function under test is not a Root Complex Event Collector.
 iv. If the function under test is a downstream port, the DRS Supported bit (Link Capabilities 2 register) value is 0.
 v. If the function under test is a downstream port, it does not contain a DPC Extended Capability structure.
 vi. If the function under test is a PF, the VF Migration Capable bit (SR-IOV Capabilities register) value is 0.
3. Examine the Capability ID field for each of the function's Capability structures. Determine how many instances of the Capability ID of 05h (MSI Capability) are found. If more than one is found, the test terminates with a failure.

4. If the Capability ID of 05h is found in a Capability structure, the following steps are performed on that Capability structure. If the Capability ID of 05h is not found in a Capability structure, the test skips to step 10.
5. A WORD is read from offset 00h in the MSI Capability structure (Capability ID field, Next Capability Pointer field) and the following tests are performed:
 a. The Next Capability Pointer field must be 00h or greater than 3Fh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
6. A WORD is read from offset 02h in the MSI Capability structure (MSI Control register) and the following tests are performed:
 a. The Multiple Message Capable field must not return 110b or 111b (Reserved). If it does this is recorded as a failure, but the test continues.
 b. If the function is not a VF and if the function implements a SR-IOV Extended Capability structure, the Per-Vector Masking Capable field must return 1. If it does not this is recorded as a failure, but the test continues.
 c. If the function is not a VF and if the function does not implement a SR-IOV Extended Capability structure, the Per-Vector Masking Capable field should return 1. If it does not a warning message is issued, but this is not treated in itself as a failure.
7. Test software writes each supported data value (based on the value read from the Multiple Message Capable field) into the Multiple Message Enable field (e.g., if the Multiple Message Capable field reports 001b meaning two messages are supported, then data values of 001b and 000b are written to the Multiple Message Enable field). After each write test software checks that the same value is read back from the Multiple Message Enable field. If a different value is read back then this is recorded as a failure, but the test continues.
8. The following register field characteristic checks are performed:

MSI Capability Header (Offset 00h) — WORD

a. Capability ID	RO
b. Next Capability Pointer	RO

Message Control Register (Offset 02h) — WORD

a. MSI Enable	RW
b. Multiple Message Capable	RO
c. Multiple Message Enable	RW
d. 64 Bit Address Capable	RO
e. Per-Vector Masking Capable	
(for VFs)	RO-Ones
(otherwise)	RO
f. Extended Message Data Capable	
(For Base 3.1 or later testing)	RO
g. Extended Message Data Enable	
(For Base 3.1 or later testing)	
(with Extended Message Data Capable as 1)	RW
(with Extended Message Data Capable as 0)	RO-Zero
h. Reserved_15-11	
(For Base 3.1 or later testing)	RO-Zero
i. Reserved_15-9	
(For Base 3.0 or earlier testing)	RO-Zero

Message Address Register (Offset 04h) — DWORD

a. RsvdP_1-0 RO-Zero
b. Message Address RW

Message Upper Address Register (Offset 08h) — DWORD (Only if 64 Bit Address Capable is 1)

a. Message Upper Address RW

Message Data Register (Offset 08h if 64 Bit Address Capable is 0 or Offset 0Ch if 64 Bit Address Capable is 1) — WORD

a. Message Data RW

Extended Message Data Register (Offset 0Ah if 64 Bit Address Capable is 0 or Offset 0Eh if 64 Bit Address Capable is 1) — WORD (Only if Extended Message Data Capable is 1)

a. Extended Message Data
(For Base 3.1 or later testing)
(with Extended Message Data Capable as 1) RW

Reserved Register (Offset 0Ah if 64 Bit Address Capable is 0 or Offset 0Eh if 64 Bit Address Capable is 1) – WORD (Only if Per-Vector Masking Capable is 1 and Extended Message Data Capable is 0)

a. RsvdP_15-0 RO-Zero

Mask Bits Register (Offset 0Ch if 64 Bit Address Capable is 0 or 10h if 64 Bit Address Capable is 1) — DWORD (Only if Per-Vector Masking Capable is 1)

The value returned in the Multiple Message Capable field is used to determine N as follows: N = 2 ** [value].

a. (bits N-1 to 0) RW
b. (bits 31 to N) RO-Zero

Pending Bits Register (Offset 10h if 64 Bit Address Capable is 0 or Offset 14h if 64 Bit Address Capable is 1) — DWORD (Only if Per-Vector Masking Capable is 1)

The value returned in the Multiple Message Capable field is used to determine N as follows: N = 2 ** [value].

a. (bits N-1 to 0) RO
b. (bits 31 to N) RO-Zero

9. The following default value checks are performed:

Message Control Register Default Value (Offset 02h) — WORD

a. MSI Enable 0
b. Multiple Message Enable 000b
c. Extended Message Data Enable
(For Base 3.1 or later testing) 0

Extended Message Data Register Default Value (Offset 0Ah if 64 Bit Address Capable is 0 or Offset 0Eh if 64 Bit Address Capable is 1) — WORD (Only if Extended Message Data Capable is 1)

a. Extended Message Data
(For Base 3.1 or later testing) 0000h

Mask Bits Register Default Value (Offset 0Ch if 64 Bit Address Capable is 0 or 10h if 64 Bit Address Capable is 1) — DWORD (Only if Per-Vector Masking Capable is 1)

The value returned in the Multiple Message Capable field is used to determine N as follows: N = 2 ** [value].

a. Mask Bits (N-1 to 0) 0 (each bit)

Pending Bits Register Default Value (Offset 10h if 64 Bit Address Capable is 0 or Offset 14h if 64 Bit Address Capable is 1) — DWORD (Only if Per-Vector Masking Capable is 1)

The value returned in the Multiple Message Capable field is used to determine N as follows: N = 2 ** [value].

a. Pending Bits (N-1 to 0) 0 (each bit)

10. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- ❑ Neither a MSI Capability structure nor a MSI-X Capability structure is present in the following:
 - A function that has Interrupt Pin register as non-zero
 - A Root Port
 - A Root Complex Event Collector
 - A downstream port that has DRS Supported set to 1
 - A downstream port that has a DPC Extended Capability structure
 - A PF that has VF Migration Supported set to 1
- ❑ More than one MSI Capability structure is present.
- ❑ A non-zero Next Capability Pointer field value is less than or equal to 3Fh, or the lower 2 bits are non-zero.
- ❑ The Multiple Message Capable field reports a reserved value.
- ❑ For a function that implements a SR-IOV Extended Capability structure, the Per-Vector Masking Capable field reports 0.
- ❑ Any of the allowed multiple message values cannot be written to and read back from the Multiple Message Enable field.
- ❑ Any of the register field characteristic tests fail.
- ❑ Any of the default value tests fail.

The test *warns* if:

- ❑ For a non-VF function that does not implement a SR-IOV Extended Capability structure, the Per-Vector Masking Capable field reports 0.

2.2.12. TD_1_7 Advanced Error Reporting Extended Capability Structure

The test verifies that if the function under test reports a PCI Express Advanced Error Reporting Extended Capability structure it is implemented as defined in the relevant specifications.

(Note: In the various revisions of the specification, the default value of unimplemented Uncorrectable Error Severity register fields was defined in a contradictory manner. The different revisions attempted to correct this with only limited success. The current specification definition makes the default value of unimplemented Uncorrectable Error Severity register fields implementation-specific and therefore having no testable value. This is the definition that this test document implements regardless of the revision testing level, since it can be supported by all specification revisions.)

Relevant Specifications

- *PCI Express Base Specification*
- *ECN Access Control Services (to Base 1.1)*
- *ECN Internal Error Reporting (to Base 2.0)*
- *ECN Multicast (to Base 2.0)*
- *ECN Atomic Operations (to Base 2.0)*
- *ECN TLP Prefix (to Base 2.0)*
- *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0*
- *Single Root I/O Virtualization and Sharing Specification (Base 3.x or earlier only)*
- *ECN Downstream Port Containment (DPC) (to Base 3.0)*
- *ECN Enhanced DPC (eDPC) (to Base 3.0)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0001h (Advanced Error Reporting Extended Capability) are found. If more than one is found, the test terminates with a failure.

3. If the Extended Capability ID of 0001h is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
4. For Base 2.x or later testing: the following tests are performed:
 a. If the function under test contains an ACS Extended Capability structure (Extended Capability ID of 000Dh) then if the Extended Capability ID of 0001h is not found in an Extended Capability structure, the test logs a warning, but the test continues.
 b. If the function under test contains a Multicast Extended Capability structure (Extended Capability ID of 0012h) then if the Extended Capability ID of 0001h is not found in an Extended Capability structure, the test logs a warning, but the test continues.
5. If the Extended Capability ID of 0001h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0001h is not found in an Extended Capability structure, the test skips to step 30.
6. DWORDs are read from offsets 00h to 28h to obtain the default values for each of the capability fields. Root Ports and Root Complex Event Collectors, that report AER Capability Version of 1h, additionally read offsets 2Ch to 34h to obtain those default values. Any non-Bridge function that reports AER Capability Version of 2h or greater additionally read offsets 2Ch to 44h to obtain these default values. Any Bridges additionally read offsets 2Ch to 48h to obtain these default values.
7. For Base 1.x testing: the Capability Version field (Advanced Error Reporting Extended Capability Header) must be 1h. If not, this is recorded as a failure, but the test continues.
8. For Base 2.x or later testing, if the function under test reports the Capability Version field (PCI Express Capabilities register) is 1h or less:
 a. The Capability Version field (Advanced Error Reporting Extended Capability Header) can be 1h or 2h. If not, this is recorded as a failure, but the test continues.
9. For Base 2.x or later testing, if the function under test reports the Capability Version field (PCI Express Capabilities register) is 2h or greater:
 a. If the End-End TLP Prefix Supported field (Device Capabilities 2 register) is 0, then the Capability Version field (Advanced Error Reporting Extended Capability Header) can be 1h or 2h. If not, this is recorded as a failure, but the test continues.
10. For Base 2.x or later testing, if the function under test reports the Capability Version field (PCI Express Capabilities register) is 2h or greater:
 a. If the End-End TLP Prefix Supported field (Device Capabilities 2 register) is 1, then the Capability Version field (Advanced Error Reporting Extended Capability Header) must be 2h. If not, this is recorded as a failure, but the test continues.
11. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
12. The default values of each of the defined bits in the Uncorrectable Error Status register must be 0 with the exception of bit 0 (undefined) which is not checked. If not, this is recorded as a failure, but the test continues.
 Note: The default value requirement applies to all devices except Root Complexes.
13. Each defined bit in the Uncorrectable Error Mask register must read zero by default with the exception of the following: bit 0 (undefined) which is not checked; bit 22 (Uncorrectable Internal Error) which is checked to default to 1 if the bit is writeable or default to 0 if it is not

writeable. If not, this is recorded as a failure, but the test continues. Test software writes 1 to each of these bits and verifies that 1 is read back. Test software records each bit that cannot be set to 1 (Unsupported uncorrectable error bits). If a required bit (bits 4, 12, 16, 18, 20 and for non-Switch Ports bit 14) cannot be set to 1, then this is recorded as a failure, but the test continues.

14. Test software writes all Uncorrectable Error Mask bits to their default values.
15. Test software checks the default values of each bit in the Uncorrectable Error Severity register defined bits with the exception of bit 0 (undefined) which is not checked. If not, this is recorded as a failure, but the test continues. Test software then writes the opposite value to each bit and checks that the written value is returned. If not, this is recorded as a failure, but the test continues.

 Note: This rule does not apply to bits corresponding to Uncorrectable Error Mask bits that are not implemented as writeable.

 Note: The default value requirement applies to all devices except Root Complexes.
16. Test software writes all Uncorrectable Error Severity bits to their default values.
17. Test software checks that all values for defined bits in the Correctable Error Status register are zero. If not, this is recorded as a failure, but the test continues.

 Note: The default value requirement applies to all devices except Root Complexes.
18. Test software checks that the Correctable Error Mask registers all read zero by default with the exception of the following: bit 13 (Advisory Non-Fatal Error) which is checked to default to 1; bit 14 (Corrected Internal Error) which is checked to default to 1 if the bit is writeable or default to 0 if it is not writeable; bit 15 (Header Log Overflow) which is checked to default to 1 if the bit is writeable or default to 0 if it is not writeable. If not, this is recorded as a failure, but the test continues. Test software records each bit that cannot be set (Unsupported correctable error bits). If a required bit (bits 6, 7, 8, 12, 13) cannot be set, then this is recorded as a failure, but the test continues.
19. Test software writes all Correctable Error Mask bits to their default values.
20. The Advanced Error Capabilities and Control register is examined. The ECRC Generation Enable and the ECRC Check Enable fields must default to zero. If not, this is recorded as a failure, but the test continues. For Base 2.x or later testing: the Multiple Header Recording Enable field must also default to zero. If not, this is recorded as a failure, but the test continues.
 a. If the ECRC Check Capable field is 1, test software checks to ensure that the ECRC Check Enable field is writeable and can be set to 1 and cleared to 0. If not, this is recorded as a failure, but the test continues.
 b. If the ECRC Generation Capable field is 1, test software checks to ensure that the ECRC Generation Enable field is writeable and can be set to 1 and cleared to 0. If not, this is recorded as a failure, but the test continues.
 c. For Base 2.x or later testing: if the Multiple Header Recording Capable field is 1, test software checks to ensure that the Multiple Header Recording Enable field is writeable and can be set to 1 and cleared to 0. If not, this is recorded as a failure, but the test continues.
 d. For Base 3.x or later testing: test software checks to ensure that the Completion Timeout Prefix/Header Log Capable field should return 1. If not, a warning message is issued, but this is not treated in itself as a failure.

 Note: The default value requirement applies to all devices except Root Complexes.

21. For Root Ports and Root Complex Event Collectors only: test software checks that the Root Error Status register defaults to zero, excluding bits 31-27 (Advanced Error Interrupt Message Number) which are not checked. If not, this is recorded as a failure, but the test continues.
22. For Root Ports and Root Complex Event Collectors only: test software checks that the Error Source Identification register defaults to zero. If not, this is recorded as a failure, but the test continues.
23. For Bridges only: the default values of each of the defined bits in the Secondary Uncorrectable Error Status register must be zero. If not, this is recorded as a failure, but the test continues.
24. For Bridges only: each defined bit in the Secondary Uncorrectable Error Mask register must read zero by default with the exception of the following: bit 3 (Received Master-Abort); bit 5 (Unexpected Split Completion Error); bit 7 (Uncorrectable Data Error Mask); bit 8 (Uncorrectable Attribute Error); bit 9 (Uncorrectable Address Error); bit 10 (Delayed Transaction Discard Timer Expired); bit 12 (SERR# Assertion Detected) all of which are checked to default to 1 if the bit is writeable or default to 0 if it is not writeable. If not, this is recorded as a failure, but the test continues. Test software writes 1 to each of these bits and verifies that 1 is read back. Test software records each bit that cannot be set to 1 (Unsupported secondary uncorrectable error bits). If a required bit (bits 1, 3, 5-13) cannot be set to 1, then this is recorded as a failure, but the test continues.
25. For Bridges only: test software writes all Secondary Uncorrectable Error Mask bits to their default values.
26. For Bridges only: test software checks the default values of each bit in the Secondary Uncorrectable Error Severity register defined bits. If not, this is recorded as a failure, but the test continues. Test software then writes the opposite value to each bit and checks that the written value is returned. If not, this is recorded as a failure, but the test continues.

 Note: This rule does not apply to bits corresponding to Secondary Uncorrectable Error Mask bits that are not implemented as writeable.
27. For Bridges only: test software writes all Secondary Uncorrectable Error Severity bits to their default values.
28. The following register field characteristic checks are performed:

Advanced Error Reporting Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

Uncorrectable Error Status Register (Offset 04h) — DWORD

a. RsvdZ_3-1	RO-Zero
b. Data Link Protocol Error Status	
(for VFs)	RO-Zero
(otherwise)	RW1CS
c. Surprise Down Error Status (Optional)	
(for Downstream Ports with Surprise Down Error Capable as 1)	RW1CS
(for Downstream Ports with Surprise Down Error Capable as 0)	RO-Zero
(for Upstream Ports or VFs)	RO-Zero
d. RsvdZ_11-6	RO-Zero

e. Poisoned TLP Received Status — RW1CS
f. Flow Control Protocol Error Status (Optional-Mask)
 (for VFs) — RO-Zero
 (otherwise) — RW1CS
g. Completion Timeout Status
 (for Switch Ports) — RW1CS or RO-Zero
 (for any device other than a Switch Port) — RW1CS
 Note: For a Switch Port there is no way to tell whether Completion Timeout Status needs to be RW1CS since there is no way to determine if the Switch Port may act as a requester on its own behalf.
h. Completer Abort Status (Optional-Mask) — RW1CS
i. Unexpected Completion Status — RW1CS
j. Receiver Overflow Status (Optional-Mask)
 (for VFs) — RO-Zero
 (otherwise) — RW1CS
k. Malformed TLP Status
 (for VFs) — RO-Zero
 (otherwise) — RW1CS
l. ECRC Error Status (Optional)
 (for VFs) — RO-Zero
 (for non-VFs with ECRC Check Capable is 1) — RW1CS
 (for non-VFs with ECRC Check Capable is 0) — RO-Zero
m. Unsupported Request Error Status — RW1CS
n. ACS Violation Status (Optional)
 (for any function without ACS Extended Capability) — RO-Zero
 (for Downstream Ports with ACS Extended Capability) — RW1CS
 (for Upstream Ports in a single function device that is not a PF) — RO-Zero
 (for Upstream Ports in single function device that is a PF with ACS P2P Egress Control as 0) — RO-Zero
 (for Upstream Ports in single function device that is a PF with ACS P2P Egress Control as 1) — RW1CS
 (for Upstream Ports in multi-function device with ACS P2P Egress Control as 0) — RO-Zero
 (for Upstream Ports in multi-function device with ACS P2P Egress Control as 1) — RW1CS
o. Uncorrectable Internal Error Status
 (For Base 2.x or later testing: Optional-Mask) — RW1CS
p. MC Blocked TLP Status
 (For Base 2.x or later testing: Optional)
 (for any function without Multicast Extended Capability) — RO-Zero
 (for any function with Multicast Extended Capability) — RW1CS
q. AtomicOp Egress Blocked Status
 (For Base 2.x or later testing: Optional)
 (if AtomicOp Routing Supported is 1) — RW1CS
 (if AtomicOp Routing Supported is 0) — RO-Zero
r. TLP Prefix Blocked Error Status
 (For Base 2.x or later testing: Optional)

(for Root Ports and Switch Ports,
with End-End TLP Prefix Supported as 0) RO-Zero
(for Root Ports and Switch Ports,
with End-End TLP Prefix Supported as 1) RW1CS
(for any function other than Root Port or Switch Port) RO-Zero

s. Poisoned TLP Egress Blocked Status
(For Base 3.x or later testing: Optional)
(for Root Ports and Switch Downstream Ports,
with Poisoned TLP Egress Blocking Supported as 0) RO-Zero
(for Root Ports and Switch Downstream Ports,
with Poisoned TLP Egress Blocking Supported as 1) RW1CS
(for any function other than Root Port or Switch Downstream Port) RO-Zero

t. RsvdZ_31-27
(For Base 3.x or later testing) RO-Zero

u. RsvdZ_31-26
(For Base 2.x) RO-Zero

v. RsvdZ_31-22
(For Base 1.x testing) RO-Zero

Note: These tests do not apply to those bits marked (Optional-Mask) if the corresponding mask is not implemented as writeable. In that case the bit is tested as RO-Zero.

Uncorrectable Error Mask Register (Offset 08h) -– DWORD

a. RsvdP_3-1 RO-Zero

b. Data Link Protocol Mask
(for VFs) RO-Zero
(otherwise) RWS

c. Surprise Down Error Mask (Optional)
(for Downstream Ports with Surprise Down Error Capable as 1) RWS
(for Downstream Ports with Surprise Down Error Capable as 0) RO-Zero
(for Upstream Ports or VFs) RO-Zero

d. RsvdP_11-6 RO-Zero

e. Poisoned TLP Received Mask
(for VFs) RO-Zero
(otherwise) RWS

f. Flow Control Protocol Error Mask (Optional-Mask)
(for VFs) RO-Zero
(otherwise) RWS or
RO-Zero

g. Completion Timeout Mask
(for Switch Ports) RWS or
RO-Zero
(for VFs) RO-Zero
(for any non-VF device other than a Switch Port) RWS
Note: For a Switch Port there is no way to tell whether Completion Timeout Mask needs to be RWS since there is no way to determine if the Switch Port may act as a requester on its own behalf.

h. Completer Abort Mask (Optional-Mask)
(for VFs) RO-Zero

(otherwise)	RWS or RO-Zero
i. Unexpected Completion Mask	
(for VFs)	RO-Zero
(otherwise)	RWS
j. Receiver Overflow Mask (Optional-Mask)	
(for VFs)	RO-Zero
(otherwise)	RWS or RO-Zero
k. Malformed TLP Mask	
(for VFs)	RO-Zero
(otherwise)	RWS
l. ECRC Error Mask (Optional)	
(for VFs)	RO-Zero
(for non-VFs with ECRC Check Capable is 1)	RWS
(for non-VFs with ECRC Check Capable is 0)	RO-Zero
m. Unsupported Request Error Mask	
(for VFs)	RO-Zero
(otherwise)	RWS
n. ACS Violation Mask (Optional)	
(for VFs, or any function without ACS Extended Capability)	RO-Zero
(for Downstream Ports with ACS Extended Capability)	RWS
(for Upstream Ports in a single function device that is not a PF)	RO-Zero
(for Upstream Ports in single function device that is a PF with ACS P2P Egress Control as 0)	RO-Zero
(for Upstream Ports in single function device that is a PF with ACS P2P Egress Control as 1)	RWS
(for Upstream Ports in multi-function device with ACS P2P Egress Control as 0)	RO-Zero
(for non-VF Upstream Ports in multi-function device with ACS P2P Egress Control as 1)	RWS
o. Uncorrectable Internal Error Mask	
(For Base 2.x or later testing: Optional-Mask)	RWS or RO-Zero
p. MC Blocked TLP Mask	
(For Base 2.x or later testing: Optional)	
(for any function without Multicast Extended Capability)	RO-Zero
(for any function with Multicast Extended Capability)	RWS
q. AtomicOp Egress Blocked Mask	
(For Base 2.x or later testing: Optional)	
(if AtomicOp Routing Supported is 1)	RWS
(if AtomicOp Routing Supported is 0)	RO-Zero
r. TLP Prefix Blocked Error Mask	
(For Base 2.x or later testing: Optional)	
(for Root Ports and Switch Ports, with End-End TLP Prefix Supported as 0)	RO-Zero
(for Root Ports and Switch Ports, with End-End TLP Prefix Supported as 1)	RWS

(for any function other than Root Port or Switch Port) RO-Zero

s. Poisoned TLP Egress Blocked Mask
(For Base 3.x or later testing: Optional)
(for Root Ports and Switch Downstream Ports,
with Poisoned TLP Egress Blocking Supported as 0) RO-Zero
(for Root Ports and Switch Downstream Ports,
with Poisoned TLP Egress Blocking Supported as 1) RWS
(for any function other than Root Port or Switch Downstream Port) RO-Zero

t. RsvdP_31-27
(For Base 3.x or later testing) RO-Zero

u. RsvdP_31-26
(For Base 2.x) RO-Zero

v. RsvdP_31-22
(For Base 1.x testing) RO-Zero

Note: Those bits that are marked (Optional-Mask) are checked to see if they are writeable or non-writeable. If one of those bits is writeable then that specific bit is considered implemented for the Status/Mask/Severity registers. Otherwise that specific bit is considered unimplemented for the Status/Mask/Severity registers. A writeable bit will be tested as RWS. A non-writeable bit will be tested as RO-Zero.

Uncorrectable Error Severity Register (Offset 0Ch) — DWORD

a. RsvdP_3-1 RO-Zero

b. Data Link Protocol Error Severity
(for VFs) RO-Zero
(otherwise) RWS

c. Surprise Down Error Severity (Optional)
(for Downstream Ports with Surprise Down Error Capable as 1) RWS
(for Downstream Ports with Surprise Down Error Capable as 0) RO
(for VFs) RO-Zero
(for non-VF Upstream Ports) RO

d. RsvdP_11-6 RO-Zero

e. Poisoned TLP Received Severity
(for VFs) RO-Zero
(otherwise) RWS

f. Flow Control Protocol Error Severity (Optional-Mask)
(for VFs) RO-Zero
(otherwise) RWS

g. Completion Timeout Severity
(for Switch Ports) RWS or
RO-Zero
(for VFs) RO-Zero
(for any non-VF device other than a Switch Port) RWS
Note: For a Switch Port there is no way to tell whether Completion Timeout Severity needs to be RWS since there is no way to determine if the Switch Port may act as a requester on its own behalf.

h. Completer Abort Error Severity (Optional-Mask)
(for VFs) RO-Zero
(otherwise) RWS

i. Unexpected Completion Severity
 (for VFs) RO-Zero
 (otherwise) RWS
j. Receiver Overflow Severity (Optional-Mask)
 (for VFs) RO-Zero
 (otherwise) RWS
k. Malformed TLP Severity
 (for VFs) RO-Zero
 (otherwise) RWS
l. ECRC Error Severity (Optional)
 (for VFs) RO-Zero
 (for non-VFs with ECRC Check Capable is 1) RWS
 (for non-VFs with ECRC Check Capable is 0) RO
m. Unsupported Request Error Severity
 (for VFs) RO-Zero
 (otherwise) RWS
n. ACS Violation Severity (Optional)
 (for VFs) RO-Zero
 (for any non-VF without ACS Extended Capability) RO
 (for Downstream Ports with ACS Extended Capability) RWS
 (for Upstream Ports in a single function device that is not a PF) RO
 (for Upstream Ports in single function device that is a PF
 with ACS P2P Egress Control as 0) RO-Zero
 (for Upstream Ports in single function device that is a PF
 with ACS P2P Egress Control as 1) RWS
 (for Upstream Ports in multi-function device
 with ACS P2P Egress Control as 0) RO
 (for Upstream Ports in multi-function device
 with ACS P2P Egress Control as 1) RWS
o. Uncorrectable Internal Error Severity
 (For Base 2.x or later testing: Optional-Mask) RWS
p. MC Blocked TLP Severity
 (For Base 2.x or later testing: Optional)
 (for any function without Multicast Extended Capability) RO
 (for any function with Multicast Extended Capability) RWS
q. AtomicOp Egress Blocked Severity
 (For Base 2.x or later testing: Optional)
 (if AtomicOp Routing Supported is 1) RWS
 (if AtomicOp Routing Supported is 0) RO
r. TLP Prefix Blocked Error Severity
 (For Base 2.x or later testing: Optional)
 (for Root Ports and Switch Ports,
 with End-End TLP Prefix Supported as 0) RO
 (for Root Ports and Switch Ports,
 with End-End TLP Prefix Supported as 1) RWS
 (for any function other than Root Port or Switch Port) RO
s. Poisoned TLP Egress Blocked Severity
 (For Base 3.x or later testing: Optional)

(for Root Ports and Switch Downstream Ports, with Poisoned TLP Egress Blocking Supported as 0) RO
(for Root Ports and Switch Downstream Ports, with Poisoned TLP Egress Blocking Supported as 1) RWS
(for any function other than Root Port or Switch Downstream Port, RO

t. RsvdP_31-27
(For Base 3.x or later testing) RO-Zero

u. RsvdP_31-26
(For Base 2.x) RO-Zero

v. RsvdP_31-22
(For Base 1.x testing: bits 31-22) RO-Zero

Note: These tests do not apply to those bits marked (Optional-Mask) if the corresponding mask is not implemented as writeable. In that case the bit must be RO (as default values for severity registers are implementation-specific).

Correctable Error Status Register (Offset 10h) — DWORD

a. Receiver Error Status (Optional-Mask)
(for VFs) RO-Zero
(otherwise) RW1CS

b. RsvdZ_5-1 RO-Zero

c. Bad TLP Status
(for VFs) RO-Zero
(otherwise) RW1CS

d. Bad DLLP Status
(for VFs) RO-Zero
(otherwise) RW1CS

e. REPLAY_NUM Rollover Status
(for VFs) RO-Zero
(otherwise) RW1CS

f. RsvdZ_11-9 RO-Zero

g. Replay Timer Timeout Status
(for VFs) RO-Zero
(otherwise) RW1CS

h. Advisory Non-Fatal Error Status RW1CS

i. Corrected Internal Error Status
(For Base 2.x or later testing: Optional-Mask) RW1CS

j. Header Log Overflow Status
(For Base 2.x or later testing: Optional-Mask) RW1CS

k. RsvdZ_31-16
(For Base 2.x or later testing) RO-Zero

l. RsvdZ_31-14
(For Base 1.x testing) RO-Zero

Note: These tests do not apply to those bits marked (Optional-Mask) if the corresponding mask is not implemented as writeable. In that case the bit must be RO-Zero.

Correctable Error Mask Register (Offset 14h) — DWORD

a. Receiver Error Mask (Optional-Mask)
(for VFs) RO-Zero

(otherwise)	RWS or RO-Zero
b. RsvdP_5-1	RO-Zero
c. Bad TLP Mask	
(for VFs)	RO-Zero
(otherwise)	RWS
d. Bad DLLP Mask	
(for VFs)	RO-Zero
(otherwise)	RWS
e. REPLAY_NUM Rollover Mask	
(for VFs)	RO-Zero
(otherwise)	RWS
f. RsvdP_11-9	RO-Zero
g. Replay Timer Timeout Mask	
(for VFs)	RO-Zero
(otherwise)	RWS
h. Advisory Non-Fatal Error Mask	
(for VFs)	RO-Zero
(otherwise)	RWS
i. Corrected Internal Error Mask	
(For Base 2.x or later testing: Optional-Mask)	RWS or RO-Zero
j. Header Log Overflow Mask	
(For Base 2.x or later testing: Optional-Mask)	RWS or RO-Zero
k. RsvdP_31-16	
(For Base 2.x or later testing)	RO-Zero
l. RsvdP_31-14	
(For Base 1.x testing)	RO-Zero

Note: Those bits that are marked (Optional-Mask) are checked to see if they are writeable or non-writeable. If one of those bits is writeable then that specific bit is considered implemented for the Status/Mask registers. Otherwise that specific bit is considered unimplemented for the Status/Mask registers. A writeable bit will be tested as RWS. A non-writeable bit will be tested as RO-Zero.

Advanced Error Capabilities and Control Register (Offset 18h) — DWORD

a. First Error Pointer	ROS
b. ECRC Generation Capable	RO
c. ECRC Generation Enable (Optional)	
(for VFs)	RO-Zero
(for non-VFs with ECRC Generation Capable is 1)	RWS
(for non-VFs with ECRC Generation Capable is 0)	RO-Zero or RWS
d. ECRC Check Capable	RO
e. ECRC Check Enable (Optional)	
(for VFs)	RO-Zero
(for non-VFs with ECRC Check Capable is 1)	RWS

(for non-VFs with ECRC Check Capable is 0)	RO-Zero or RWS
f. RsvdP_31-9	
(For Base 1.x testing)	RO-Zero
g. Multiple Header Recording Capable	
(For Base 2.x or later testing)	RO
h. Multiple Header Recording Enable	
(For Base 2.x or later testing: Optional)	
(if Multiple Header Recording Capable is 1)	RWS
(if Multiple Header Recording Capable is 0)	RO-Zero or RWS
i. TLP Prefix Log Present	
(For Base 2.x or later testing: Optional)	
(if End-End TLP Prefix Supported is 1)	ROS
(if End-End TLP Prefix Supported is 0)	RO-Zero
j. RsvdP_31-12	
(For Base 2.x testing)	RO-Zero
k. Completion Timeout Prefix/Header Log Capable	
(For Base 3.x or later testing)	RO
l. RsvdP_31-13	
(For Base 3.x or later testing)	RO-Zero

Header Log Register (Offset 1Ch) — 4 DWORDS

a. Header Log register (1st DW)	ROS
b. Header Log register (2nd DW)	ROS
c. Header Log register (3rd DW)	ROS
d. Header Log register (4th DW)	ROS

Root Error Command Register (Offset 2Ch) — DWORD

(for Root Port and RC Event Collector)

a. Correctable Error Reporting Enable	RW
b. Non-Fatal Error Reporting Enable	RW
c. Fatal Error Reporting Enable	RW
d. RsvdP_31-3	RO-Zero

Root Error Command Register (Offset 2Ch) — DWORD

(For Base 2.x or later testing)
(for all device types with AER Capability Version of 2h or greater and the End-End TLP Prefix Supported field as 1, except: Root Port, RC Event Collector, PCI Express to PCI/PCI-X Bridge, or PCI/PCI-X to PCI Express Bridge)

a. RsvdP_31-0	RO-Zero

Root Error Status Register (Offset 30h) — DWORD

(for Root Port and RC Event Collector)

a. ERR_COR Received	RW1CS
b. Multiple ERR_COR Received	RW1CS
c. ERR_FATAL/NONFATAL Received	RW1CS
d. Multiple ERR_FATAL/NONFATAL Received	RW1CS
e. First Uncorrectable Fatal	RW1CS
f. Non-Fatal Error Messages Received	RW1CS

g. Fatal Error Messages Received RW1CS
h. RsvdZ_26-7 RO-Zero
i. Advanced Error Interrupt Message Number RO

Root Error Status Register (Offset 30h) — DWORD

(For Base 2.x or later testing)
(for all device types with AER Capability Version of 2h or greater and the End-End TLP Prefix Supported field as 1, except: Root Port, RC Event Collector, PCI Express to PCI/PCI-X Bridge, or PCI/PCI-X to PCI Express Bridge)

a. RsvdZ_31-0 RO-Zero

Error Source Identification Register (Offset 34h) — DWORD

(for Root Port and RC Event Collector)

a. ERR_COR Source Identification ROS
b. ERR_FATAL/NONFATAL Source Identification ROS

Error Source Identification Register (Offset 34h) — DWORD

(For Base 2.x or later testing)
(for all device types with AER Capability Version of 2h or greater and the End-End TLP Prefix Supported field as 1, except: Root Port, RC Event Collector, PCI Express to PCI/PCI-X Bridge, or PCI/PCI-X to PCI Express Bridge)

a. RsvdP_31-0 RO-Zero

TLP Prefix Log Register (Offset 38h) — 4 DWORDS

(For Base 2.x or later testing)
(for all device types with AER Capability Version of 2h or greater and the End-End TLP Prefix Supported field as 1, except: PCI Express to PCI/PCI-X Bridge, or PCI/PCI-X to PCI Express Bridge)

a. TLP Prefix Log register (1st DW) ROS
b. TLP Prefix Log register (2nd DW) ROS
c. TLP Prefix Log register (3rd DW) ROS
d. TLP Prefix Log register (4th DW) ROS

Secondary Uncorrectable Error Status Register (Offset 2Ch) — DWORD

(for PCI Express to PCI/PCI-X Bridge or PCI/PCI-X to PCI Express Bridge)

a. Target-Abort on Split Completion Status (Optional-Mask) RW1CS
b. Master-Abort on Split Completion Status RW1CS
c. Received Target-Abort Status (Optional-Mask) RW1CS
d. Received Master-Abort Status RW1CS
e. RsvdZ_4 RO-Zero
f. Unexpected Split Completion Error Status RW1CS
g. Uncorrectable Split Completion Message Data Error Status RW1CS
h. Uncorrectable Data Error Status RW1CS
i. Uncorrectable Attribute Error Status RW1CS
j. Uncorrectable Address Error Status RW1CS
k. Delayed Transaction Discard Timer Expired Status RW1CS
l. PERR# Assertion Detected RW1CS
m. SERR# Assertion Detected RW1CS
n. Internal Bridge Error Status RW1CS
o. RsvdZ_31-14 RO-Zero

Note: These tests do not apply to those bits marked (Optional-Mask) if the corresponding mask is not implemented as writeable. In that case the bit must be RO-Zero.

Secondary Uncorrectable Error Mask Register (Offset 30h) — DWORD

(for PCI Express to PCI/PCI-X Bridge or PCI/PCI-X to PCI Express Bridge)

a. Target-Abort on Split Completion Mask (Optional-Mask)	RWS or RO-Zero
b. Master-Abort on Split Completion Mask	RWS
c. Received Target-Abort Mask (Optional-Mask)	RWS or RO-Zero
d. Received Master-Abort Mask	RWS
e. RsvdP_4	RO-Zero
f. Unexpected Split Completion Error Mask	RWS
g. Uncorrectable Split Completion Message Data Error Mask	RWS
h. Uncorrectable Data Error Mask	RWS
i. Uncorrectable Attribute Error Mask	RWS
j. Uncorrectable Address Error Mask	RWS
k. Delayed Transaction Discard Timer Expired Mask	RWS
l. PERR# Assertion Detected Mask	RWS
m. SERR# Assertion Detected Mask	RWS
n. Internal Bridge Error Mask	RWS
o. RsvdP_31-14	RO-Zero

Note: Those bits that are marked (Optional-Mask) are checked to see if they are writeable or non-writeable. If one of those bits is writeable then that specific bit is considered implemented for the Status/Mask/Severity registers. Otherwise that specific bit is considered unimplemented for the Status/Mask/Severity registers. A writeable bit will be tested as RWS. A non-writeable bit will be tested as RO-Zero.

Secondary Uncorrectable Error Severity Register (Offset 34h) — DWORD

(for PCI Express to PCI/PCI-X Bridge or PCI/PCI-X to PCI Express Bridge)

a. Target-Abort on Split Completion Severity (Optional-Mask)	RWS
b. Master-Abort on Split Completion Severity	RWS
c. Received Target-Abort Severity (Optional-Mask)	RWS
d. Received Master-Abort Severity	RWS
e. RsvdP_4	RO-Zero
f. Unexpected Split Completion Error Severity	RWS
g. Uncorrectable Split Completion Message Data Error Severity	RWS
h. Uncorrectable Data Error Severity	RWS
i. Uncorrectable Attribute Error Severity	RWS
j. Uncorrectable Address Error Severity	RWS
k. Delayed Transaction Discard Timer Expired Severity	RWS
l. PERR# Assertion Detected Severity	RWS
m. SERR# Assertion Detected Severity	RWS
n. Internal Bridge Error Severity	RWS
o. RsvdP_31-14	RO-Zero

Note: These tests do not apply to those bits marked (Optional-Mask) if the corresponding mask is not implemented as writeable. In that case the bit must be RO-Zero.

Secondary Error Capabilities and Control Register (Offset 38h) — DWORD

(for PCI Express to PCI/PCI-X Bridge or PCI/PCI-X to PCI Express Bridge)

a. Secondary Uncorrectable First Error Pointer — ROS
b. RsvdP_31-5 — RO-Zero

Secondary Header Log Register (Offset 3Ch) — 4 DWORDS

(for PCI Express to PCI/PCI-X Bridge or PCI/PCI-X to PCI Express Bridge)

a. Transaction Attribute — ROS
b. Transaction Command Lower — ROS
c. Transaction Command Upper — ROS
d. RsvdZ_63-44 — RO-Zero
e. Transaction Address — ROS

29. The following default value checks are performed:

Uncorrectable Error Status Register Default Value (Offset 04h) –– DWORD

a. Data Link Protocol Error Status
 (for non-VFs) — 0
b. Surprise Down Error Status (Optional)
 (for Downstream Ports with Surprise Down Error Capable as 1) — 0
c. Poisoned TLP Received Status — 0
d. Flow Control Protocol Error Status (Optional-Mask)
 (for non-VFs) — 0
e. Completion Timeout Status
 (for any device other than a Switch Port) — 0
f. Completer Abort Status (Optional-Mask) — 0
g. Unexpected Completion Status — 0
h. Receiver Overflow Status (Optional-Mask)
 (for non-VFs) — 0
i. Malformed TLP Status
 (for non-VFs) — 0
j. ECRC Error Status (Optional)
 (for non-VFs with ECRC Check Capable is 1) — 0
k. Unsupported Request Error Status — 0
l. ACS Violation Status (Optional)
 (for Downstream Ports with ACS Extended Capability) — 0
 (for Upstream Ports in single function device that is a PF
 with ACS P2P Egress Control as 1) — 0
 (for Upstream Ports in multi-function device
 with ACS P2P Egress Control as 1) — 0
m. Uncorrectable Internal Error Status
 (For Base 2.x or later testing: Optional-Mask) — 0
n. MC Blocked TLP Status
 (For Base 2.x or later testing: Optional)
 (for any function with Multicast Extended Capability) — 0
o. AtomicOp Egress Blocked Status
 (For Base 2.x or later testing: Optional)
 (if AtomicOp Routing Supported is 1) — 0
p. TLP Prefix Blocked Error Status

(For Base 2.x or later testing: Optional)
(for Root Ports and Switch Ports,
with End-End TLP Prefix Supported as 1) 0

q. Poisoned TLP Egress Blocked Status
(For Base 3.x or later testing: Optional)
(for Root Ports and Switch Downstream Ports,
with Poisoned TLP Egress Blocking Supported as 1) 0

Note: These tests do not apply to those bits marked (Optional-Mask) if the corresponding mask is not implemented as writeable. In that case the default value is not checked.

Uncorrectable Error Mask Register Default Value (Offset 08h) –– DWORD

a. Data Link Protocol Mask
(for non-VFs) 0

b. Surprise Down Error Mask (Optional)
(for Downstream Ports with Surprise Down Error Capable as 1) 0

c. Poisoned TLP Received Mask
(for non-VFs) 0

d. Flow Control Protocol Error Mask (Optional-Mask)
(for non-VFs) 0

e. Completion Timeout Mask
(for any non-VF device other than a Switch Port) 0

f. Completer Abort Mask (Optional-Mask)
(for non-VFs) 0

g. Unexpected Completion Mask
(for non-VFs) 0

h. Receiver Overflow Mask (Optional-Mask)
(for non-VFs) 0

i. Malformed TLP Mask
(for non-VFs) 0

j. ECRC Error Mask (Optional)
(for non-VFs with ECRC Check Capable is 1) 0

k. Unsupported Request Error Mask
(for non-VFs) 0

l. ACS Violation Mask (Optional)
(for Downstream Ports with ACS Extended Capability) 0
(for non-VF Upstream Ports in single function device that is a PF
with ACS P2P Egress Control as 1) 0
(for non-VF Upstream Ports in multi-function device
with ACS P2P Egress Control as 1) 0

m. Uncorrectable Internal Error Mask
(For Base 2.x or later testing: Optional-Mask) 1

n. MC Blocked TLP Mask
(For Base 2.x or later testing: Optional)
(for any function with Multicast Extended Capability) 0

o. AtomicOp Egress Blocked Mask
(For Base 2.x or later testing: Optional)
(if AtomicOp Routing Supported is 1) 0

p. TLP Prefix Blocked Error Mask

(For Base 2.x or later testing: Optional)
(for Root Ports and Switch Ports,
with End-End TLP Prefix Supported as 1) 0

q. Poisoned TLP Egress Blocked Mask
(For Base 3.x or later testing: Optional)
(for Root Ports and Switch Downstream Ports,
with Poisoned TLP Egress Blocking Supported as 1) 1

Note: These tests do not apply to those bits that are marked (Optional-Mask) if the bit is not implemented as writeable. In that case the default value is not checked.

Uncorrectable Error Severity Register Default Value (Offset 0Ch) — DWORD

a. Data Link Protocol Error Severity
(for non-VFs) 1

b. Surprise Down Error Severity (Optional)
(for Downstream Ports with Surprise Down Error Capable as 1) 1

c. Poisoned TLP Received Severity
(for non-VFs) 0

d. Flow Control Protocol Error Severity (Optional-Mask)
(for non-VFs) 1

e. Completion Timeout Severity
(for any non-VF device other than a Switch Port) 0

f. Completer Abort Error Severity (Optional-Mask)
(for non-VFs) 0

g. Unexpected Completion Severity
(for non-VFs) 0

h. Receiver Overflow Severity (Optional-Mask)
(for non-VFs) 1

i. Malformed TLP Severity
(for non-VFs) 1

j. ECRC Error Severity (Optional)
(for non-VFs with ECRC Check Capable is 1) 0

k. Unsupported Request Error Severity
(for non-VFs) 0

l. ACS Violation Severity (Optional)
(for Downstream Ports with ACS Extended Capability) 0
(for Upstream Ports in single function device that is a PF
with ACS P2P Egress Control as 1) 0
(for Upstream Ports in multi-function device
with ACS P2P Egress Control as 1) 0

m. Uncorrectable Internal Error Severity (Optional-Mask)
(For Base 2.x or later testing) 1

n. MC Blocked TLP Severity (Optional)
(For Base 2.x or later testing)
(for any function with Multicast Extended Capability) 0

o. AtomicOp Egress Blocked Severity (Optional)
(For Base 2.x or later testing)
(if AtomicOp Routing Supported is 1) 0

p. TLP Prefix Blocked Error Severity (Optional)

(For Base 2.x or later testing)
(for Root Ports and Switch Ports,
with End-End TLP Prefix Supported as 1) 0

q. Poisoned TLP Egress Blocked Severity (Optional)
(For Base 3.x or later testing)
(for Root Ports and Switch Downstream Ports,
with Poisoned TLP Egress Blocking Supported as 1) 0

Note: These tests do not apply to those bits that are marked (Optional-Mask) if the corresponding mask is not implemented as writeable. In that case the default value is not checked.

Correctable Error Status Register Default Value (Offset 10h) — DWORD

a. Receiver Error Status (Optional-Mask)
(for non-VFs) 0
b. Bad TLP Status
(for non-VFs) 0
c. Bad DLLP Status
(for non-VFs) 0
d. REPLAY_NUM Rollover Status
(for non-VFs) 0
e. Replay Timer Timeout Status
(for non-VFs) 0
f. Advisory Non-Fatal Error Status 0
g. Corrected Internal Error Status
(For Base 2.x or later testing: Optional-Mask) 0
h. Header Log Overflow Status
(For Base 2.x or later testing: Optional-Mask) 0

Note: These tests do not apply to those bits marked (Optional-Mask) if the corresponding mask is not implemented as writeable. In that case the default value is not checked.

Correctable Error Mask Register Default Value (Offset 14h) — DWORD

a. Receiver Error Mask (Optional-Mask)
(for non-VFs) 0
b. Bad TLP Mask
(for non-VFs) 0
c. Bad DLLP Mask
(for non-VFs) 0
d. REPLAY_NUM Rollover Mask
(for non-VFs) 0

e. Replay Timer Timeout Mask
(for non-VFs) 0
f. Advisory Non-Fatal Error Mask
(for non-VFs) 1
g. Corrected Internal Error Mask
(For Base 2.x or later testing: Optional-Mask) 1
h. Header Log Overflow Mask
(For Base 2.x or later testing: Optional-Mask) 1

Note: These tests do not apply to those bits that are marked (Optional-Mask) if the bit is not implemented as writeable. In that case the default value is not checked.

Advanced Error Capabilities and Control Register Default Value (Offset 18h) — DWORD

a. ECRC Generation Enable (Optional)
 (for non-VFs with ECRC Generation Capable is 1) 0
b. ECRC Check Enable (Optional)
 (for non-VFs with ECRC Check Capable is 1) 0
c. Multiple Header Recording Enable
 (For Base 2.x or later testing: Optional)
 (if Multiple Header Recording Capable is 1) 0
d. TLP Prefix Log Present
 (For Base 2.x or later testing: Optional)
 (if End-End TLP Prefix Supported is 1) 0

Root Error Command Register Default Value (Offset 2Ch) — DWORD

(for Root Port and RC Event Collector)

a. Correctable Error Reporting Enable 0
b. Non-Fatal Error Reporting Enable 0
c. Fatal Error Reporting Enable 0

Root Error Status Register Default Value (Offset 30h) — DWORD

(for Root Port and RC Event Collector)

a. ERR_COR Received 0
b. Multiple ERR_COR Received 0
c. ERR_FATAL/NONFATAL Received 0
d. Multiple ERR_FATAL/NONFATAL Received 0
e. First Uncorrectable Fatal 0
f. Non-Fatal Error Messages Received 0
g. Fatal Error Messages Received 0

Error Source Identification Register Default Value (Offset 34h) — DWORD

(for Root Port and RC Event Collector)

a. ERR_COR Source Identification 0000h
b. ERR_FATAL/NONFATAL Source Identification 0000h

Secondary Uncorrectable Error Status Register Default Value (Offset 2Ch) — DWORD

(for PCI Express to PCI/PCI-X Bridge or PCI/PCI-X to PCI Express Bridge)

a. Target-Abort on Split Completion Status (Optional-Mask) 0
b. Master-Abort on Split Completion Status 0
c. Received Target-Abort Status (Optional-Mask) 0
d. Received Master-Abort Status 0
e. Unexpected Split Completion Error Status 0
f. Uncorrectable Split Completion Message Data Error Status 0
g. Uncorrectable Data Error Status 0
h. Uncorrectable Attribute Error Status 0
i. Uncorrectable Address Error Status 0
j. Delayed Transaction Discard Timer Expired Status 0
k. PERR# Assertion Detected 0
l. SERR# Assertion Detected 0

m. Internal Bridge Error Status 0

Note: These tests do not apply to those bits marked (Optional-Mask) if the corresponding mask is not implemented as writeable. In that case the default value is not checked.

Secondary Uncorrectable Error Mask Register Default Value (Offset 30h) — DWORD

(for PCI Express to PCI/PCI-X Bridge or PCI/PCI-X to PCI Express Bridge)

a. Target-Abort on Split Completion Mask (Optional-Mask) 0
b. Master-Abort on Split Completion Mask 0
c. Received Target-Abort Mask (Optional-Mask) 0
d. Received Master-Abort Mask 1
e. Unexpected Split Completion Error Mask 1
f. Uncorrectable Split Completion Message Data Error Mask 0
g. Uncorrectable Data Error Mask 1
h. Uncorrectable Attribute Error Mask 1
i. Uncorrectable Address Error Mask 1
j. Delayed Transaction Discard Timer Expired Mask 1
k. PERR# Assertion Detected Mask 0
l. SERR# Assertion Detected Mask 1
m. Internal Bridge Error Mask 0

Note: These tests do not apply to those bits that are marked (Optional-Mask) if the bit is not implemented as writeable. In that case the default value is not checked.

Secondary Uncorrectable Error Severity Register Default Value (Offset 34h) — DWORD

(for PCI Express to PCI/PCI-X Bridge or PCI/PCI-X to PCI Express Bridge)

a. Target-Abort on Split Completion Severity (Optional-Mask) 0
b. Master-Abort on Split Completion Severity 0
c. Received Target-Abort Severity (Optional-Mask) 0
d. Received Master-Abort Severity 0
e. Unexpected Split Completion Error Severity 0
f. Uncorrectable Split Completion Message Data Error Severity 1
g. Uncorrectable Data Error Severity 0
h. Uncorrectable Attribute Error Severity 1
i. Uncorrectable Address Error Severity 1
j. Delayed Transaction Discard Timer Expired Severity 0
k. PERR# Assertion Detected Severity 0
l. SERR# Assertion Detected Severity 1
m. Internal Bridge Error Severity 0

Note: These tests do not apply to those bits marked (Optional-Mask) if the corresponding mask is not implemented as writeable. In that case the default value is not checked.

30. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

31. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- More than one Advanced Error Reporting Extended Capability structure is present.
- An RCRB contains an Advanced Error Reporting Extended Capability structure.
- A Root Port or a Root Complex Event Collector does not implement the Root Error Command, Root Error Status, or Error Source Identification registers.
- The Capability Version field does not report 2h or 1h (if End-End TLP Prefixes not supported).
- The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- Any of the defined bits in the Uncorrectable Error Status register report an error (after standard configuration performed by the test).
- A required bit in the Uncorrectable Error Mask register cannot be set.
- A required bit in the Uncorrectable Error Severity register cannot be set.
- Any of the defined bits in the Correctable Error Status register report an error (after standard configuration performed by the test).
- A required bit in the Correctable Error Mask register cannot be set.
- ECRC Check Capable is 1 and the ECRC Check Enable field is not writeable.
- ECRC Generation Capable is 1 and the ECRC Generation Enable field is not writeable.
- Multiple Header Recording Capable is 1 and the Multiple Header Recording Enable field is not writeable (for Base 2.x or later testing only).
- A Root Port or a Root Complex Event Collector has the Root Error Status register report an error.
- A Root Port or a Root Complex Event Collector has the Error Source Identification register report an error.
- A Bridge has any of the defined bits in the Secondary Uncorrectable Error Status register report an error (after standard configuration performed by the test).
- A Bridge has a required bit in the Secondary Uncorrectable Error Mask register that cannot be set.
- A Bridge has a required bit in the Secondary Uncorrectable Error Severity register that cannot be set.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

The test *warns* if:

- A non-RCRB device type that supports ACS, and the Advanced Error Reporting Extended Capability structure is not present.

- A non-RCRB device type that supports Multicast, and the Advanced Error Reporting Extended Capability structure is not present.
- Completion Timeout Prefix/Header Log Capable is 0(for Base 3.x or later testing only).

2.2.13. TD_1_8 Virtual Channel Extended Capability Structure

The test verifies that if the function under test reports a PCI Express Virtual Channel Extended Capability structure, it is implemented as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *Single Root I/O Virtualization and Sharing Specification (Base 3.x or earlier only)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of either the Extended Capability ID of 0002h (Virtual Channel Extended Capability) or the Extended Capability ID of 0009h (Virtual Channel Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Extended Capability ID of 0002h is found in an Extended Capability structure for a VF, the test terminates with a failure.
4. If the Extended Capability ID of 0009h is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
5. If the Extended Capability ID of 0009h is found in an Extended Capability structure for a VF, the test terminates with a failure.
6. If the Extended Capability ID of 0002h or if the Extended Capability ID of 0009h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0002h or the Extended Capability ID of 0009h is not found in an Extended Capability structure, the test skips to step 23.
7. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.

8. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
9. Test software reads the DWORD at offset 04h (Port VC Capability Register 1) and performs the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The Low Priority Extended VC Count field is less than or equal to the Extended VC Count field value.
 b. The Reference Clock field must be 00b.
10. Set the Number of Virtual Channels [NVC] to the value in the Extended VC Count field.
11. Test software reads the DWORD from offset 08h (Port VC Capability Register 2 register) and performs the following checks:
 a. No reserved bits (4-7) in the VC Arbitration Capability field are set. If not, this is recorded as a failure, but the test continues.
 b. The VC Arbitration Capability field must not be zero, if the Low Priority Extended VC Count field value is non-zero. If not, this is recorded as a failure, but the test continues.
 c. The VC Arbitration Capability field must be zero, if the Low Priority Extended VC Count field value is zero. If not, this is recorded as a failure, but the test continues.
 d. The VC Arbitration Table Offset field should not be zero, if any of bits 1, 2, or 3 of the VC Arbitration Capability field are set. If not, the test logs a warning, but the test continues.
 e. (VC Arbitration Table Offset field value * 4) must be greater than (4 + (3 * (Extended VC Count field value + 1))), if the VC Arbitration Table Offset field is non-zero. If not, this is recorded as a failure, but the test continues.
12. Test software reads the DWORD from offset 0Ch (Port VC Control register and Port VC Status register) and performs the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The VC Arbitration Table Status field returns zero.
13. For non-FLR testing only, if the VC Arbitration Table Offset field is non-zero and the default VC Arbitration Select field value is a WRR based arbitration method test software reads the default values in the VC Arbitration table. These values must all be zero. If not, this is recorded as a failure, but the test continues.
14. Test software writes each of the supported data values indicated by the VC Arbitration Capability field value to the VC Arbitration Select field and verifies the value is read back. If not correct this is recorded as a failure, but the test continues.
15. If the VC Arbitration Table Offset field is non-zero, test software performs the following:
 a. For each supported WRR arbitration field mechanism, test software tests loading the table by writing a table of all zeroes of the appropriate size to the indicated VC Arbitration table offset. Test software then checks that the VC Arbitration Table Status field returns 1. If not, this is recorded as a failure and the test skips to step 16. Test software then writes 1 to the Load VC Arbitration Table field, while preserving all the other fields in this register.. Test software then reads the VC Arbitration Table Status field repeatedly until it returns 0. If it does not return 0 within 1 second, the test fails and this is recorded as a failure, but the test continues.
16. Step 15 is repeated using all VC entries for the highest supported VC instead of zero.
17. Test software verifies that VC Resource Control, VC Resource Status, and VC Resource Capability registers are present for each VC supported by the function (from 0 to [NVC]).

18. For each set of VC Resource Control, VC Resource Status, and VC Resource Capability registers (from 0 to [NVC]), test software performs the following checks:
 a. The Port Arbitration Capability field: for a Switch Port or RCRB it must not have bit 6 or 7 set (reserved). If not, this is recorded as a failure, but the test continues.
 b. The Port Arbitration Table Offset field: for a Switch Port or RCRB it should be non-zero, if any of bits 1, 2, 3, 4, or 5 of the Port Arbitration Capability field are set. If not, the test logs a warning, but the test continues.
 c. (Port Arbitration Table Offset field value * 4): for a Switch Port or RCRB it must be greater than (4 + (3 * (Extended VC Count field value + 1))), if the Port Arbitration Table Offset field is non-zero. If not, this is recorded as a failure, but the test continues.
 d. For non-FLR testing only, the TC/VC Map field must be FFh for the first VC resource (VC0) by default. For all other VCs it must be 00h by default. Test software writes each valid TC combination to this field and ensures that the same value can be read back, with the exception of bit 0 which is RO=1 for the first VC resource (VC0) and RO=0 for all other VCs. If not, this is recorded as a failure, but the test continues.
 Note: This default value restriction does not apply to an RCRB.
 e. The Load Port Arbitration Table field: for a Switch Port or RCRB it must be zero. If not, this is recorded as a failure, but the test continues.
 f. The Port Arbitration Select field: for a Switch Port or RCRB – Test software writes each supported data value (based on the Port Arbitration Capability field value) and ensures that the same value is read back. If not, this is recorded as a failure, but the test continues.
 g. The VC-ID field: test software ensures that the value is hard-wired to 000b for the first VC resource (VC0).
 h. The VC Enable field: test software checks that this field is hardwired to one for the first VC resource (VC0). If not, this is recorded as a failure, but the test continues.
 i. The Port Arbitration Table Status field: for a Switch Port or RCRB it must be zero. If not, this is recorded as a failure, but the test continues.

19. If the Port Arbitration Table Offset field is non-zero, test software performs the following:
 a. For each supported WRR based Port Arbitration scheme test software writes a table with all values of the minimum port number. After the first write to the table, test software checks that the Port Arbitration Table Status field returns 1. If not, this is recorded as a failure and the test skips to step 20. Test software writes 1 to the Load Port Arbitration Table field, while preserving all the other fields in this register. Test software then reads the Port Arbitration Table Status field repeatedly until it returns 0. If it does not return 0 within 1 second, the test fails and this is recorded as a failure, but the test continues.

20. Step 19 is repeated with a valid arbitration table containing all ports.

21. The following register field characteristic checks are performed:

Virtual Channel Extended Capability Header (Offset 00h) –– DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

Port VC Capability Register 1 (Offset 04h) –– DWORD

a. Extended VC Count	RO
b. RsvdP_3	RO-Zero
c. Low Priority Extended VC Count	RO

d. RsvdP_7 RO-Zero
e. Reference Clock RO
f. Port Arbitration Table Entry Size
(for Endpoints) RO-Zero
(for non-Endpoints) RO
g. RsvdP_31-12 RO-Zero

Port VC Capability Register 2 (Offset 08h) — DWORD

a. VC Arbitration Capability RO
b. RsvdP_23-8 RO-Zero
c. VC Arbitration Table Offset RO

Port VC Control Register (Offset 0Ch) — WORD

a. Load VC Arbitration Table RO-Zero
b. VC Arbitration Select
(if more than one VC in the LPVC group is not enabled)
(for non-FLR testing) RW
(for FLR testing) RWS
(if more than one VC in the LPVC group is enabled) RO
(only those values in VC Arbitration Capability are written)
c. RsvdP_15-4 RO-Zero

Port VC Status Register (Offset 0Eh) — WORD

a. VC Arbitration Table Status RO
b. RsvdZ_15-1 RO-Zero

22. For each VC Resource register set instance Number [n] (from 0 to [NVC]), the following register field characteristic checks and register field default value checks are performed:

VC Resource Capability Register (n) (Offset 10h + n * 0Ch) — DWORD

a. Port Arbitration Capability RO
b. RsvdP_13-8 RO-Zero
c. Undefined_14 RO
Note: This was once Advanced Packet Switching.
d. Reject Snoop Transactions
(for non-FLR testing) HwInit
(for FLR testing) RO
e. Maximum Time Slots
(for non-FLR testing) HwInit
(for FLR testing) RO
f. RsvdP_23 RO-Zero
g. Port Arbitration Table Offset RO

VC Resource Control Register (n) (Offset 14h + n * 0Ch) — DWORD

a. TC/VC Map
(for VC0: bit 0) RO-Ones
(for non-VC0: bit 0) RO-Zero
(bits 7-1)
(for non-FLR testing) RW
(for FLR testing) RWS
b. RsvdP_15-8 RO-Zero

c. Load Port Arbitration Table — RO-Zero
d. Port Arbitration Select
 (for non-FLR testing) — RW
 (for FLR testing) — RWS
 (only those values reported in Port Arbitration Capability are written)
e. RsvdP_23-20 — RO-Zero
f. VC ID
 (for VC0) — RO-Zero
 (for all non VC0)
 (for non-FLR testing) — RW
 (for FLR testing) — RWS
g. RsvdP_30-27 — RO-Zero
h. VC Enable
 (for VC0) — RO
 (for all non-VC0)
 (for non-FLR testing) — RW
 (for FLR testing) — RWS

Reserved Register (n) (Offset 18h + n * 0Ch) — WORD

a. RsvdP_15-0 — RO-Zero

VC Resource Status Register (n) (Offset 1Ah + n * 0Ch) — WORD

a. Port Arbitration Table Status — RO
b. VC Negotiation Pending — RO
c. RsvdZ_15-2 — RO-Zero

VC Resource Control Register (n) Default Value (Offset 14h + n * 0Ch) – DWORD

a. TC/VC Map
 (for VC0) — FFh
 (for all non VC0) — 00h
b. VC Enable
 (for VC0) — 1
 (for all non-VC0) — 0

23. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
24. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one Virtual Channel Extended Capability structure is present.
- ❑ A VF contains a Virtual Channel Extended Capability structure with Extended Capability ID of 0002h or 0009h.

- An RCRB contains a Virtual Channel Extended Capability structure with Extended Capability ID of 0009h.
- The Capability Version field does not report 1h.
- The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- The Low Priority Extended VC Count field is greater than the Extended VC Count field (Port VC Capability Register 1).
- The Reference Clock field is non-zero (Port VC Capability Register 1).
- The VC Arbitration Capability field contains a reserved value.
- The VC Arbitration Capability field contains a zero value and the Low Priority Extended VC Count field is non-zero.
- The VC Arbitration Capability field contains a non-zero value and the Low Priority Extended VC count field is zero.
- The VC Arbitration Table Offset field value is too small when the VC Arbitration Table Offset is non-zero.
- The VC Arbitration Table Status field reads non-zero by default.
- The default VC Arbitration Select field value is a WRR based arbitration method and the non-FLR default VC Arbitration table values are not all zero when the VC Arbitration Table Offset is non-zero.
- A valid VC Arbitration Select field value cannot be written.
- The VC Arbitration table cannot be written when the VC Arbitration Table Offset is non-zero.
- VC Resource Control, VC Resource Status, and VC Resource Capability registers are not present for each VC supported by the function (as indicated by Extended VC Count field).
- Any of the described VC Resource Control and VC Resource Status register value checks are not met:
 - For a Switch Port or RCRB, the Port Arbitration Capability field contains a reserved value
 - For a Switch Port or RCRB, the Port Arbitration Table Offset field value is too small when the Port Arbitration Table Offset field is non-zero
 - The TC/VC Map field non-FLR default value is not FFh for VC0
 - The TC/VC Map field non-FLR default value is not 00h for any VCn other than VC0
 - The VC_ID field is not 000b for VC0
 - The VC Enable field is not 1 for VC0
 - For a Switch Port or RCRB, a valid Port Arbitration Select field value cannot be written
 - For a Switch Port or RCRB, the Port Arbitration Table Status field reads non-zero by default.
 - The Port Arbitration table cannot be written when the Port Arbitration Table Offset field is non-zero.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

The test *warns* if:

- ❑ The VC Arbitration Table Offset field is zero when WRR based VC Arbitration Capabilities are supported.
- ❑ Any of the described VC Resource Control and VC Resource Status register value checks are not met:
 - For a Switch Port or RCRB, the Port Arbitration Table Offset field is zero when WRR based Port Arbitration Capabilities are supported.

2.2.14. TD_1_9 Device Serial Number Extended Capability Structure

The test verifies that if the function under test reports a PCI Express Device Serial Number Extended Capability structure, it is implemented as defined in the relevant specifications.

Relevant Specifications

- ❑ *PCI Express Base Specification*
- ❑ *Single Root I/O Virtualization and Sharing Specification (Base 3.x or earlier only)*
- ❑ *ECN SR-IOV Table Updates (to SR-IOV 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0003h (Device Serial Number Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Extended Capability ID of 0003h is found in an Extended Capability structure for a VF, the test logs a warning, but the test continues.
4. If the Extended Capability ID of 0003h is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
5. If the Extended Capability ID of 0003h is found in an Extended Capability structure for device type that is a Root Complex Integrated Endpoint, the test logs a warning, but the test continues.

6. If the Extended Capability ID of 0003h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0003h is not found in an Extended Capability structure, the test skips to step 12.
7. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
8. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
9. The DWORD at offset 04h (Serial Number register Lower DW) is read. The test logs a warning if the value is zero, but the test continues.
10. The DWORD at offset 08h (Serial Number register Upper DW) is read. The test logs a warning if the value is zero, but the test continues.
11. The following register field characteristic checks are performed:

Device Serial Number Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID RO
b. Capability Version RO
c. Next Capability Offset RO

Serial Number Register (Offset 04h) — 2 DWORDS

a. Serial Number register (Lower DW) RO
b. Serial Number register (Upper DW) RO

12. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
13. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one Device Serial Number Extended Capability structure is present.
- ❑ An RCRB contains a Device Serial Number Extended Capability structure.
- ❑ The Capability Version field does not report 1h.
- ❑ The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- ❑ Any of the register field characteristic tests fail.

The test *warns* if:

- ❑ A VF contains a Device Serial Number Extended Capability structure.
- ❑ A Root Complex Integrated Endpoint contains a Device Serial Number Extended Capability structure.

- Either of the Serial Number registers read zero.

2.2.15. TD_1_10 Power Budgeting Extended Capability Structure

The test verifies that if the function under test reports a PCI Express Power Budgeting Extended Capability structure, it is implemented as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *Single Root I/O Virtualization and Sharing Specification (Base 3.x or earlier only)*
- *ECN Emergency Power Reduction mechanism with PWRBRK signal (to Base 3.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0004h (Power Budgeting Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Extended Capability ID of 0004h is found in an Extended Capability structure for a VF, the test terminates with a failure.
4. If the Extended Capability ID of 0004h is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
5. If the Extended Capability ID of 0004h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0004h is not found in an Extended Capability structure, the test skips to step 19.
6. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
7. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
8. Set the Data Select Value [DSV] to 00h.
9. Test software writes the [DSV] value to the Data Select register.

10. Test software reads a DWORD from offset 8h (Data register).
11. If the returned Data register value is non-zero, test software performs the following checks on the Data register and if any are not as stated, this is recorded as a failure, but the test continues:
 a. Test software checks that the Power Rail field is one of the defined values (000b, 001b, 010b, or 111b).
 b. For Base 3.0 or earlier testing: test software checks that the Type field of the Power Budgeting data is one of the defined values (000b, 001b, 010b, 011b, or 111b).
 c. For Base 3.1 or later testing: test software checks that the Type field of the Power Budgeting data is one of the defined values (000b, 001b, 010b, 011b, 100b, 101b, or 111b).
 d. Test software records the PM State and Type fields for Power Budgeting data.
 e. If the Data Scale field is 00b then the Base Power field must not be F3h to FFh.
12. Test software increments [DSV] by 1 and repeats steps 9-12. Test software continues repeating until the Data register returns 0000 0000h, or until [DSV] exceeds FFh. The value written to the Data Select register for the instance when the Data register first returns 0000 0000h determines the Out of Bound Index [OBI] which is recorded. If the Data register does not return 0000 0000h before [DSV] exceeds FFh, then [OBI] is set to 100h.
13. If [DSV] does not yet exceed FFh, test software increments [DSV] by 1 and repeats steps 9, 10, 13, but now checks that the Data register only returns 0000 0000h. If the Data register does not return 0000 0000h, this is recorded as a failure, but the test continues. Test software continues repeating until [DSV] exceeds FFh.
14. Test software checks that at least one of the recorded Power Budget data values contains the following information for each value of Power Rail that was recorded from the device and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The PM State field is equal to 00b (D0) and the Type field is equal to 111b (Maximum).
 b. The PM State field is equal to 00b (D0) and the Type field is equal to 011b (Sustained).
15. If Emergency Power Reduction Supported is not 00b (Device Capabilities 2 register): test software checks that at least one of the recorded Power Budget data values contains the following information for each value of Power Rail that was recorded from the device and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The PM State field is equal to 00b (D0) and the Type field is equal to 101b (Maximum – Emergency Power Reduction State).
 b. The PM State field is equal to 00b (D0) and the Type field is equal to 100b (Sustained – Emergency Power Reduction State).
16. Test software repeats steps 9-15 with the [DSV] value written to the Data Select register in inverse order (starting with [OBI]-1 and decrementing to 00h). The returned information must be the same. If not, this is recorded as a failure, but the test continues.
17. If [OBI] is equal to or less than FFh, test software repeats steps 9-15 with the [DSV] value written to the Data Select register starting with [OBI] for the first access, and then using 00h for the second access, incrementing which each access up to [OBI]-1. The returned information must be the same. If not, this is recorded as a failure, but the test continues.
18. The following register field characteristic checks are performed:

Power Budgeting Extended Capability Header (Offset 00h) –– DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO

c. Next Capability Offset RO

Data Select Register (Offset 04h) — BYTE

a. Data Select RW

Reserved Register (Offset 05h) — 3 BYTES

a. RsvdP_23-0 RO-Zero

Data (n) Register (Offset 08h) — DWORD

Data Select register is written with value (n) prior to this register test. This test is then repeated for all values of (n) = 00h to ([OBI]-1) where [OBI] is the first Data Select value that returns all zeroes in the Data register.

a. Base Power RO
b. Data Scale RO
c. PM Sub State RO
d. PM State RO
e. Type RO
f. Power Rail RO
g. RsvdP_31-21 RO-Zero

Note: Since the Data Select register is not sticky, it must be re-written following any Reset Sequence (described in Section 2.1.1.1) being executed while testing this register.

Data (n) Register (Offset 08h) — DWORD

If [OBI] is less than or equal to FFh, then Data Select register is written with value (n) prior to this register test. This test is then repeated for all values of (n) = [OBI] to FFh where [OBI] is the first Data Select value that returns all zeroes in the Data register.

a. RsvdP_31-0 RO-Zero

Note: Since the Data Select register is not sticky, it must be re-written following any Reset Sequence (described in Section 2.1.1.1) being executed while testing this register.

Power Budget Capability Register (Offset 0Ch) — BYTE

a. System Allocated
 (for non-FLR testing) HwInit
 (for FLR testing) RO
b. RsvdP_7-1 RO-Zero

Reserved Register (Offset 0Dh) — 3 BYTES

a. RsvdP_23-0 RO-Zero

19. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
20. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- More than one Power Budgeting Extended Capability structure is present.
- A VF contains a Power Budgeting Extended Capability structure.
- An RCRB contains a Power Budgeting Extended Capability structure.
- The Capability Version field does not report 1h.
- The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- The function under test reports an invalid Power Rail field value for any of the non-zero Power Budgeting data sets that it reports.
- The function under test reports an invalid Type field value for any of the non-zero Power Budgeting data sets that it reports.
- The device does not report at least a D0 Max and D0 Sustained set of power data for every power rail it uses power from.
- The device has Emergency Power Reduction Supported not 00b and does not report at least a D0 Max – Emergency Power Reduction State and D0 Sustained – Emergency Power Reduction State set of power data for every power rail it uses power from.
- The device reports more than one set of data for the same PM State, Type, and Power Rail combination.
- The device reports a non-zero set of data for a Data Select register value greater than the number of supported data sets.
- Any of the register field characteristic tests fail.
- The power information is not returned normally when valid indices are used after an out of bound index is written to the Data Select register.

2.2.16. TD_1_11 Command and Status Registers

The test verifies that the function under test implements the Command and Status registers as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *PCI Local Bus Specification, Revision 3.0 (Base 3.x or earlier only)*
- *Single Root I/O Virtualization and Sharing Specification (Base 3.x or earlier only)*
- *ECN Readiness Notifications (RN) (to Base 3.0)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. The following register field characteristic checks are performed:

Command Register (Location 04h) — WORD

a. I/O Space Enable

(for VFs)	RO-Zero
(otherwise)	RW or RO-Zero

b. Memory Space Enable

(for VFs)	RO-Zero
(for any function with a Type 0 Configuration Space Header excluding VFs)	RW or RO-Zero
(for any function with a Type 1 Configuration Space Header)	RW

c. Bus Master Enable

(for any function with a Type 0 Configuration Space Header)	RW or RO-Zero
(for any function with a Type 1 Configuration Space Header)	RW

d. Special Cycle Enable — RO-Zero

e. Memory Write and Invalidate

(for PCI Express to PCI/PCI-X Bridges or PCI/PCI-X to PCI Express Bridges)	RW or RO-Zero
(for all except for PCI Express to PCI/PCI-X Bridge or PCI/PCI-X to PCI Express Bridge)	RO-Zero

f. VGA Palette Snoop

(for PCI/PCI-X to PCI Express Bridges)	RW or RO-Zero
(for all except for PCI/PCI-X to PCI Express Bridge)	RO-Zero

g. Parity Error Response

(for VFs)	RO-Zero
(for RC Integrated Endpoints)	RW or RO-Zero
(for any function excluding VFs and RC Integrated Endpoints)	RW

h. IDSEL Sleeping/Wait Cycle Control — RO-Zero

i. SERR# Enable

(for VFs)	RO-Zero
(for RC Integrated Endpoints)	RW or RO-Zero
(for any function excluding VFs and RC Integrated Endpoints)	RW

j. Fast Back-to-Back Transactions Enable

(for PCI/PCI-X to PCI Express Bridges) RW or RO-Zero
(for all except for PCI/PCI-X to PCI Express Bridge) RO-Zero

k. Interrupt Disable
(for VFs) RO-Zero
(for non-VFs where Interrupt Pin is non-zero) RW
(for non-VFs where Interrupt Pin is zero) RW or RO-Zero

l. RsvdP_15-11 RO-Zero

Status Register (Location 06h) — WORD

a. Reserved_2-0
(For Base 2.x or earlier testing) RO-Zero
b. Immediate Readiness
(For Base 3.x or later testing) RO
c. RsvdZ_2-1
(For Base 3.x or later testing) RO-Zero
d. Interrupt Status
(for VFs) RO-Zero
(otherwise) RO
e. Capabilities List RO-Ones
f. 66 MHz Capable
(for PCI/PCI-X to PCI Express Bridges) RO
(for all except for PCI/PCI-X to PCI Express Bridge) RO-Zero
g. RsvdZ_6 RO-Zero
h. Fast Back-to-Back Transactions Capable
(for PCI/PCI-X to PCI Express Bridges) RO
(for all except for PCI/PCI-X to PCI Express Bridge) RO-Zero
i. Master Data Parity Error RW1C
j. DEVSEL Timing
(for PCI/PCI-X to PCI Express Bridges) RO
(for all except for PCI/PCI-X to PCI Express Bridge) RO-Zero
k. Signaled Target Abort RW1C
l. Received Target Abort RW1C
m. Received Master Abort RW1C
n. Signaled System Error RW1C
o. Detected Parity Error RW1C

3. The following default value checks are performed:

Command Register Default Value (Location 04h) — WORD

a. I/O Space Enable 0
b. Memory Space Enable 0
c. Bus Master Enable 0
d. Memory Write and Invalidate 0
e. VGA Palette Snoop 0
f. Parity Error Response 0
g. SERR# Enable 0
h. Fast Back-to-Back Transactions Enable 0

i. Interrupt Disable 0

Status Register Default Value (Location 06h) — WORD

a. Interrupt Status 0
b. Master Data Parity Error 0
c. Signaled Target Abort 0
d. Received Target Abort 0
e. Received Master Abort 0
f. Signaled System Error 0
g. Detected Parity Error 0

Note: The zero default values on the Status register assume that no events that would cause an interrupt to be generated, or an error to be detected, have occurred in the test environment.

4. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

2.2.17. TD_1_12 Cache Line Size, Latency Timer, and Min_Gnt/Max_Lat Registers

The test verifies that the function under test implements the Cache Line Size, Latency Timer, Min_Gnt, and Max_Lat register fields as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0*
- *Single Root I/O Virtualization and Sharing Specification (Base 3.x or earlier only)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.

2. For a PCI/PCI-X to PCI Express Bridge the following checks are performed and if any are not as stated, this is recorded as a failure, but the test continues:
 a. Write a byte of FFh to location 0Dh (Latency Timer register).
 b. Read a byte from location 0Dh (Latency Timer register) and verify that one of the following values is returned: (FFh, F8h, or 10h to 00h).
 c. Write a byte of 00h to location 0Dh (Latency Timer register).
 d. Read a byte from location 0Dh (Latency Timer register) and verify that one of the following values is returned: (10h to 00h).
 e. If the value returned is 00h, then record this by setting Latency Timer Non-Zero [LTNZ] to 0. If the value returned is non-zero, then set [LTNZ] to 1. (The value in [LTNZ] will be used by the default value test to indicate that the Latency Timer register is not hard-wired to a non-zero value.)

3. The following register field characteristic checks are performed:

Cache Line Size Register (Location 0Ch) — BYTE	
(for VFs)	RO-Zero
(for PCI Express to PCI/PCI-X Bridges or PCI/PCI-X to PCI Express Bridges)	RW or RO-Zero
(for all except for PCI Express to PCI/PCI-X Bridge or PCI/PCI-X to PCI Express Bridge)	RW
Latency Timer Register (Location 0Dh) — BYTE	
(for PCI/PCI-X to PCI Express Bridges: bits 2-0)	RW or RO
(for PCI/PCI-X to PCI Express Bridges: bits 7-3)	RW or RO
(for all except for PCI/PCI-X to PCI Express Bridge)	RO-Zero
Min_Gnt (Location 3Eh) — BYTE (only if device has Type 0 Configuration Space Header)	RO-Zero
Max_Lat (Location 3Fh) — BYTE (only if device has Type 0 Configuration Space Header)	RO-Zero

4. The following default value checks are performed:

Cache Line Size Register Default Value (Location 0Ch) — BYTE	0
Latency Timer Register Default Value (Location 0Dh) — BYTE	
(for PCI/PCI-X to PCI Express Bridges)	
(if [LTNZ] is 0)	0

5. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- ❑ For a PCI/PCI-X to PCI Express Bridge, the Latency Timer register is not implemented as RW, RW with lower 3 bits hard-wired to 000b, or RO with a value between 16 and 0 inclusive.

- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

2.2.18. TD_1_13 Interrupt Pin and Interrupt Line Registers

The test verifies that the function under test implements the Interrupt Pin and Interrupt Line registers as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *Single Root I/O Virtualization and Sharing Specification (Base 3.x or earlier only)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Read the byte from location 3Dh (Interrupt Pin register) in configuration space and perform the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. For a VF this value must be 00h.
 b. For Base 3.x or earlier testing: for a non-VF this value must be one of the following: (00h, 01h, 02h, 03h, or 04h).
 c. For Base 4.x or later testing: for a non-VF in a single function device this value must be one of the following: (00h or 01h).
 d. For Base 4.x or later testing: for a non-VF in a multi-function device this value must be one of the following: (00h, 01h, 02h, 03h, or 04h).
3. The following register field characteristic checks are performed:

 Interrupt Line Register (Location 3Ch) — BYTE

(for VFs)	RO-Zero
(otherwise)	RW

 Interrupt Pin Register (Location 3Dh) — BYTE

(for VFs)	RO-Zero
(otherwise)	RO

4. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.

d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- For a VF, the Interrupt Pin register does not return 00h.
- For a non-VF, the Interrupt Pin register does not return 00h, 01h, 02h, 03h, or 04h (for Base 3.x or earlier testing only).
- For a non-VF in a single function device, the Interrupt Pin register does not return 00h or 01h (for Base 4.x or later testing only).
- For a non-VF in a multi-function device, the Interrupt Pin register does not return 00h, 01h, 02h, 03h, or 04h (for Base 4.x or later testing only).
- Any of the register field characteristic tests fail.

2.2.19. TD_1_14 Secondary Latency Timer and Secondary Status Registers

The test verifies that the function under test implements the Secondary Latency Timer and Secondary Status registers as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Read the Header Type register and if the value in bits 6-0 is 000 0001b (Type 1 Configuration Space Header) the test continues. If not, the test terminates (this is not a failure and the test result is reported as skipped).
3. For a PCI Express to PCI/PCI-X Bridge the following checks are performed and if any are not as stated, this is recorded as a failure, but the test continues:
 a. Write a byte of FFh to location 1Bh (Secondary Latency Timer register).
 b. Read a byte from location 1Bh (Secondary Latency Timer register) and verify that one of the following values is returned: (FFh, F8h, or 10h to 00h).
 c. Write a byte of 00h to location 1Bh (Secondary Latency Timer register).
 d. Read a byte from location 1Bh (Secondary Latency Timer register) and verify that one of the following values is returned: (10h to 00h).

e. If the value returned is 00h, then record this by setting Latency Timer Non-Zero [LTNZ] to 0. If the value returned is non-zero, then set [LTNZ] to 1. (The value in [LTNZ] will be used by the default value test to indicate that the Secondary Latency Timer register is not hard-wired to a non-zero value.)

4. The following register field characteristic checks are performed:

Secondary Latency Timer Register (Location 1Bh) — BYTE

(for PCI Express to PCI/PCI-X Bridges: bits 2-0)	RW or RO
(for PCI Express to PCI/PCI-X Bridges: bits 7-3)	RW or RO
(for all except for PCI Express to PCI/PCI-X Bridge)	RO-Zero

Secondary Status Register (Location 1Eh) — WORD

a. RsvdZ_4-0	RO-Zero
b. 66 MHz Capable	
(for all except for PCI Express to PCI/PCI-X Bridge)	RO-Zero
(for PCI Express to PCI/PCI-X Bridges)	RO
c. RsvdZ_6	RO-Zero
d. Fast Back-to-Back Transactions Capable	
(for all except for PCI Express to PCI/PCI-X Bridge)	RO-Zero
(for PCI Express to PCI/PCI-X Bridges)	RO
e. Master Data Parity Error	RW1C
f. DEVSEL Timing	
(for all except for PCI Express to PCI/PCI-X Bridge)	RO-Zero
(for PCI Express to PCI/PCI-X Bridges)	RO
g. Signaled Target Abort	RW1C
h. Received Target Abort	RW1C
i. Received Master Abort	RW1C
j. Received System Error	RW1C
k. Detected Parity Error	RW1C

5. The following default value checks are performed:

Secondary Latency Timer Register Default Value (Location 1Bh) — BYTE

(for PCI Express to PCI/PCI-X Bridges)	
(if [LTNZ] is 0)	0

Secondary Status Register Default Value (Location 1Eh) — WORD

a. Master Data Parity Error	0
b. Signaled Target Abort	0
c. Received Target Abort	0
d. Received Master Abort	0
e. Received System Error	0
f. Detected Parity Error	0

Note: The zero default values on the Secondary Status register assume that no events that would cause an error to be detected have occurred in the test environment.

6. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.

c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- For a PCI Express to PCI/PCI-X Bridge, the Secondary Latency Timer register is not implemented as RW, RW with lower 3 bits hard-wired to 000b, or RO with a value between 16 and 0 inclusive.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

2.2.20. TD_1_15 Bridge Control Register

The test verifies that the function under test implements the Bridge Control register as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0*
- *PCI-to-PCI Bridge Architecture Specification, Revision 1.2 (Base 3.x or earlier only)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Read the Header Type register and if the value in bits 6-0 is 000 0001b (Type 1 Configuration Space Header) the test continues. If not, the test terminates (this is not a failure and the test result is reported as skipped).
3. The following register field characteristic checks are performed:

Bridge Control Register (Location 3Eh) — WORD

a. Parity Error Response Enable	RW
b. SERR# Enable	RW
c. ISA Enable	RW
d. VGA Enable	RW or RO-Zero
e. VGA 16-bit Decode	RW or RO-Zero
f. Master Abort Mode	

(for all except for PCI Express to PCI/PCI-X Bridge or PCI/PCI-X to PCI Express Bridge)	RO-Zero
(for PCI Express to PCI/PCI-X Bridges or PCI/PCI-X to PCI Express Bridges)	RW
g. Secondary Bus Reset	RW
h. Fast Back-to-Back Transactions Enable	
(for all except for PCI Express to PCI/PCI-X Bridge)	RO-Zero
(for PCI Express to PCI/PCI-X Bridges)	RW or RO-Zero
i. Primary Discard Timer	
(for all except for PCI/PCI-X to PCI Express Bridge)	RO-Zero
(for PCI/PCI-X to PCI Express Bridges)	RW
j. Secondary Discard Timer	
(for all except for PCI Express to PCI/PCI-X Bridge)	RO-Zero
(for PCI Express to PCI/PCI-X Bridges)	RW
k. Discard Timer Status	
(for all except for PCI Express to PCI/PCI-X Bridge or PCI/PCI-X to PCI Express Bridge)	RO-Zero
(for PCI Express to PCI/PCI-X Bridges or PCI/PCI-X to PCI Express Bridges)	RW1C
l. Discard Timer SERR# Enable	
(for all except for PCI Express to PCI/PCI-X Bridge or PCI/PCI-X to PCI Express Bridge)	RO-Zero
(for PCI Express to PCI/PCI-X Bridges or PCI/PCI-X to PCI Express Bridges)	RW
m. RsvdP_15-12	RO-Zero

4. The following default value checks are performed:

Bridge Control Register Default Value (Location 3Eh) — WORD

a. Parity Error Response Enable	0
b. SERR# Enable	0
c. ISA Enable	0
d. VGA Enable	0
e. VGA 16-bit Decode	0
f. Master Abort Mode	0
g. Secondary Bus Reset	0
h. Fast Back-to-Back Transactions Enable	0
i. Primary Discard Timer	0
j. Secondary Discard Timer	0
k. Discard Timer Status	0
l. Discard Timer SERR# Enable	0

5. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

2.2.21. TD_1_16 PCI Power Management Capability Structure

The test verifies that the function under test reports a PCI Power Management Capability structure and that it is implemented as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *PCI Bus Power Management Interface Specification, Revision 1.2 (Base 3.x or earlier only)*
- *Single Root I/O Virtualization and Sharing Specification (Base 3.x or earlier only)*
- *ECN Readiness Notifications (RN) (to Base 3.0)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Capability ID field for each of the function's Capability structures. Determine how many instances of the Capability ID of 01h (PCI Power Management Capability) are found. If more than one is found, the test terminates with a failure.
3. For all non-VFs, if the Capability ID of 01h is not found in a Capability structure, the test terminates with a failure.
4. If the Capability ID of 01h is found in a Capability structure, the following steps are performed on that Capability structure. If the Capability ID of 01h is not found in a Capability structure, the test skips to step 21.
5. Read the DWORD from offset 00h (Power Management Capabilities register) in the PCI Power Management Capability structure.
6. The Next Capability Pointer field must be 00h or greater than 3Fh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
7. The Version field must be set to 011b. If not, this is recorded as a failure, but the test continues.
8. The PME Clock field must be zero. If not, this is recorded as a failure, but the test continues.

9. If device type is Root Port, or Switch Upstream Port, or Switch Downstream Port then the following checks are performed and if any are not as stated, this is recorded as a failure, but the test continues:
 a. For Base 3.0 or earlier testing: PME Support field bits 31, 30, and 27 must each return 1.
 b. For Base 3.1 or later testing: PME Support field bits 30, and 27 must each return 1.
 c. For Base 3.1 or later testing: if D1 Support bit is 1, then PME Support field bit 28 must return 1.
 d. For Base 3.1 or later testing: if D2 Support bit is 1, then PME Support field bit 29 must return 1.
10. For the WORD at offset 04h (Power Management Status and Control register) the following checks are performed and if any are not as stated, this is recorded as a failure, but the test continues:
 a. Read a WORD from offset 04h and use this as the base PM Value [PMV].
 b. Clear to 00b the lower two bits of [PMV] and use this as the new [PMV] value (bits 15-2 contain what was read, and bits 1-0 are 00b).
 c. Write a WORD to offset 04h using the data as [PMV] ORed with 0000h (Power State field = 00b).
 d. Wait 10 seconds.
 e. Read a WORD from offset 04h - the Power State field must return 00b.
 f. If the D1 Support field is 1 (in Power Management Capabilities register), then write a WORD to offset 04h using the data as [PMV] ORed with 0001h (Power State field = 01b). Otherwise skip to step i.
 g. Wait 10 seconds.
 h. Read a WORD from offset 04h - the Power State field must return 01b.
 i. If the D2 Support field is 1 (in Power Management Capabilities register), then write a WORD to offset 04h using the data as [PMV] ORed with 0002h (Power State field = 10b). Otherwise skip to step l).
 j. Wait 10 seconds.
 k. Read a WORD from offset 04h - the Power State field must return 10b.
 l. Write a WORD to offset 04h using the data as [PMV] ORed with 0003h (Power State field = 11b).
 m. Wait 10 seconds.
 n. Read a WORD from offset 04h - the Power State field must return 11b.
 o. Write a WORD to offset 04h using the data as [PMV] ORed with 0000h (Power State field = 00b).
 p. Wait 10 seconds.
 q. Read a WORD from offset 04h - the Power State field must return 00b.
11. Set the Data Present Flag [DPF] to 0.
12. Test software writes a data value of Fh to the Data Select field and the reads back the value from the Data Select field and performs the following checks and if not as stated, this is recorded as a failure, but the test continues:
 a. For a VF, the value must be 0h.
 b. For a VF, skip to step 19.
 c. For a non-VF, if the value is 0h, skip to step 19.
13. Set the Data Select Value [DSV] to 0h.

14. Test software writes the [DSV] value to the Data Select field
15. Test software reads back a byte from offset 07h (Data register) in the PCI Power Management Capability structure and performs the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. If the read byte is non-zero, then set [DPF] to 1.
 b. Read the Data Scale field and if it is non-zero, then set [DPF] to 1.
 c. If the data value written to the Data Select field is 0h to 7h, then if the read byte was non-zero, then the Data Scale field must be non-zero.
 d. If the data value written to the Data Select field is 8h and the device is a multi-function device, and the function under test is function 0, then if the read byte was non-zero then the Data Scale field must be non-zero.
 e. If the data value written to Data Select field is 0h, 3h, 4h, 7h, then if the read byte was 00h a warning message is issued, but this is not treated in itself as a failure.
 f. If the data value written to Data Select field is 1h or 5h and the D1 Support field returns 1, then if the read byte was 00h a warning message is issued, but this is not treated in itself as a failure.
 g. If the data value written to Data Select field is 2h or 6h and the D2 Support field returns 1, then if the read byte was 00h a warning message is issued, but this is not treated in itself as a failure.
 h. If the data value written to Data Select field is 8h and the device is a multi-function device, and the function under test is function 0, then if the read byte was 00h a warning message is issued, but this is not treated in itself as a failure.
 i. If the data value written to the Data Select field is 8h and the device is a single function device, or if the function under test is not function 0, then the read byte must be 00h and the Data Scale field must be 00b.
 j. If the data value written to the Data Select field is 9h to Fh, then the read byte must be 00h and the Data Scale field must be 00b.
 k. Write a new data value to the Data Scale field which is the inverse of the current read back value. Read back the Data Scale field again and ensure that it returns the original value (it is a RO field).
 l. Write a new data value to the Data register which is the inverse of the current read back value. Read back the Data register again and ensure that it returns the original value (it is a RO field).
16. Test software increments [DSV] by 1 and repeats steps 14-16. Test software continues repeating until [DSV] exceeds Fh.
17. Test software repeats steps 14-15, 17 with the [DSV] value written to the Data Select register in inverse order and stopping when it decrements below 0h (starting with Fh and decrementing to 0h). The returned information must be the same. If not, this is recorded as a failure, but the test continues.
18. If [DPF] is 1, test software reads back a word from offset 02h (Power Management Capabilities register) in the PCI Power Management Capability structure and performs the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. Test software writes a 1 to the Aux Power PM Enable (Device Control register) and then reads it back, and only if it returns 0:
 i. The Aux Current field must return 000b.

19. The following register field characteristic checks are performed:

Power Management Capability Header (Offset 00h) — WORD

a. Capability ID — RO
b. Next Capability Pointer — RO

Power Management Capabilities Register (Offset 02h) — WORD

a. Version — RO
b. PME Clock — RO-Zero
c. RsvdP_4
 (For Base 2.x or earlier testing) — RO-Zero
d. Immediate Readiness on Return to D0
 (For Base 3.x or later testing) — RO
e. Device Specific Initialization — RO
f. Aux Current
 (for Root Ports, Switch Ports, and Bridges) — RO
 (for non-Root Ports, non-Switch Ports, and non-Bridges, if Aux Power PM Enable (Device Control) is not RO-Zero or PME Support field is 1 xxxxb) — RO
 (for non-Root Ports, non-Switch Ports, and non-Bridges, if Aux Power PM Enable (Device Control) is RO-Zero and PME Support field is 0 xxxxb) — RO-Zero
 Note: Prior to Base 3.1, for a Root Port or a Switch Port there was no way to tell whether Aux Current needed to be RO-Zero since the PME Support field must be 1 1xx1b for forwarding PME even if the device cannot generate PME, but this requirement was removed in Base 3.1.
g. D1 Support — RO
h. D2 Support — RO
i. PME Support — RO

Power Management Control/Status (n) Register (Offset 04h) — DWORD

Data Select register is written with value (n) prior to this register test. This test is then repeated for (n) = 0h to Fh.

a. Power State — RW
b. RsvdP_2 — RO-Zero
c. No_Soft_Reset — RO
d. RsvdP_7-4 — RO-Zero
e. PME_En
 (if PME Support field is 0 0000b) — RW or RO-Zero
 (for Root Ports, Switch Ports, and Bridges) — RWS or RW
 (for non-Root Ports, non-Switch Ports, and non-Bridges, if PME Support field is 1 xxxxb) — RWS
 (for non-Root Ports, non-Switch Ports, and non-Bridges, if PME Support field is 0 xxxxb and non-zero) — RW
 Note: Prior to Base 3.1, for a Root Port or a Switch Port there was no way to tell whether PME_En needed to be RWS since the PME Support field must be 1 1xx1b

for forwarding PME even if the device cannot generate PME, but this requirement was removed in Base 3.1.

f. Data Scale (n)
 (for VFs) RO-Zero
 (otherwise) RO
g. PME_Status
 (for Root Ports, Switch Ports, and Bridges) RW1CS or RW1C
 (for non-Root Ports, non-Switch Ports, and non-Bridges, if PME Support field is 1 xxxxb) RW1CS
 (for non-Root Ports, non-Switch Ports, and non-Bridges, if PME Support field is 0 xxxxb) RW1C
 Note: Prior to Base 3.1, for a Root Port or a Switch Port there was no way to tell whether PME_Status needed to be RW1CS since the PME Support field must be 1 1xx1b for forwarding PME even if the device cannot generate PME, but this requirement was removed in Base 3.1.
h. RsvdP_21-16 RO-Zero
i. Undefined_22
 (For Base 3.1 or later testing) RO-Zero
 (For Base 3.0 or earlier testing)
 (for all except PCI Express to PCI/PCI-X Bridge) RO-Zero
 (for PCI Express to PCI/PCI-X Bridges) RO
 Note: This was once B2/B3 Support.
j. Undefined_23
 (For Base 3.1 or later testing) RO-Zero
 (For Base 3.0 or earlier testing)
 (for all except PCI Express to PCI/PCI-X Bridge) RO-Zero
 (for PCI Express to PCI/PCI-X Bridges) RO
 Note: This was once Bus Power/Clock Control Enable.
k. Data (n)
 (For Base 2.x or earlier testing: for VFs) RO
 (For Base 3.x or later testing: for VFs) RO-Zero
 (otherwise) RO
 Note: Since the Data Select register is not sticky, it must be re-written following any Reset Sequence (described in Section 2.1.1.1) being executed while testing this register.

20. The following default value checks are performed:

Power Management Control/Status Register Default Value (Offset 04h) –– DWORD

a. Power State 0
b. PME_En
 (for non-Root Ports, non-Switch Ports, and non-Bridges, if PME Support field is 0 xxxxb) 0
c. PME_Status
 (for non-Root Ports, non-Switch Ports, and non-Bridges, if PME Support field is 0 xxxxb) 0

21. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):

a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- For a non-VF, a PCI Power Management Capability structure is not present.
- More than one PCI Power Management Capability structure is present.
- A non-zero Next Capability Pointer field is less than or equal to 3Fh, or the lower 2 bits are non-zero.
- The version for the PCI Power Management Capability structure is not 011b.
- The PME Clock field is non-zero.
- A Root Port or a Switch Port does not have bits 31, 30, and 27 each return 1 in the PME Support field (for Base 3.0 or earlier testing only).
- A Root Port or a Switch Port does not have bits 30 and 27 each return 1 in the PME Support field (for Base 3.1 or later testing only).
- A Root Port or a Switch Port does not have bit 28 return 1 in the PME Support field when D1 Support is 1 (for Base 3.1 or later testing only).
- A Root Port or a Switch Port does not have bit 29 return 1 in the PME Support field when D2 Support is 1 (for Base 3.1 or later testing only).
- The Power State field is non-zero in the Power Management Status and Control register.
- The PME Support is non-zero and the PME_En field is not writeable.
- The Power State field cannot be set to D0, D1 (if supported), D2 (if supported), and D3.
- The Power State field does not read D0 after a reset when the function is in D0-Uninitialized or D0-Initialized state.
- For a VF, the Data Select register returns a non-zero value.
- The Data register contains unsupported entries.
- The Data Scale field contains unsupported entries.
- The Aux Current field is non-zero when any Data register entry is non-zero and Aux Power PM Enable is RO-Zero.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

The test *warns* if:

- The Data register contains a valid entry of 0W.

2.2.22. TD_1_17 MSI-X Capability Structure

This test verifies that if the function under test reports a MSI-X Capability structure, it is implemented as defined in the relevant specifications. (If support for specific features is indicated

the function must implement at least either a MSI or a MSI-X Capability structure. The MSI Capability structure is tested elsewhere.)

Relevant Specifications

- *PCI Express Base Specification*
- *PCI Local Bus Specification, Revision 3.0 (Base 3.x or earlier only)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Capability ID field for each of the function's Capability structures. If the Capability ID of 11h is not found in a Capability structure, the following tests are performed on that function:
 a. Examine the Capability ID field for each of the function's Capability structures. If the Capability ID of 05h (MSI Capability) is not found in a Capability structure, all of the following are checked. If any of these are not true, the test fails and this is recorded as a failure, while the test continues at the next step.
 i. The Interrupt Pin register (location 3Dh) value is zero.
 ii. The function under test is not a Root Port.
 iii. The function under test is not a Root Complex Event Collector.
 iv. If the function under test is a downstream port, the DRS Supported bit (Link Capabilities 2 register) value is 0.
 v. If the function under test is a downstream port, it does not contain a DPC Extended Capability structure.
 vi. If the function under test is a PF, the VF Migration Capable bit (SR-IOV Capabilities register) value is 0.
3. Examine the Capability ID field for each of the function's Capability structures. Determine how many instances of the Capability ID of 11h (MSI-X Capability) are found. If more than one is found, the test terminates with a failure.
4. If the Capability ID of 11h is found in a Capability structure, the following steps are performed on that Capability structure. If the Capability ID of 11h is not found in a Capability structure, the test skips to step 14.
5. A WORD is read from offset 00h in the MSI-X Capability structure (Capability ID field, Next Capability Pointer field) and the following tests are performed:
 a. The Next Capability Pointer field must be 00h or greater than 3Fh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.

6. One WORD is read from offset 02h (Message Control) in the MSI-X Capability structure.
7. One DWORD is read from offset 04h (Table Offset/Table BIR) in the MSI-X Capability structure.
8. The Table BIR field must return a valid value as follows and if any are not as stated, this is recorded as a failure, but the test continues:
 a. For a function with a Type 0 Configuration Space Header valid values are (0, 1, 2, 3, 4, or 5).
 b. For a function with a Type 1 Configuration Space Header valid values are (0, 1).
 c. The BAR pointed to by Table BIR is read and bit 0 of that BAR must be 0 (Memory BAR).
9. One DWORD is read from offset 08h (PBA Offset/PBA BIR) in the MSI-X Capability structure.
10. The PBA BIR field must return a valid value as follows and if any are not as stated, this is recorded as a failure, but the test continues:
 a. For a function with a Type 0 Configuration Space Header valid values are (0, 1, 2, 3, 4, or 5).
 b. For a function with a Type 1 Configuration Space Header valid values are (0, 1).
 c. The BAR pointed to by PBA BIR is read and bit 0 of that BAR must be 0 (Memory BAR).
11. If the Table BIR field and the PBA BIR field return the same value, test software performs the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The Table Offset field and the PBA Offset field must not have the same value.
 b. If the PBA Offset field is greater than the Table Offset field, then the PBA Offset field's value must be greater than (Table Offset + (Table Size +1) * 16).
 c. If the Table Offset field is greater than the PBA Offset field, then the Table Offset field's value must be greater than (PBA Offset + ((Table Size +1) divided by 64 and discarding remainder) * 8).
12. The following register field characteristic checks are performed:

MSI-X Capability Header (Offset 00h) — WORD

a. Capability ID	RO
b. Next Capability Pointer	RO

Message Control Register (Offset 02h) — WORD

a. Table Size	RO
b. RsvdP_13-11	RO-Zero
c. Function Mask	RW
d. MSI-X Enable	RW

Table Offset/Table BIR Register (Offset 04h) — DWORD

a. Table BIR	RO
b. Table Offset	RO

PBA Offset/PBA BIR (Offset 08h) — DWORD

a. PBA BIR	RO
b. PBA Offset	RO

Message Address ([table] + ([n-1] * 16) + 00h) — DWORD

a. Message Address_1-0	RW or RO-Zero
b. Message Address_31-2	RW

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by Table BIR field) plus the offset (value in the Table Offset field multiplied by 8). All values of [n-1] between 0 and the value given in the Table Size field must be tested.

Message Upper Address ([table] + ([n-1] * 16) + 04h) — DWORD

a. Message Upper Address — RW

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by Table BIR field) plus the offset (value in the Table Offset field multiplied by 8). All values of [n-1] between 0 and the value given in the Table Size field must be tested.

Message Data ([table] + ([n-1] * 16) + 08h) — DWORD

a. Message Data — RW

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by Table BIR field) plus the offset (value in the Table Offset field multiplied by 8). All values of [n-1] between 0 and the value given in the Table Size field must be tested.

Vector Control ([table] + ([n-1] * 16) + 0Ch) — DWORD

a. Mask Bit — RW
b. RsvdP_15-1 — RW or RO-Zero
c. ST Lower
 (if function implements a TPH Requester Extended Capability structure and ST Table Location is 10b and [n-1] is less than or equal to ST Table Size) — RW
 (otherwise) — RO-Zero
d. ST Upper
 (if function implements a TPH Requester Extended Capability structure and ST Table Location is 10b and Extended TPH Requester Support is 1 and [n-1] is less than or equal to ST Table Size) — RW
 (otherwise) — RO-Zero

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by Table BIR field) plus the offset (value in the Table Offset field multiplied by 8). All values of [n-1] between 0 and the value given in the Table Size field must be tested.

Pending Bit Array ([ptable] + ([n-1] * 8) + 00h) — 2 DWORDS

a. Pending Bits
 (all bits) — RW or RO-Zero

Note: Testing this requires programming the designated Memory BAR and enabling Memory decoding. The value of [ptable] is the BAR contents (pointed to by PBA BIR field) plus the offset (value in the PBA Offset field multiplied by 8). All values of [n-1] between 0 and the length (((value in the Table Size field plus one) divided by 64) discarding any remainder) must be tested.

13. The following default value checks are performed:

Message Control Register Default Value (Offset 02h) — WORD

a. Function Mask 0
b. MSI-X Enable 0

Message Address Default Value ([table] + ([n-1] * 16) + 00h) — DWORD

a. Message Address_1-0 00b

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by Table BIR field) plus the offset (value in the Table Offset field multiplied by 8). All values of [n-1] between 0 and the value given in the Table Size field must be tested.

Vector Control Default Value ([table] + ([n-1] * 16) + 0Ch) — DWORD

a. Mask Bit 1
b. ST Lower 00h
c. ST Upper 00h

Note: Testing this requires programming the designated Memory BAR and enabling Memory decoding. The value of [table] is the BAR contents (pointed to by Table BIR field) plus the offset (value in the Table Offset field multiplied by 8). All values of [n-1] between 0 and the value given in the Table Size field must be tested.

Pending Bit Array Default Value ([ptable] + ([n-1] * 8) + 00h) — 2 DWORDS

a. Pending Bits
(all bits) 0

Note: Testing this requires programming the designated Memory BAR and enabling Memory decoding. The value of [ptable] is the BAR contents (pointed to by PBA BIR field) plus the offset (value in the PBA Offset field multiplied by 8). All values of [n-1] between 0 and the length (((value in the Table Size field plus one) divided by 64) discarding any remainder) must be tested.

14. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- ❑ Neither a MSI-X Capability structure nor a MSI Capability structure is present in the following:
 - A function that has Interrupt Pin register as non-zero
 - A Root Port
 - A Root Complex Event Collector
 - A downstream port that has DRS Supported set to 1
 - A downstream port that has a DPC Extended Capability structure
 - A PF that has VF Migration Supported set to 1
- ❑ More than one MSI-X Capability structure is present.

- A non-zero Next Capability Pointer field value is less than or equal to 3Fh, or the lower 2 bits are non-zero.
- The Table BIR field has a reserved value.
- The Table BIR field points to an I/O Space BAR.
- The PBA BIR field has a reserved value.
- The PBA BIR field value points to an I/O Space BAR.
- The Table Offset field and the PBA Offset field values overlap.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

2.2.23. TD_1_18 Base Address Registers

The test verifies that the function under test implements all BAR registers as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *PCI Local Bus Specification, Revision 3.0 (Base 3.x or earlier only)*
- *Single Root I/O Virtualization and Sharing Specification (Base 3.x or earlier only)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Starting at location 10h the next 6 DWORDs (for a function with a Type 0 Configuration Space Header), or next 2 DWORDs (for a function with a Type 1 Configuration Space Header), are read. These are the BAR0, BAR1 (all functions), BAR2 to BAR5 (for a function with a Type 0 Configuration Space Header) registers. (Some BAR registers may occupy 2 DWORDs if they are 64 bit BARs.)
 a. For a function with a Type 0 Configuration Space Header, location 24h (BAR 5) must not have both bit 0 = 0 (Memory Space BAR) and Type field = 10b (64 bit addressing). If it does this is recorded as a failure, but the test continues.
 b. For a function with a Type 1 Configuration Space Header, location 14h (BAR 1) must not have both bit 0 = 0 (Memory Space BAR) and Type field = 10b (64 bit addressing). If it does this is recorded as a failure, but the test continues.

3. For a VF, for each BAR test software performs the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. Test software writes FFFF FFFFh to the BAR and then reads back the same register. The BAR register must return 0000 0000h.
 b. For a VF, skip to step 9.
4. For each BAR register test software writes FFFF FFFFh to the BAR and then reads back the same register. If it returns 0000 0000h, then this is an empty BAR. Empty BARs are excluded from further testing.
5. For each non-empty BAR register test software checks bit 0 (Space Indicator). If the Space Indicator indicates an I/O Space BAR, then perform the tests in step 6. If the Space Indicator indicates a Memory Space BAR, then perform the tests in step 7.
6. For I/O Space BARs only perform the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. Bit 1 must be zero.
 b. Test software writes FFFF FFFFh to the BAR and then reads back the same register. Bit 8 must return 1 (I/O BAR must claim 256 Bytes or less).
 c. Test software writes bit 31 with 1, then reads it back and sets the Bit 31 is Read-Write [B31RW] to the value read.
 d. Starting at bit 2 determine the least significant bit value that is set to 1 and record it in Least Significant Bit [LSB]. [LSB] must be less than 9. This same [LSB] value is used in subsequent tests of this same BAR.
 vii. If [B31RW] is 0, all bits from 31 to 16 must also be 0.
 viii. If [B31RW] is 0, all bits from 15 to [LSB] must also be 1.
 ix. If [B31RW] is 1, all bits from 31 to [LSB] must also be 1.
 e. Test software writes 5555 5555h to the BAR and then reads back the same register.
 i. If [B31RW] is 0, all bits from 31 to 16 must also be 0.
 ii. If [B31RW] is 0, bits 15-[LSB] must return the written value.
 iii. If [B31RW] is 1, bits 31-[LSB] must return the written value.
 iv. Bits [LSB]-2 must return all 0.
 f. Test software writes AAAA AAAAh to the BAR and then reads back the same register.
 i. If [B31RW] is 0, all bits from 31 to 16 must also be 0.
 ii. If [B31RW] is 0, bits 15-[LSB] must return the written value.
 iii. If [B31RW] is 1, bits 31-[LSB] must return the written value.
 iv. Bits [LSB]-2 must return all 0.
 g. Test software writes CCCC CCCCh to the BAR and then reads back the same register.
 i. If [B31RW] is 0, all bits from 31 to 16 must also be 0.
 ii. If [B31RW] is 0, bits 15-[LSB] must return the written value.
 iii. If [B31RW] is 1, bits 31-[LSB] must return the written value.
 iv. Bits [LSB]-2 must return all 0.
 h. Test software writes 0000 0000h to the BAR and then reads back the same register.
 i. If [B31RW] is 0, all bits from 31 to 16 must also be 0.
 ii. If [B31RW] is 0, bits 15-[LSB] must return the written value.
 iii. If [B31RW] is 1, bits 31-[LSB] must return the written value.
 iv. Bits [LSB]-2 must return all 0.
 i. If the function under test is a PCI/PCI-X to PCI Express Bridge or a PCI Express to PCI/PCI-X Bridge, then a test failure is recorded, but testing continues.

7. For Memory Space BARs only perform the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. For all device types (except Legacy Endpoints and Root Complex Integrated Endpoints) if the Prefetchable bit is 1, then the Type field must be 10b (indicating only 64 bit addressing is supported).
 b. For all device types (except Legacy Endpoints and Root Complex Integrated Endpoints) if the Prefetchable bit is 0, then the Type field must be 10b or 00b (indicating either 64 or 32 bit addressing is supported).
 c. For Legacy Endpoints and Root Complex Integrated Endpoints the Type field must be 10b or 00b (indicating either 64 or 32 bit addressing is supported).
 d. Test software writes FFFF FFFFh to the BAR and then reads back the same register. Bits 6-4 must be 0 (MEMORY BAR size must be 128 Bytes or larger).
 e. If Type field returns 00b, then starting at bit 4 determine the least significant bit value that is set to 1 and record it in Least Significant Bit [LSB]. [LSB] must be less than or equal to 31. All bits from 31 to [LSB] must also be 1. This same [LSB] value is used in subsequent tests of this same BAR.
 f. If Type field returns 10b, test software writes FFFF FFFFh to the immediate next higher Configuration Space location (this is the upper half of a 64 bit BAR) then starting at bit 4 of the lower 32 bit BAR determine the least significant bit value that is set to 1 and record it in Least Significant Bit [LSB]. [LSB] must be less than or equal to 63. All bits from 63 to [LSB] must also be 1.
 g. Test software writes 5555 5555h (for 32 bit BAR) or 5555 5555 5555 5555h (for 64 bit BAR) to the BAR and then reads back the same register. Bits 31-[LSB] (for 32 bit BAR) or Bits 63-[LSB] (for 64 bit BAR) must return the written value. Bits [LSB]-4 must return all 0.
 h. Test software writes AAAA AAAAh (for 32 bit BAR) or AAAA AAAA AAAA AAAAh (for 64 bit BAR) to the BAR and then reads back the same register. Bits 31-[LSB] (for 32 bit BAR) or Bits 63-[LSB] (for 64 bit BAR) must return the written value. Bits [LSB]-4 must return all 0.
 i. Test software writes CCCC CCCCh (for 32 bit BAR) or CCCC CCCC CCCC CCCCh (for 64 bit BAR) to the BAR and then reads back the same register. Bits 31-[LSB] (for 32 bit BAR) or Bits 63-[LSB] (for 64 bit BAR) must return the written value. Bits [LSB]-4 must return all 0.
 j. Test software writes 0000 0000h (for 32 bit BAR) or 0000 0000 0000 0000h (for 64 bit BAR) to the BAR and then reads back the same register. Bits 31-[LSB] (for 32 bit BAR) or Bits 63-[LSB] (for 64 bit BAR) must return the written value. Bits [LSB]-4 must return all 0.

8. If the function implements at least one I/O Space BAR, then it should implement at least one Memory Space BAR. If it does not a warning message is issued, but this is not treated in itself as a failure.

9. The following register field characteristic checks are performed for each non-empty BAR (where the number of BARs depends on the Configuration Space Header type and the BAR size):

 I/O BAR (n) Register –– DWORD
 (for non-VFs)

 a. bit 0 — RO
 b. bit 1 — RO-Zero

 Memory BAR (n) (lower 32) Register –– DWORD
 (for non-VFs)

a. bit 0 RO
b. Type RO
c. Prefetchable RO

10. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- ❑ The highest location that can contain a BAR reports it is the lower 32 bits of a 64 bit BAR.
- ❑ A VF has a non-zero BAR.
- ❑ An I/O Space BAR claims more than 256 Bytes of I/O space per I/O Space BAR.
- ❑ An I/O Space BAR does not return contiguous 1's across all implemented address bits.
- ❑ An I/O Space BAR does not implement RW bits across all implemented address bits.
- ❑ A Memory Space BAR does not contain a valid Type field value.
- ❑ A device type that is neither a Legacy Endpoint nor a Root Complex Integrated Endpoint has a Memory BAR that is Prefetchable and does not support 64 bit addressing.
- ❑ A Memory Space BAR claims less than 128 Bytes of memory space.
- ❑ A Memory Space BAR does not return contiguous 1's across all implemented address bits.
- ❑ A Memory Space BAR does not implement RW bits across all implemented address bits.
- ❑ Any of the register field characteristic tests fail.

The test *warns* if:

- ❑ At least one I/O Space BAR is implemented, but no Memory Space BARs are implemented.

2.2.24. TD_1_19 Multi-Function Virtual Channel Extended Capability Structure

The test verifies that if a function under test reports a PCI Express Multi-Function Virtual Channel Extended Capability structure, it is implemented as defined in the relevant specifications.

Relevant Specifications

- ❑ *PCI Express Base Specification*
- ❑ *Single Root I/O Virtualization and Sharing Specification (Base 3.x or earlier only)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps:

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0008h (Multi-Function Virtual Channel Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Extended Capability ID of 0008h is found in an Extended Capability structure for a VF, the test terminates with a failure.
4. If the Extended Capability ID of 0008h is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
5. If the Extended Capability ID of 0008h is found in an Extended Capability structure, the function must be a device type associated with an Upstream Port. If not, the test terminates with a failure.
6. If the Extended Capability ID of 0008h is found in an Extended Capability structure, the function must be function 0 and the Multi-Function Device field (Header Type register) must be 1 (it must be function 0 of a multi-function device). If not, this is recorded as a failure, but the test continues.
7. If the Extended Capability ID of 0008h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0008h is not found in an Extended Capability structure, the test skips to step 24.
8. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
9. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
10. Test software reads the DWORD at offset 04h (Port VC Capability Register 1) and performs the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The Low Priority Extended VC Count field is less than or equal to the Extended VC Count field value.
 b. The Reference Clock field must be 00b.
11. Set the Number of Virtual Channels [NVC] to the value in the Extended VC Count field.
12. Test software reads the DWORD from offset 08h (Port VC Capability Register 2 register) and performs the following checks:
 a. No reserved bits (4-7) in the VC Arbitration Capability field are set. If not, this is recorded as a failure, but the test continues.
 b. The VC Arbitration Capability field must not be zero, if the Low Priority Extended VC Count field value is non-zero. If not, this is recorded as a failure, but the test continues.

c. The VC Arbitration Capability field must be zero, if the Low Priority Extended VC Count field value is zero. If not, this is recorded as a failure, but the test continues.
d. The VC Arbitration Table Offset field should not be zero, if any of bits 1, 2, or 3 of the VC Arbitration Capability field are set. If not, the test logs a warning, but the test continues.
e. (VC Arbitration Table Offset field value * 4) must be greater than (4 + (3 * (Extended VC Count field value + 1))), if the VC Arbitration Table Offset field is non-zero. If not, this is recorded as a failure, but the test continues.

13. Test software reads the DWORD from offset 0Ch (Port VC Control register and Port VC Status register) and performs the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The VC Arbitration Table Status field returns zero.
14. For non-FLR testing only, if the VC Arbitration Table Offset field is non-zero and the default VC Arbitration Select field value is a WRR based arbitration method test software reads the default values in the VC Arbitration table. These values must all be zero. If not, this is recorded as a failure, but the test continues.
15. Test software writes each of the supported data values indicated by the VC Arbitration Capability field to the VC Arbitration Select field and verifies the value is read back. If not correct this is recorded as a failure, but the test continues.
16. If the VC Arbitration Table Offset field is non-zero, test software performs the following:
 a. For each supported WRR arbitration field mechanism, test software tests loading the table by writing a table of all zeros of the appropriate size to the indicated VC Arbitration table offset. Test software then checks that the VC Arbitration Table Status field returns 1. If not, this is recorded as a failure and the test skips to step 17. Test software then writes 1 to the Load VC Arbitration Table field, while preserving all the other fields in this register.. Test software then reads the VC Arbitration Table Status field repeatedly until it returns 0. If it does not return 0 within 1 second, the test fails and this is recorded as a failure, but the test continues.
17. Step 16 is repeated using all VC entries for the highest supported VC instead of zero.
18. Test software verifies that VC Resource Control, VC Resource Status, and VC Resource Capability registers are present for each VC supported by the function (from 0 to [NVC]).
19. For each set of VC Resource Control, VC Resource Status, and VC Resource Capability registers (from 0 to [NVC]), test software performs the following checks:
 a. The Function Arbitration Capability field must not have bit 6 or 7 set (reserved). If not, this is recorded as a failure, but the test continues.
 b. The Function Arbitration Table Offset field should be non-zero, if any of bits 1, 2, 3, 4, or 5 of the Function Arbitration Capability field are set. If not, the test logs a warning, but the test continues.
 c. (Function Arbitration Table Offset field value * 4) must be greater than (4 + (3 * (Extended VC Count field value + 1))), if the Function Arbitration Table Offset field is non-zero. If not, this is recorded as a failure, but the test continues.
 d. For non-FLR testing only, the TC/VC Map field must be FFh for the first VC resource (VC0) by default. For all other VCs it must be 00h by default. Test software writes each valid TC combination to the field and ensures that the same value can be read back, with the

exception of bit 0 which is RO=1 for the first VC resource (VC0) and RO=0 for all other VCs. If not, this is recorded as a failure, but the test continues.

e. The Load Function Arbitration Table field must be zero. If not, this is recorded as a failure, but the test continues.
f. The Function Arbitration Select field: test software writes each supported data value (based on the Function Arbitration Capability field value) and ensures that the same value is read back. If not, this is recorded as a failure, but the test continues.
g. The VC-ID field: test software ensures that the value is hard-wired to 000b for the first VC resource (VC0). If not, this is recorded as a failure, but the test continues.
h. The VC Enable field: test software checks that this bit is hardwired to one for the first VC resource (VC0). If not, this is recorded as a failure, but the test continues.
i. The Function Arbitration Table Status field must be zero. If not, this is recorded as a failure, but the test continues.

20. If the Function Arbitration Table Offset field is non-zero, test software performs the following:
 a. For each supported WRR based Function Arbitration scheme test software writes a table with all values of the minimum Function number. After the first write to the table test software checks that the Function Arbitration Table Status field returns 1. If not, this is recorded as a failure and the test skips to step 21. Test software writes 1 to the Load Function Arbitration Table field, while preserving all the other fields in this register. Test software then reads the Function Arbitration Table Status field repeatedly until it returns 0. If it does not return 0 within 1 second, the test fails and this is recorded as a failure, but the test continues.
21. Test software repeats step 20 with a valid arbitration table containing all functions in the multi-function device.
22. The following register field characteristic checks are performed:

MFVC Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

Port VC Capability Register 1 (Offset 04h) — DWORD

a. Extended VC Count	RO
b. RsvdP_3	RO-Zero
c. Low Priority Extended VC Count	RO
d. RsvdP_7	RO-Zero
e. Reference Clock	RO
f. Function Arbitration Table Entry Size	RO
g. RsvdP_31-12	RO-Zero

Port VC Capability Register 2 (Offset 08h) — DWORD

a. VC Arbitration Capability	RO
b. RsvdP_23-8	RO-Zero
c. VC Arbitration Table Offset	RO

Port VC Control Register (Offset 0Ch) — WORD

a. Load VC Arbitration Table	RO-Zero
b. VC Arbitration Select (if more than one VC in the LPVC group is not enabled)	

(for non-FLR testing) RW
(for FLR testing) RWS
(if more than one VC in the LPVC group is enabled) RO
(only those values in VC Arbitration Capability are written)

c. RsvdP_15-4 RO-Zero

Port VC Status Register (Offset 0Eh) — WORD

a. VC Arbitration Table Status RO
b. RsvdZ_15-1 RO-Zero

23. For each VC Resource register set instance Number [n] (from 0 to [NVC]), the following register field characteristic checks and register field default value checks are performed:

VC Resource Capability Register (n) (Offset 10h + n * 0Ch) — DWORD

a. Function Arbitration Capability RO
b. RsvdP_15-8 RO-Zero
c. Maximum Time Slots
(for non-FLR testing) HwInit
(for FLR testing) RO
d. RsvdP_23 RO-Zero
e. Function Arbitration Table Offset RO

VC Resource Control Register (n) (Offset 14h + n * 0Ch) — DWORD

a. TC/VC Map
(for VC0: bit 0) RO-Ones
(for non-VC0: bit 0) RO-Zero
(bits 7-1)
(for non-FLR testing) RW
(for FLR testing) RWS
b. RsvdP_15-8 RO-Zero
c. Load Function Arbitration Table RO-Zero
d. Function Arbitration Select
(for non-FLR testing) RW
(for FLR testing) RWS
(only those values in Port Arbitration Capability are written)
e. RsvdP_23-20 RO-Zero
f. VC ID
(for VC0) RO-Zero
(for all non VC0)
(for non-FLR testing) RW
(for FLR testing) RWS
g. RsvdP_30-27 RO-Zero
h. VC Enable
(for VC0) RO
(for all non-VC0)
(for non-FLR testing) RW
(for FLR testing) RWS

Reserved Register (n) (Offset 18h + n * 0Ch) — WORD

a. RsvdP_15-0 RO-Zero

VC Resource Status Register (n) (Offset 1Ah + n * 0Ch) — WORD

a. Function Arbitration Table Status	RO
b. VC Negotiation Pending	RO
c. RsvdZ_15-2	RO-Zero

VC Resource Control Register (n) Default Value (Offset 14h + n * 0Ch) — DWORD

a. TC/VC Map	
(for VC0)	FFh
(for all non VC0)	00h
b. VC Enable	
(for VC0)	1
(for all non-VC0)	0

24. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
25. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one Multi-Function Virtual Channel Extended Capability structure is present.
- ❑ A VF contains a Multi-Function Virtual Channel Extended Capability structure.
- ❑ An RCRB contains a Multi-Function Virtual Channel Extended Capability structure
- ❑ A Multi-Function Virtual Channel Extended Capability structure is present anywhere except in function 0 in the Upstream Port of a multi-function device.
- ❑ The Capability Version field does not report 1h.
- ❑ The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- ❑ The Low Priority Extended VC Count field is greater than the Extended VC Count field (Port VC Capability Register 1).
- ❑ The Reference Clock field is non-zero (Port VC Capability Register 1).
- ❑ The VC Arbitration Capability field contains a reserved value.
- ❑ The VC Arbitration Capability field contains a zero value and the Low Priority Extended VC Count field is non-zero.
- ❑ The VC Arbitration Capability field contains a non-zero value and the Low Priority Extended VC count field is zero.
- ❑ The VC Arbitration Table Offset field value is too small when the VC Arbitration Table Offset is non-zero.

- ❑ The VC Arbitration Table Status field reads non-zero by default.
- ❑ The default VC Arbitration Select field value is a WRR based arbitration method and the non-FLR default VC Arbitration table values are not all zero when the VC Arbitration Table Offset is non-zero.
- ❑ A valid VC Arbitration Select field value cannot be written.
- ❑ The VC Arbitration table cannot be written when the VC Arbitration Table Offset is non-zero.
- ❑ VC Resource Control, VC Resource Status, and VC Resource Capability registers are not present for each VC supported by the function (as indicated by Extended VC Count field).
- ❑ Any of the described VC Resource Control and VC Resource Status register value checks are not met:
 - The Function Arbitration Capability field contains a reserved value
 - The Function Arbitration Table Offset field value is too small when the Function Arbitration Table Offset field is non-zero
 - The TC/VC Map field non-FLR default value is not FFh for VC0
 - The TC/VC Map field non-FLR default value is not 00h for any VCn other than VC0
 - The VC_ID field is not 000b for VC0
 - The VC Enable field is not 1 for VC0
 - A valid Function Arbitration Select field value cannot be written
 - The Function Arbitration Table Status field reads non-zero by default.
 - The Function Arbitration table cannot be written when the Function Arbitration Table Offset field is non-zero.
- ❑ Any of the register field characteristic tests fail.
- ❑ Any of the default value tests fail.

The test *warns* if:

- ❑ The VC Arbitration Table Offset field is zero when WRR based VC Arbitration Capabilities are supported.
- ❑ Any of the described VC Resource Control and VC Resource Status register value checks are not met:
 - The Function Arbitration Table Offset field is zero when WRR based Function Arbitration Capabilities are supported.

2.2.25. TD_1_52 Vendor-Specific Capability Structure

The test verifies that if a function under test reports a Vendor-Specific Capability structure, it is implemented as defined in the relevant specifications.

Relevant Specifications

- ❑ *PCI Express Base Specification*
- ❑ *PCI Local Bus Specification, Revision 3.0 (Base 3.x or earlier only)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps:

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Capability ID field for each of the function's Capability structures. Determine how many instances of the Capability ID of 09h (Vendor-Specific Capability) are found.
3. If the Capability ID of 09h is found in a Capability structure, the following steps are performed for each instance of that Capability structure. If the Capability ID of 09h is not found in a Capability structure, the test skips to step 9.
4. The Next Capability Pointer field must be 00h or greater than 3Fh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
5. If the Next Capability Pointer field is non-zero, it must be a value less than the starting offset of this Capability structure by at least 4 bytes or must be larger than the starting offset of this Capability structure plus the Capability Length field value rounded to the next highest DWORD boundary. If not, this is recorded as a failure, but the test continues.
6. The value for Capability Length field must be at least 03h (3 bytes). If not, this is recorded as a failure, but the test continues.
7. If the Capability Length field is greater than 03h, test software reads each byte starting at offset 03h, and continuing until the byte length given by the value in the Capability Length field is reached. (This checks that Vendor-Specific registers can be read safely. No check on the returned data value is done.)
8. The following register field characteristic checks are performed:

 Vendor-Specific Capability Header (Offset 00h) — WORD

 a. Capability ID RO
 b. Next Capability Pointer RO

 Capability Length (Offset 02h) — BYTE RO
9. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- A non-zero Next Capability Pointer field is less than or equal to 3Fh, or the lower 2 bits are non-zero.
- The Next Capability Pointer field, when non-zero, is not at least 4 bytes less than the current Capability offset or it is less than the current Capability offset plus the Capability Length field value rounded to the next highest DWORD boundary.

- The Capability Length field is less than 3.
- Any of the register field characteristic tests fail.

2.2.26. TD_1_20 Vendor-Specific Extended Capability Structure

The test verifies that if a function under test reports a PCI Express Vendor-Specific Extended Capability structure, it is implemented as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.
This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps:

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 000Bh (Vendor-Specific Extended Capability) are found.
3. If the Extended Capability ID of 000Bh is found in an Extended Capability structure for an RCRB the following checks are performed:
 a. Examine the Extended Capability ID field for each of the RCRB's Extended Capability structures. Determine how many instances of the Extended Capability ID of 000Ah (RCRB Header Extended Capability) are found. If none are found, the test terminates with a failure.
4. If the Extended Capability ID of 000Bh is found in an Extended Capability structure, the following steps are performed for each instance of that Extended Capability structure. If the Extended Capability ID of 000Bh is not found in an Extended Capability structure, the test skips to step 11.
5. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
6. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
7. If the Next Capability Offset field is non-zero, it must return a value less than the starting offset of this Extended Capability structure by at least 4 bytes or must be larger than the starting offset

of this Extended Capability structure plus the VSEC Length field value rounded to the next highest DWORD boundary. If not, this is recorded as a failure, but the test continues.

8. The value for the VSEC Length field must be at least 008h (8 bytes). If not, this is recorded as a failure, but the test continues.
9. If the VSEC Length field is greater than 008h, test software reads each byte starting at offset 08h, and continuing until the byte length given by the value in the VSEC Length field is reached. (This checks that Vendor-Specific registers can be read safely. No check on the returned data value is done.)
10. The following register field characteristic checks are performed:

Vendor-Specific Capability Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

Vendor-Specific Header (Offset 04h) — DWORD

a. VSEC ID	RO
b. VSEC Rev	RO
c. VSEC Length	RO

11. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
12. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ An RCRB contains a Vendor-Specific Extended Capability structure, but does not contain an RCRB Header capability structure.
- ❑ The Capability Version field does not report 1h.
- ❑ The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- ❑ The Next Capability Offset field, when non-zero, is not at least 4 bytes less than the current Extended Capability offset or it is less than the current Extended Capability offset plus the VSEC Length field value rounded to the next highest DWORD boundary.
- ❑ The VSEC Length field is less than 8.
- ❑ Any of the register field characteristic tests fail.

2.2.27. TD_1_68 Designated Vendor-Specific Extended Capability Structure

The test verifies that if a function under test reports a PCI Express Designated Vendor-Specific Extended Capability structure, it is implemented as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *ECN Designated Vendor-Specific Extended Capability (to Base 3.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.
This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps:

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0023h (Designated Vendor-Specific Extended Capability) are found.
3. For Base 2.x or earlier testing: if the Extended Capability ID of 0023h is found in an Extended Capability structure, the test terminates with a failure.
4. For Base 3.x or later testing: if the Extended Capability ID of 0023h is found in an Extended Capability structure, the following steps are performed for each instance of that Extended Capability structure. If the Extended Capability ID of 0023h is not found in an Extended Capability structure, the test skips to step 12.
5. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
6. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
7. If the Next Capability Offset field is non-zero, it must return a value less than the starting offset of this Extended Capability structure by at least 4 bytes or must be larger than the starting offset of this Extended Capability structure plus the DVSEC Length field value rounded to the next highest DWORD boundary. If not, this is recorded as a failure, but the test continues.
8. The DVSEC Vendor ID field must return a valid value assigned by the PCI-SIG. If not, this is recorded as a failure, but the test continues. (For the purposes of this test program, reads of the DVSEC Vendor ID field must not return 0000h, FFFFh, or 0001h (CRS Software Visibility notification).)

9. The value for the DVSEC Length field must be at least 00Ah (10 bytes). If not, this is recorded as a failure, but the test continues.
10. If the DVSEC Length field is greater than 00Ah, test software reads each byte starting at offset 0Ah, and continuing until the byte length given by the value in the DVSEC Length field is reached. (This checks that Designated Vendor-Specific registers can be read safely. No check on the returned data value is done.)
11. The following register field characteristic checks are performed:

 Designated Vendor-Specific Capability Extended Capability Header (Offset 00h) — DWORD

 a. PCI Express Extended Capability ID — RO
 b. Capability Version — RO
 c. Next Capability Offset — RO

 Designated Vendor-Specific Header 1 (Offset 04h) — DWORD

 a. DVSEC Vendor ID — RO
 b. DVSEC Revision — RO
 c. DVSEC Length — RO

 Designated Vendor-Specific Header 2 (Offset 08h) — WORD

 a. DVSEC ID — RO

12. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
13. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ The Capability Version field does not report 1h.
- ❑ The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- ❑ The Next Capability Offset field, when non-zero, is not at least 4 bytes less than the current Extended Capability offset or it is less than the current Extended Capability offset plus the DVSEC Length field value rounded to the next highest DWORD boundary.
- ❑ The DVSEC Vendor ID field returns 0000h, or FFFFh, or 0001h.
- ❑ The DVSEC Length field is less than 10.
- ❑ Any of the register field characteristic tests fail.

2.2.28. TD_1_70 Null Capability Structure

The test verifies that if a function under test reports a Null Capability structure, it is implemented as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *PCI Code and ID Assignment, Revision 1.1 (or later)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps:

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Capability ID field for each of the function's Capability structures. Determine how many instances of the Capability ID of 00h (Null Capability) are found.
3. If the Capability ID of 00h is found in a Capability structure, the following steps are performed for each instance of that Capability structure. If the Capability ID of 00h is not found in a Capability structure, the test skips to step 7.
4. The Next Capability Pointer field must be 00h or greater than 3Fh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
5. If the Next Capability Pointer field is non-zero, it must be a value less than the starting offset of this Capability structure by at least 4 bytes or must be larger than it by at least 4 bytes. If not, this is recorded as a failure, but the test continues.
6. The following register field characteristic checks are performed:

 Null Capability Header (Offset 00h) — WORD

 a. Capability ID — RO
 b. Next Capability Pointer — RO

7. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- A non-zero Next Capability Pointer field is less than or equal to 3Fh, or the lower 2 bits are non-zero.

- The Next Capability Pointer field, when non-zero, is not at least 4 bytes less than the current Capability offset or at least 4 bytes greater.
- Any of the register field characteristic tests fail.

2.2.29. TD_1_71 Null Extended Capability Structure

The test verifies that if a function under test reports a PCI Express Null Extended Capability structure, it is implemented as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *PCI Code and ID Assignment, Revision 1.1 (or later)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps:

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0000h (Null Extended Capability) are found.
3. If the Extended Capability ID of 0000h is found in an Extended Capability structure, the following steps are performed for each instance of that Extended Capability structure.
4. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
5. If the Next Capability Offset field is non-zero, it must return a value less than the starting offset of this Extended Capability structure by at least 4 bytes or must be larger than it by at least 4 bytes. If not, this is recorded as a failure, but the test continues.
6. The following register field characteristic checks are performed:

 Null Capability Extended Capability Header (Offset 00h) — DWORD

 a. PCI Express Extended Capability ID — RO
 b. Capability Version — RO
 c. Next Capability Offset — RO

7. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.

b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

8. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- The Next Capability Offset field, when non-zero, is not at least 4 bytes less than the current Extended Capability offset or at least 4 bytes greater.
- Any of the register field characteristic tests fail.

2.2.30. TD_1_21 BIST Register

This test verifies that the function under test implements the BIST register as defined in the relevant specifications. (This tests both the case where HW BIST is implemented and the case where HW BIST is not implemented.)

Relevant Specifications

- *PCI Express Base Specification*
- *PCI Local Bus Specification (Base 3.x or earlier only)*
- *Single Root I/O Virtualization and Sharing Specification (Base 3.x or earlier only)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Read the byte from location 0Fh (BIST register) in configuration space.
3. If the BIST Capable field is 0, the following checks are performed and if any are not as stated, this is recorded as a failure, but the test continues:
 a. Write a 1 to Bit 6 (Start BIST field) to see it has no effect.
 b. Immediately read the BIST register and check the following:
 i. Bit 6 (Start BIST field) must be zero.
 ii. Bits 3-0 (Completion Code field) must return zero.
 iii. Bits 5-4 (Reserved field) must return zero.

4. For non-VFs, if the BIST Capable field is 1, the following checks are performed and if any are not as stated, this is recorded as a failure, but the test continues:
 a. Write a 1 to Bit 6 (Start BIST field) to invoke BIST.
 b. After 2 seconds, read the BIST register and check the following:
 i. Bit 6 (Start BIST field) must be zero.
 ii. Bits 3-0 (Completion Code field) must return zero.
 iii. Bits 5-4 (Reserved field) must return zero.

5. The following register field characteristic checks are performed:

BIST Register (Location 0Fh) — BYTE

a. Completion Code	
(if BIST Capable is 1)	RO
(if BIST Capable is 0)	RO-Zero
b. RsvdP_5-4	RO-Zero
c. Start BIST	
(if BIST Capable is 0)	RO-Zero
d. BIST Capable	
(For Base 4.x or later testing)	
(for VFs)	RO-Zero
(otherwise)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
(For Base 3.x or earlier testing)	
(for VFs)	RO-Zero
(otherwise)	RO

6. The following default value checks are performed:

BIST Register Default Value (Location 0Fh) — BYTE

a. Completion Code	0000b
b. Start BIST	0

7. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- ❑ If the BIST Capable field is 0 and immediately after writing 1 to the Start BIST field, reading the BIST register returns non-zero values for the following fields: Completion Code, Reserved, or Start BIST.
- ❑ If the BIST Capable field is 1 and 2 seconds after writing 1 to the Start BIST field, reading the BIST register returns non-zero values for the following fields: Completion Code, Reserved, or Start BIST.
- ❑ Any of the register field characteristic tests fail.
- ❑ Any of the default value tests fail.

2.2.31. TD_1_22 Slot Numbering Capability Structure

The test verifies that if the function under test reports a Slot Numbering capability, it is implemented as defined in the relevant specifications. (Since this Capability structure may only be present in a PCI Express to PCI/PCI-X Bridge, the test also checks that this Capability structure is not present in other device types.)

Relevant Specifications

- *PCI Local Bus Specification, Revision 3.0*
- *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0*
- *PCI-to-PCI Bridge Architecture Specification, Revision 1.2*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Capability ID field for each of the function's Capability structures. Determine how many instances of the Capability ID of 04h (Slot Numbering Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Capability ID of 04h is found in a Capability structure for a device that is not a Root Port, Switch Downstream Port, not a PCI/PCI-X to PCI Express Bridge, and not a PCI Express to PCI/PCI-X Bridge (a device with a slot), the test terminates with a failure.
4. If the Capability ID of 04h is found in a Capability structure, the function's Slot Implemented field (PCI Express Capabilities register) must return 1. If not, this is recorded as a failure, but the test continues.
5. If the Capability ID of 04h is found in a Capability structure, the following steps are performed on that Capability structure. If the Capability ID of 04h is not found in a Capability structure, the test skips to step 9.
6. The Next Capability Pointer field must be 00h or greater than 3Fh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
7. Read the WORD from offset 02h (Expansion Slot and Chassis Number registers). If Bit 5 (First in Chassis field) is set, the Chassis Number register must be non-zero and unique. If not, this is recorded as a failure, but the test continues. (For the purposes of this test, a non-zero value is assumed unique.)
8. The following register field characteristic checks are performed:

Slot Numbering Capability Header (Offset 00h) — WORD

a. Capability ID RO
b. Next Capability Pointer RO

Expansion Slot Register (Offset 02h) — BYTE

a. Expansion Slots Provided
 (for non-FLR testing) HwInit
 (for FLR testing) RO
b. First in Chassis
 (for non-FLR testing) HwInit
 (for FLR testing) RO
c. Reserved_7-6 RO-Zero

Chassis Number Register (Offset 03h) — BYTE

a. Chassis Number RW

9. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- ❑ More than one Slot Numbering Capability structure is present.
- ❑ For devices other than Root Port, Switch Downstream Port, PCI/PCI-X to PCI Express Bridge or PCI Express to PCI/PCI-X Bridge, the Slot Numbering capability is present.
- ❑ The Slot Implemented field is 0, when the Slot Numbering capability is present.
- ❑ A non-zero Next Capability Pointer field is less than or equal to 3Fh, or the lower 2 bits are non-zero.
- ❑ For Root Port, Switch Downstream Port, PCI/PCI-X to PCI Express Bridge or PCI Express to PCI/PCI-X Bridge devices:
 - The Expansion Slots Provided field is zero
 - The Chassis Number register is zero and cannot be written with a non-zero value.
- ❑ Any of the register field characteristic tests fail.

2.2.32. TD_1_53 SSID/SSVID Capability Structure

The test verifies that if the function under test reports a SSID/SSVID (Subsystem ID/Subsystem Vendor ID) Capability, it is implemented as defined in the relevant specifications. (Since this Capability structure may only be present in a device with a Type 1 Configuration Space Header, the test also checks that this Capability structure is not present in other Configuration Space Header types.)

Relevant Specifications

- ❑ *PCI-to-PCI Bridge Architecture Specification, Revision 1.2*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Capability ID field for each of the function's Capability structures. Determine how many instances of the Capability ID of 0Dh (SSID/SSVID Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Capability ID of 0Dh is found in a Capability structure, read a byte from the function's location 0Eh (Header Type register) and perform the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The value in bits 6-0 must be 000 0001b (SSID/SSVID Capability may only be present in a device with a Type 1 Configuration Space Header).
4. If the Capability ID of 0Dh is found in a Capability structure, the following steps are performed on that Capability structure. If the Capability ID of 0Dh is not found in a Capability structure, the test skips to step 8.
5. The Next Capability Pointer field must be 00h or greater than 3Fh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
6. Read the WORD from offset 04h (SSVID register) and perform the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The Subsystem Vendor ID field must return a valid value assigned by the PCI-SIG. (For the purposes of this test program, a valid value is any value other than 0000h, or FFFFh, or 0001h.)
7. The following register field characteristic checks are performed:

 SSID/SSVID Capability Header (Offset 00h) — WORD

 a. Capability ID — RO
 b. Next Capability Pointer — RO

 Reserved Register (Offset 02h) — WORD

 a. Reserved_15-0 — RO-Zero

 SSVID Register (Offset 04h) — WORD

 a. SSVID — RO

 SSID Register (Offset 06h) — WORD

 a. SSID — RO

8. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.

c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- More than one SSID/SSVID Capability structure is present.
- For functions with a Configuration Space Header type that is not Type 1, the SSID/SSVID Capability structure is present.
- A non-zero Next Capability Pointer field is less than or equal to 3Fh, or the lower 2 bits are non-zero.
- The SSVID field returns 0000h, or FFFFh, or 0001h.
- Any of the register field characteristic tests fail.

2.2.33. TD_1_23 PCI Next Capability Pointer Register

The test verifies that the function under test implements the Next Capability Pointer registers fields as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *PCI Local Bus Specification, Revision 3.0 (Base 3.x or earlier only)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Read the WORD from location 06h (Status register) and if the Capabilities List field is 0, then the test terminates with a failure.
3. Read the byte from location 34h (Capabilities Pointer register) in the Configuration Space and perform the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The lower two bits must be zero (00b).
 b. The value read, if non-zero, must be greater than 3Fh and less than FDh.
 c. The value (with the lower two bits masked to 00b) is recorded in a table to check that subsequent Next Cap Pointers do not use the same value (creating a loop of pointers).
4. The current pointer value (with the lower two bits masked to 00b), if non-zero and if greater than 3Fh and less than FFh, is used to retrieve the Next Cap Pointer field of the capability that the capability pointer is indicating. Otherwise if the pointer is the end of list, skip to step 7.

5. If the Next Cap Pointer value is non-zero the following checks are performed and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The lower two bits must be zero (00b).
 b. The value read must be greater than 3Fh and less than FDh.
 c. The value (with the lower two bits masked to 00b) is recorded in a table to check that subsequent Next Cap Pointers do not use the same value (creating a loop of pointers).
6. Test software repeats steps 4-5 until:
 a. The Next Cap Pointer is zero, or
 b. The Value is not greater than 3Fh and less than FDh, or
 c. The current pointer value (with the lower two bits masked to 00b) was used by the Capabilities Pointer or a previous Next Cap Pointer (this stops any loop of pointers).
7. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- ❑ The Capability List field returns 0.
- ❑ Any capability pointer contains an invalid value (either the lower two bits are not 00b, or the value is not greater than 3Fh and less than FDh).
- ❑ The capability list contains a loop of pointers.

2.2.34. TD_1_24 PCI Express Next Extended Capability Pointer Register

The test verifies that the function under test implements the Next Extended Capability Pointer registers fields as defined in the relevant specifications.

Relevant Specifications

- ❑ *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.

2. If testing Extended Configuration Space, read the DWORD from location 100h in configuration space.
3. If testing RCRB, read the DWORD from offset 000h in the RCRB (in memory space).
4. If testing Extended Configuration Space, then if the value is not 0000 0000h, the following steps are performed. If the value is 0000 0000h (no Extended Capability structures present) skip to step 9.
5. If testing RCRB, then if the value is not 000x FFFFh (where x indicates that bits 19-16 are don't cares), the following steps are performed. If the value is 000x FFFFh (no Extended Capability structures present) skip to step 9.
6. If the Next Capability Offset field value is not 000h, the following checks are performed and if any are not as stated, this is recorded as a failure, but the test continues. If the value is 000h (no further Extended Capability structures present), skip to step 9.
 a. The lower two bits must be zero (00b).
 b. The value read must be greater than 107h and less than FF9h.
 c. The value (with the lower two bits masked to 00b) is recorded in a table to check that subsequent Next Capability Offsets do not use the same value (creating a loop of pointers).
7. The current pointer value (with the lower two bits masked to 00b), if non-zero and if greater than 107h and less than FF9h, is used to retrieve the Next Capability Offset of the Extended Capability structure that the Extended Capabilities Pointer is indicating. Otherwise if the pointer is the end of list, skip to step 9.
8. Read the DWORD from the offset indicated in the current Next Capability Offset. Test software repeats steps 4-7 until:
 a. The Next Capability Offset is 000h, or
 b. The Value is not greater than 107h and less than FF9h, or
 c. The current pointer value (with the lower two bits masked to 00b) was used by a previous Next Capability Offset (this stops any loop of pointers).
9. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
10. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ Any Next Capability Offset contains an invalid value (either the lower two bits are not 00b, or the value is not greater than 107h and less than FF9h).
- ❑ The capability list contains a loop of pointers.

2.2.35. TD_1_25 Misc Type 0 Config Space Header Registers

The test verifies that if the function under test reports a Type 0 Configuration Space Header, it implements the Vendor ID, Device ID, Revision ID, Class Code, Header Type, Cardbus CIS Pointer, Subsystem ID, Subsystem Vendor ID, and Expansion ROM Base Address registers as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *PCI Local Bus Specification, Revision 3.0 (Base 3.x or earlier only)*
- *Single Root I/O Virtualization and Sharing Specification (Base 3.x or earlier only)*
- *ECN Change Root Complex Event Collector Class Code (to Base 3.0)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Read a byte from location 0Eh (Header Type register) and perform the following checks:
 a. For Base 4.x or later testing, if the value in bits 6-0 is neither 000 0000b (Type 0 Configuration Space Header) nor 000 0001b (Type 1 Configuration Space Header), this is recorded as a failure and the test terminates.
 b. If the value in bits 6-0 is 000 0000b (Type 0 Configuration Space Header) the test continues. If not, the test terminates (this is not a failure and the test result is reported as skipped).
3. For a VF, the Multi-Function Device field (Header Type register) must be 0. If not, this is recorded as a failure, but the test continues.
4. Read a WORD from location 00h (Vendor ID register) and perform the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. For a VF, the Vendor ID field must return FFFFh.
 b. For a non-VF, the Vendor ID field must return a valid value assigned by the PCI-SIG. (For the purposes of this test program, reads of the Vendor ID field must not return 0000h, FFFFh, or 0001h (CRS Software Visibility notification).)
5. Read 3 bytes from location 09h (Class Code register) and perform the following checks:
 a. For Base 3.x or later testing, if the Base Class Code field is 00h, then a warning message is issued, but this is not treated in itself as a failure.
 b. For Base 2.x or earlier testing, for device type of Root Complex Event Collector, the Base Class Code field must be 08h, the Sub-Class Code field must be 06h, and the Programming

Interface field (byte at 09h) must be 00h and if any are not as stated, this is recorded as a failure, but the test continues.

c. For Base 3.x or later testing, for device type of Root Complex Event Collector, the Base Class Code field must be 08h, the Sub-Class Code field must be 06h or 07h, and the Programming Interface field (byte at 09h) must be 00h and if any are not as stated, this is recorded as a failure, but the test continues.

d. For Base 3.x or later testing, for device type of Root Complex Event Collector, if the Base Class Code field is 08h, the Sub-Class Code field is 06h, and the Programming Interface field (byte at 09h) is 00h, then a warning message is issued, but this is not treated in itself as a failure.

6. Read a WORD from location 2Ch (Subsystem Vendor ID register) and perform the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. If the function is neither Base Class 06h, Sub-Class 00h-04h nor Base Class 08h, Sub-Class 00h-03h, then the Subsystem Vendor ID field must return a valid value assigned by the PCI-SIG. (For the purposes of this test program, a valid value is any value other than 0000h, FFFFh, or 0001h (CRS Software Visibility notification).)

7. Test software writes FFFF FFFFh to the Expansion ROM Base Address (location 30h for Type 0 Configuration Space Header) register and then reads back the same register and if it is zero the test skips to step 12, but if it is non-zero, the following checks are performed:
 a. The function under test must not be a VF. If it is a VF, a failure is reported, but testing continues at step 12.
 b. Bit 0 (Expansion ROM Enable field) must return 1. If not, this is recorded as a failure, but the test continues.
 c. Bit 24 must return 1 (ROM BAR must claim 16 MB or less). If not, this is recorded as a failure, but the test continues.
 d. Starting at bit 11 determine the least significant bit value that is set to 1 and record it in Least Significant Bit [LSB]. [LSB] must be less than 25. All bits from 31 to [LSB] must also be 1. This same [LSB] value is used in subsequent tests.

8. Test software writes 5555 5555h to the ROM BAR and then reads back the same register. Bits 31-[LSB] must return the written value. Bits [LSB]-11 must return all 0. If any do not this is recorded as a failure, but the test continues.

9. Test software writes AAAA AAAAh to the ROM BAR and then reads back the same register. Bits 31-[LSB] must return the written value. Bits [LSB]-11 must return all 0. If any do not this is recorded as a failure, but the test continues.

10. Test software writes CCCC CCCCh to the ROM BAR and then reads back the same register. Bits 31-[LSB] must return the written value. Bits [LSB]-11 must return all 0. If any do not this is recorded as a failure, but the test continues.

11. Test software writes 0000 0000h to the ROM BAR and then reads back the same register. Bits 31-[LSB] must return the written value. Bits [LSB]-11 must return all 0. Bit 0 (Expansion ROM Enable) must return 0. If any do not this is recorded as a failure, but the test continues.

12. The following register field characteristic checks are performed:

Vendor ID Register (Location 00h) –– WORD

(For Base 4.x or later testing)
(for VFs) RO-Ones

(otherwise)
(for non-FLR testing) HwInit
(for FLR testing) RO
(For Base 3.x or earlier testing)
(for VFs) RO-Ones
(otherwise) RO

Device ID Register (Location 02h) — WORD
(For Base 4.x or later testing)
(for VFs) RO-Ones
(otherwise)
(for non-FLR testing) HwInit
(for FLR testing) RO
(For Base 3.x or earlier testing)
(for VFs) RO-Ones
(otherwise) RO

Revision ID Register (Location 08h) – BYTE
(For Base 4.x or later testing)
(for non-FLR testing) HwInit
(for FLR testing) RO
(For Base 3.x or earlier testing) RO

Class Code Register (Location 09h) — 3 BYTES
a. Programming Interface RO
b. Sub-Class Code RO
c. Base Class Code RO

Header Type Register (Location 0Eh) — BYTE
(For Base 4.x or later testing)
a. Header Layout RO
b. Multi-Function Device
(for VFs) RO-Zero
(otherwise) RO
(For Base 3.x or earlier testing)
(for VFs) RO-Zero
(otherwise) RO

Cardbus CIS Pointer Register (Location 28h) — DWORD
(For Base 4.x or later testing) RO-Zero
(For Base 3.x or earlier testing)
(for VFs) RO-Zero
(otherwise) RO

Subsystem Vendor ID Register (Location 2Ch) — WORD RO

Subsystem ID Register (Location 2Eh) — WORD RO

Expansion ROM Base Address Register (Location 30h) — DWORD
(for non-VFs and non-empty BAR)

a. Expansion ROM Enable — RW or RO-Zero
b. Reserved_10-1 — RO-Zero

Expansion ROM Base Address Register (Location 30h) — DWORD (for VFs)
a. Reserved_31-0 — RO-Zero

Capabilities Pointer Register (Location 34h) – BYTE — RO

Reserved Register (Location 35h) — 3 BYTES
a. Reserved_23-0 — RO-Zero

Reserved Register (Location 38h) — DWORD
a. Reserved_31-0 — RO-Zero

13. The following default value checks are performed:

Header Type Register Default Value (Location 0Eh) — BYTE (For Base 4.x or later testing)
a. Header Layout — 000 0000b

Expansion ROM Base Address Register Default Value (Location 30h) — DWORD
a. Expansion ROM Enable — 0

14. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- ❑ The Header Layout field returns other than 000 0000b or 000 0001b (for Base 4.x or later testing only).
- ❑ For a VF, the Multi-Function Device field returns 1.
- ❑ For a VF, the Vendor ID field returns other than FFFFh.
- ❑ For a non-VF, the Vendor ID field returns 0000h, or FFFFh, or 0001h.
- ❑ For a Root Complex Event Collector, the Class Code field is not 08 0600h (for Base 2.x or earlier testing only).
- ❑ For a Root Complex Event Collector, the Class Code field is neither 08 0700h nor 08 0600h (for Base 3.x or later testing only).
- ❑ The Subsystem Vendor ID field returns 0000h or FFFFh and Base Class/Sub-Class is not one of the following: 06h/00h-04h; 08h/00h-03h.
- ❑ For a VF, Expansion ROM BAR returns a non-zero value.
- ❑ If implemented, Expansion ROM BAR claims more than 16 MB of space.
- ❑ If implemented, Expansion ROM BAR does not return contiguous 1's across all implemented address bits.

- If implemented, Expansion ROM BAR does not implement RW bits across all implemented address bits.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

The test *warns* if:

- The Base Class Code field is 00h (for Base 3.x or later testing only).
- For a Root Complex Event Collector, the Class Code field is not 08 0700h (for Base 3.x or later testing only).

2.2.36. TD_1_26 Misc Type 1 Config Space Header Registers

The test verifies that if the function under test reports a Type 1 Configuration Space Header, it implements the Vendor ID, Device ID, Revision ID, Class Code, Header Type, I/O Base, I/O Limit, I/O Base Upper 16 Bits, I/O Limit Upper 16 Bits, Memory Base, Memory Limit, Prefetchable Memory Base, Prefetchable Memory Limit, Prefetchable Base Upper 32 Bits, Prefetchable Limit Upper 32 Bits, and Expansion ROM Base Address registers as defined in the relevant specifications. (The following registers are not tested because they control the Configuration Space decoding and may interfere with system operation: Primary Bus Number; Secondary Bus Number; Subordinate Bus Number.)

Relevant Specifications

- *PCI Express Base Specification*
- *PCI Local Bus Specification, Revision 3.0 (Base 3.x or earlier only)*
- *PCI-to-PCI Bridge Architecture Specification, Revision 1.2 (Base 3.x or earlier only)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types implementing Type 1 Configuration Space Headers.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Read a byte from location 0Eh (Header Type register) and perform the following checks:
 a. For Base 4.x or later testing, if the value in bits 6-0 is neither 000 0000b (Type 0 Configuration Space Header) nor 000 0001b (Type 1 Configuration Space Header), this is recorded as a failure and the test terminates.
 b. If the value in bits 6-0 is 000 0001b (Type 1 Configuration Space Header) the test continues. If not, the test terminates (this is not a failure and the test result is reported as skipped).

3. Read a WORD from location 00h (Vendor ID register) and perform the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The Vendor ID field must return a valid value assigned by the PCI-SIG. (For the purposes of this test program, reads of the Vendor ID field must not return 0000h, FFFFh, or 0001h (CRS Software Visibility notification).)
4. Read 3 bytes from location 09h (Class Code registers) and perform the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. For Base 3.x or later testing, if the Base Class Code field is 00h, then a warning message is issued, but this is not treated in itself as a failure.
 b. For a device type that is a Root Port, a Switch Upstream Port, a Switch Downstream Port, a PCI Express to PCI/PCI-X Bridge or a PCI/PCI-X to PCI Express Bridge, the Base Class Code field (byte at 0Bh) must be 06h and the Sub-Class Code field (byte at 0Ah) must be 04h.
5. Test software reads and saves (for later restoration) the values in the following registers: I/O Base; I/O Limit; I/O Base Upper 16 Bits; I/O Limit Upper 16 Bits.
6. Test software writes the I/O Space Enable field (Command register) with 1 and then reads it back. If it returns 0, then the fact that this function does not support I/O Space decoding is recorded. Otherwise if the value returns 1 it is recorded that the function supports I/O Space decoding.
7. Test software writes the I/O Space Enable field (Command register) with 0 (to disable I/O Space decoding if supported).
8. If the function does not support I/O Space decoding then the following tests are performed:
 a. Test software writes a byte of FFh to the I/O Base register (location 1Ch) and then reads back a byte from the same location and if it does not return 00h, the test fails and this is recorded as a failure, but the test continues.
 b. Test software writes a byte of FFh to the I/O Limit register (location 1Dh) and then reads back a byte from the same location and if it does not return 00h, the test fails and this is recorded as a failure, but the test continues.
 c. Test software writes a WORD of FFFFh to the I/O Base Upper 16 Bits register (location 30h) and then reads back a WORD from the same location and if it does not return 0000h, the test fails and this is recorded as a failure, but the test continues.
 d. Test software writes a WORD of FFFFh to the I/O Limit Upper 16 Bits register (location 32h) and then reads back a WORD from the same location and if it does not return 0000h, the test fails and this is recorded as a failure, but the test continues.
 e. Test software reads a DWORD at location 10h (BAR0) and if bit 0 is not 0, then the test fails and this is recorded as a failure, but the test continues (if the I/O Space Enable field is RO-Zero, the function cannot claim any I/O Space via BARs).
 f. Test software reads a DWORD at location 14h (BAR1) and if bit 0 is not 0, then the test fails and this is recorded as a failure, but the test continues (if the I/O Space Enable field is RO-Zero, the function cannot claim any I/O Space via BARs).
9. If the function supports I/O Space decoding then the following tests are performed:
 a. Test software reads the byte from the I/O Base register (location 1Ch) and saves this value as [IOV].

b. Test software reads the byte from the I/O Limit register (location 1Dh) and compares bits 3-0 of this result with bits 3-0 of [IOV]. If bits 3-0 of the two results are not the same value, the test fails and this is recorded as a failure, but the test continues.
c. Test software verifies that bits 3-0 of [IOV] contain a valid value (0h or 1h). If an invalid value is returned, the test fails and this is recorded as a failure, but the test continues.
d. Test software looks at the value of bits 3-0 of [IOV] and if it is 1h, it records that 32 bit I/O Space addressing is supported.
e. Test software looks at the value of bits 3-0 of [IOV] and if it is 0h, it writes a byte of FFh to the I/O Base register (location 1Ch) and then reads back a byte from the same location and checks that bits 7-4 are non-zero. If they are non-zero it records that 16 bit I/O Space addressing is supported. Otherwise it reads back the DWORD at location 10h (BAR 0) and if bit 0 is not 1, it then reads back the DWORD at location 14h (BAR1) and if bit 0 is also not 1, the test fails and this is recorded as a failure, but the test continues (I/O Space Enable must be RO-Zero if neither I/O BAR nor I/O address ranges are supported).

10. If the function supports 16 bit I/O Space addressing then the following tests are performed:
 a. Test software writes a byte of FFh to the I/O Base register (location 1Ch) and then reads back a byte from the same location and checks the returned value as follows: bits 7-4 return bits 7-4 of the value written; bits 3-0 return the same value as the previously recorded [IOV]. If any of these are not true, the test fails and this is recorded as a failure, while the test continues at the next step. Otherwise repeat this step using the following write values: 55h; AAh; CCh; 00h.
 b. Test software writes a byte of FFh to the I/O Limit register (location 1Dh) and then reads back a byte from the same location and checks the returned value as follows: bits 7-4 return bits 7-4 of the value written; bits 3-0 return the same value as the previously recorded [IOV]. If any of these are not true, the test fails and this is recorded as a failure, while the test continues at the next step. Otherwise repeat this step using the following write values: 55h; AAh; CCh; 00h.
 c. Test software writes a WORD of FFFFh to the I/O Base Upper 16 Bits register (location 30h) and then reads back a WORD from the same location and if it does not return 0000h, the test fails and this is recorded as a failure, but the test continues.
 d. Test software writes a WORD of FFFFh to the I/O Limit Upper 16 Bits register (location 32h) and then reads back a WORD from the same location and if it does not return 0000h, the test fails and this is recorded as a failure, but the test continues.

11. If the function supports 32 bit I/O Space addressing then the following tests are performed:
 a. Test software writes a byte of FFh to the I/O Base register (location 1Ch) and then reads back a byte from the same location and checks the returned value as follows: bits 7-4 return bits 7-4 of the value written; bits 3-0 return the same value as the previously recorded [IOV]. If any of these are not true, the test fails and this is recorded as a failure, while the test continues at the next step. Otherwise repeat this step using the following write values: 55h; AAh; CCh; 00h.
 b. Test software writes a byte of FFh to the I/O Limit register (location 1Dh) and then reads back a byte from the same location and checks the returned value as follows: bits 7-4 return bits 7-4 of the value written; bits 3-0 return the same value as the previously recorded [IOV]. If any of these are not true, the test fails and this is recorded as a failure, while the test continues at the next step. Otherwise repeat this step using the following write values: 55h; AAh; CCh; 00h.

c. Test software writes a WORD of FFFFh to the I/O Base Upper 16 Bits register (location 30h) and then reads back a WORD from the same location and if it does not return the value written, the test fails and this is recorded as a failure, while the test continues at the next step. Otherwise repeat this step using the following write values: 5555h; AAAAh; CCCCh; 0000h.
d. Test software writes a WORD of FFFFh to the I/O Limit Upper 16 Bits register (location 32h) and then reads back a WORD from the same location and if it does not return the value written, the test fails and this is recorded as a failure, while the test continues at the next step. Otherwise repeat this step using the following write values: 5555h; AAAAh; CCCCh; 0000h.

12. Test software restores the previously saved (in step 5) values to the following registers: I/O Base; I/O Limit; I/O Base Upper 16 Bits; I/O Limit Upper 16 Bits.
13. Test software reads and saves (for later restoration) the values in the following registers: Memory Base; Memory Limit.
14. Test software writes the Memory Space Enable field (Command register) with 0 (to disable Memory Space decoding).
15. The following tests are performed:
 a. Test software writes a WORD of FFFFh to the Memory Base register (location 20h) and then reads back a WORD from the same location and checks the returned value as follows: bits 15-4 return bits 15-4 of the value written; bits 3-0 return 0h. If any of these are not true, the test fails and this is recorded as a failure, while the test continues at the next step. Otherwise repeat this step using the following write values: 5555h; AAAAh; CCCCh; 0000h.
 b. Test software writes a WORD of FFFFh to the Memory Limit register (location 22h) and then reads back a WORD from the same location and checks the returned value as follows: bits 15-4 return bits 15-4 of the value written; bits 3-0 return 0h. If any of these are not true, the test fails and this is recorded as a failure, while the test continues at the next step. Otherwise repeat this step using the following write values: 5555h; AAAAh; CCCCh; 0000h.
16. Test software restores the previously saved (in step 13) values to the following registers: Memory Base; Memory Limit.
17. Test software reads and saves (for later restoration) the values in the following registers: Prefetchable Memory Base; Prefetchable Memory Limit; Prefetchable Base Upper 32 Bits; Prefetchable Limit Upper 32 Bits.
18. Test software writes the Memory Space Enable field (Command register) with 1 and then reads it back. If it returns 0, then the test fails and this is recorded as a failure, but the test continues, after recording that the function does not support Memory Space decoding. Otherwise if the value returns 1 it is recorded that the function supports Memory Space decoding.
19. Test software writes the Memory Space Enable field (Command register) with 0 (to disable Memory Space decoding).
20. If the function supports Memory Space decoding then the following tests are performed:
 a. Test software reads the WORD from the Prefetchable Memory Base register (location 24h) and saves this value as [PMEMV].

b. Test software reads the WORD from the Prefetchable Memory Limit register (location 26h) and compares bits 3-0 of this result with bits 3-0 of [PMEMV]. If bits 3-0 of the two results are not the same value the test fails and this is recorded as a failure, while the test continues at step 24.
c. Test software verifies that bits 3-0 of [PMEMV] contain a valid value (0h or 1h). If an invalid value is returned, the test fails and this is recorded as a failure, while the test continues at step 24.
d. Test software looks at the value of bits 3-0 of [PMEMV] and if it is 1h, it records that 64 bit Prefetchable Memory Space addressing is supported.
e. Test software looks at the value of bits 3-0 of [PMEMV] and if it is 0h, it writes a WORD of FFFFh to the Prefetchable Memory Base register (location 24h) and then reads back the same location and checks that bits 15-4 are non-zero. If they are non-zero it records that 32 bit Prefetchable Memory Space addressing is supported. Otherwise it records that Prefetchable Memory Space addressing is not supported.

21. If the function does not support Prefetchable Memory Space addressing then the following tests are performed:
 a. Test software writes a WORD of FFFFh to the Prefetchable Memory Base register (location 24h) and then reads back a WORD from the same location and if it does not return 0000h, the test fails and this is recorded as a failure, but the test continues.
 b. Test software writes a WORD of FFFFh to the Prefetchable Memory Limit register (location 26h) and then reads back a WORD from the same location and if it does not return 0000h, the test fails and this is recorded as a failure, but the test continues.
 c. Test software writes a DWORD of FFFF FFFFh to the Prefetchable Base Upper 32 Bits register (location 28h) and then reads back a DWORD from the same location and if it does not return 0000 0000h, the test fails and this is recorded as a failure, but the test continues.
 d. Test software writes a DWORD of FFFF FFFFh to the Prefetchable Limit Upper 32 Bits register (location 2Ch) and then reads back a DWORD from the same location and if it does not return 0000 0000h, the test fails and this is recorded as a failure, but the test continues.
22. If the function supports 32 bit Prefetchable Memory Space addressing then the following tests are performed:
 a. Test software writes a WORD of FFFFh to the Prefetchable Memory Base register (location 24h) and then reads back a WORD from the same location and checks the returned value as follows: bits 15-4 return bits 15-4 of the value written; bits 3-0 return the same value as the previously recorded [PMEMV]. If any of these are not true, the test fails and this is recorded as a failure, while the test continues at the next step. Otherwise repeat this step using the following write values: 5555h; AAAAh; CCCCh; 0000h.
 b. Test software writes a WORD of FFFFh to the Prefetchable Memory Limit register (location 26h) and then reads back a WORD from the same location and checks the returned value as follows: bits 15-4 return bits 15-4 of the value written; bits 3-0 return the same value as the previously recorded [PMEMV]. If any of these are not true, the test fails and this is recorded as a failure, while the test continues at the next step. Otherwise repeat this step using the following write values: 5555h; AAAAh; CCCCh; 0000h.
 c. Test software writes a DWORD of FFFF FFFFh to the Prefetchable Base Upper 32 Bits register (location 28h) and then reads back a DWORD from the same location and if it does not return 0000 0000h, the test fails and this is recorded as a failure, but the test continues.

d. Test software writes a DWORD of FFFF FFFFh to the Prefetchable Limit Upper 32 Bits register (location 2Ch) and then reads back a DWORD from the same location and if it does not return 0000 0000h, the test fails and this is recorded as a failure, but the test continues.

23. If the function supports 64 bit Prefetchable Memory Space addressing then the following tests are performed:
 a. Test software writes a WORD of FFFFh to the Prefetchable Memory Base register (location 24h) and then reads back a WORD from the same location and checks the returned value as follows: bits 15-4 return bits 15-4 of the value written; bits 3-0 return the same value as the previously recorded [PMEMV]. If any of these are not true, the test fails and this is recorded as a failure, while the test continues at the next step. Otherwise repeat this step using the following write values: 5555h; AAAAh; CCCCh; 0000h.
 b. Test software writes a WORD of FFFFh to the Prefetchable Memory Limit register (location 26h) and then reads back a WORD from the same location and checks the returned value as follows: bits 15-4 return bits 15-4 of the value written; bits 3-0 return the same value as the previously recorded [PMEMV]. If any of these are not true, the test fails and this is recorded as a failure, while the test continues at the next step. Otherwise repeat this step using the following write values: 5555h; AAAAh; CCCCh; 0000h.
 c. Test software writes a DWORD of FFFF FFFFh to the Prefetchable Base Upper 32 Bits register (location 28h) and then reads back a DWORD from the same location and if it does not return the value written, the test fails and this is recorded as a failure, while the test continues at the next step. Otherwise repeat this step using the following write values: 5555 5555h; AAAA AAAAh; CCCC CCCCh; 0000 0000h.
 d. Test software writes a DWORD of FFFF FFFFh to the Prefetchable Limit Upper 32 Bits register (location 2Ch) and then reads back a DWORD from the same location and if it does not return the value written, the test fails and this is recorded as a failure, while the test continues at the next step. Otherwise repeat this step using the following write values: 5555 5555h; AAAA AAAAh; CCCC CCCCh; 0000 0000h.

24. Test software restores the previously saved (in step 17) values to the following registers: Prefetchable Memory Base; Prefetchable Memory Limit; Prefetchable Base Upper 32 Bits; Prefetchable Limit Upper 32 Bits.

25. Test software writes FFFF FFFFh to the Expansion ROM Base Address register (location 38h for Type 1 Configuration Space Header) and then reads back a DWORD from the same register and if it is zero the test skips to step 30, but if it is non-zero, the following checks are performed and if any are not as stated, this is recorded as a failure, but the test continues:
 a. Bit 0 (Expansion ROM Enable field) must return 1.
 b. Bit 24 must return 1 (ROM BAR must claim 16 MB or less).
 c. Starting at bit 11 determine the least significant bit value that is set to 1 and record it in Least Significant Bit [LSB]. [LSB] must be less than 25. All bits from 31 to [LSB] must also be 1. This same [LSB] value is used in subsequent tests.

26. Test software writes 5555 5555h to the ROM BAR and then reads back a DWORD from the same register. Bits 31-[LSB] must return the written value. Bits [LSB]-11 must return all 0. If any do not this is recorded as a failure, but the test continues.

27. Test software writes AAAA AAAAh to the ROM BAR and then reads back a DWORD from the same register. Bits 31-[LSB] must return the written value. Bits [LSB]-11 must return all 0. If any do not this is recorded as a failure, but the test continues.

28. Test software writes CCCC CCCCh to the ROM BAR and then reads back a DWORD from the same register. Bits 31-[LSB] must return the written value. Bits [LSB]-11 must return all 0. If any do not this is recorded as a failure, but the test continues.
29. Test software writes 0000 0000h to the ROM BAR and then reads back a DWORD from the same register. Bits 31-[LSB] must return the written value. Bits [LSB]-11 must return all 0. Bit 0 (Expansion ROM Enable) must return 0. If any do not this is recorded as a failure, but the test continues.
30. The following register field characteristic checks are performed:

 Vendor ID Register (Location 00h) –– WORD

(For Base 4.x or later testing)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
(For Base 3.x or earlier testing)	RO

 Device ID Register (Location 02h) –– WORD

(For Base 4.x or later testing)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
(For Base 3.x or earlier testing)	RO

 Revision ID Register (Location 08h) –– BYTE

(For Base 4.x or later testing)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
(For Base 3.x or earlier testing)	RO

 Class Code Register (Location 09h) –– 3 BYTES

a. Programming Interface	RO
b. Sub-Class Code	RO
c. Base Class Code	RO

 Header Type Register (Location 0Eh) –– BYTE

(For Base 4.x or later testing)	
a. Header Layout	RO
b. Multi-Function Device	RO
(For Base 3.x or earlier testing)	RO

 Capabilities Pointer Register (Location 34h) – BYTE RO

 Reserved Register (Location 35h) –– 3 BYTES

a. Reserved_23-0	RO-Zero

 Expansion ROM Base Address Register (Location 38h) –– DWORD

a. Expansion ROM Enable	RW or RO-Zero
b. Reserved_10-1	RO-Zero

31. The following default value checks are performed:

 Header Type Register Default Value (Location 0Eh) –– BYTE

 (For Base 4.x or later testing)

a. Header Layout 000 0001b

Expansion ROM Base Address Register Default Value (Location 38h) — DWORD

a. Expansion ROM Enable 0

32. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- The Header Layout field returns other than 000 0000b or 000 0001b (for Base 4.x or later testing only).
- The Vendor ID field returns 0000h, FFFFh, or 0001h.
- For a Root Port, Switch Port, or Bridge, the Class Code register is not 06 04xxh.
- If I/O Base bits 3-0 does not return the same value as I/O Limit bits 3-0.
- If I/O Base bits 3-0 returns a reserved value.
- If I/O Space Enable is RO-Zero, but any of the following occurs: BAR0 bit 0 is not 0; BAR1 bit 0 is not 0; I/O Base is not RO-Zero; I/O Limit is not RO-Zero; I/O Base Upper 16 Bits are not RO-Zero; I/O Limit Upper 16 Bits are not RO-Zero.
- If 16 bit I/O addressing is reported, but any of the following occurs: I/O Base bits 15-12 are not RW; I/O Base bits 11-4 are not RO-Zero; I/O Base bits 3-0 are not RO; I/O Limit bits 15-12 are not RW; I/O Limit bits 11-4 are not RO-Zero; I/O Limit bits 3-0 are not RO; I/O Base Upper 16 Bits is not RO-Zero; I/O Limit Upper 16 Bits is not RO-Zero.
- If 32 bit I/O addressing is reported, but any of the following occurs: I/O Base bits 15-12 are not RW; I/O Base bits 11-4 are not RO-Zero; I/O Base bits 3-0 are not RO; I/O Limit bits 15-12 are not RW; I/O Limit bits 11-4 are not RO-Zero; I/O Limit bits 3-0 are not RO; I/O Base Upper 16 Bits is not RW; I/O Limit Upper 16 Bits is not RW.
- If any of the following occurs: Memory Base bits 15-4 are not RW; Memory Base bits 3-0 are not RO-Zero; Memory Limit bits 15-4 are not RW; Memory Limit bits 3-0 are not RO-Zero
- If Prefetchable Memory Base bits 3-0 does not return the same value as Prefetchable Memory Limit bits 3-0.
- If Prefetchable Memory Base bits 3-0 returns a reserved value.
- If Prefetchable Memory addressing is not reported, but any of the following occurs: Memory Prefetchable Base is not RO-Zero; Memory Prefetchable Limit is not RO-Zero; Prefetchable Base Upper 32 Bits are not RO-Zero; Prefetchable Limit Upper 32 Bits are not RO-Zero.
- If 32 bit Prefetchable Memory addressing is reported, but any of the following occurs: Memory Prefetchable Base bits 15-4 are not RW; Memory Prefetchable Base bits 3-0 are not RO; Memory Prefetchable Limit bits 15-4 are not RW; Memory Prefetchable Limit bits 3-0 are not RO; Prefetchable Base Upper 32 Bits is not RO-Zero; Prefetchable Limit Upper 32 Bits is not RO-Zero.

- If 64 bit Prefetchable Memory addressing is reported, but any of the following occurs: Memory Prefetchable Base bits 15-4 are not RW; Memory Prefetchable Base bits 3-0 are not RO; Memory Prefetchable Limit bits 15-4 are not RW; Memory Prefetchable Limit bits 3-0 are not RO; Prefetchable Base Upper 32 Bits is not RW; Prefetchable Limit Upper 32 Bits is not RW.
- If implemented, Expansion ROM BAR claims more than 16 MB of space.
- If implemented, Expansion ROM BAR does not return contiguous 1's across all implemented address bits.
- If implemented, Expansion ROM BAR does not implement RW bits across all implemented address bits.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

The test *warns* if:

- The Base Class Code field is 00h (for Base 3.x or later testing only).

2.2.37. TD_1_27 Multi-Function

The test verifies that if the function under test is part of a multi-function device then all other implemented functions in the same device respond correctly as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *PCI Local Bus Specification, Revision 3.0 (Base 3.x or earlier only)*
- *ECN Alternate Routing-ID Interpretation (to Base 2.0 and Base 1.1)*
- *ECN Latency Tolerance Reporting (to Base 2.0)*
- *ECN Multicast (to Base 2.0)*
- *ECN Optimized Buffer Flush/Fill (to Base 2.0 and Base 2.1)*
- *Single Root I/O Virtualization and Sharing Specification (Base 3.x or earlier only)*
- *ECN Separate Refclk Independent SSC Architecture (SRIS) (to Base 3.0)*
- *ECN Readiness Notifications (RN) (to Base 3.0)*
- *ECN Emergency Power Reduction mechanism with PWRBRK signal (to Base 3.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Since this test checks the function under test as well as any other functions (both ARI and non-ARI), PFs, and VFs within the device under test, the test must ensure that all the necessary initialization of the hierarchy is done so that the device under test's ARI functions and VFs are visible at this point. This requires that the test re-execute the detection algorithm described in Section 1.4.1.
3. Read a byte from location 0Eh (Header Type register) in the Configuration Space. (For this test, the current function is the function under test. Function 0 is function number 0. Other non-ARI functions are the complete range of function number 1 to function number 7. Other ARI functions are in the complete range of function number 1 to function number 255.)
4. For a VF perform the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. Check that the current function number is non-zero, if the Bus Number is the same as the associated PF's.
 b. For a non-ARI device, check that the device does respond to configuration requests to Function Number = 000b with the same Bus Number and Device Number as the associated PF. (For the purposes of this test, responding means that reading back a WORD at location 00h (Vendor ID) returns any value other than FFFFh or 0001h (CRS Software Visibility notification).)
 c. For an ARI device, check that the device does respond to configuration requests to Device Number/Function Number = 00h with the same Bus Number as the associated PF. (For the purposes of this test, responding means that reading back a WORD at location 00h (Vendor ID) returns any value other than FFFFh or 0001h (CRS Software Visibility notification).)
 d. For Base 2.x or later testing, if the function under test reports the Capability Version field (PCI Express Capabilities register) is 2h or greater:
 i. Read a DWORD at offset 24h (Device Capabilities 2 register) from the VF under test and record the value as the expected value for the field checks for this register. Check the associated PF that it returns the same expected value in its Device Capabilities 2 register for all the following and if any are not as stated, this is recorded as a failure, but the test continues:
 a. LTR Mechanism Supported
 b. OBFF Supported
 e. For Base 3.1 or later testing, if the function under test reports the Capability Version field (PCI Express Capabilities register) is 2h or greater:
 i. Read a DWORD at offset 24h (Device Capabilities 2 register) from the VF under test and record the value as the expected value for the field checks for this register. Check the associated PF that it returns the same expected value in its Device Capabilities 2 register for all the following and if any are not as stated, this is recorded as a failure, but the test continues:
 a. Emergency Power Reduction Supported
 b. Emergency Power Reduction Initialization Required
 f. For Base 4.x or later testing, if the function under test reports the Capability Version field (PCI Express Capabilities register) is 2h or greater:
 i. Read a DWORD at offset 24h (Device Capabilities 2 register) from the VF under test and record the value as the expected value for the field checks for this register. Check

the associated PF that it returns the same expected value in its Device Capabilities 2 register for all the following and if any are not as stated, this is recorded as a failure, but the test continues:

a. 10-Bit Tag Completer Supported

g. For Base 4.x or later testing, if the function under test reports the Capability Version field (PCI Express Capabilities register) is 2h or greater:
 i. Read a DWORD at offset 24h (Device Capabilities 2 register) and record the value of bit 17 (10-Bit Tag Requester Supported) as the expected value. Check the associated PF that it returns the same expected value for bit 2 (VF 10-Bit Tag Requester Supported) in its SR-IOV Capabilities register and if not, this is recorded as a failure, but the test continues.

h. For Base 3.1 or later testing, if the optional Device Serial Number Extended Capability structure is found in the current function, check that it returns the same value for the PCI Express Device Serial Number field (64 bits) as function 0 does. (For an ARI device, function 0 is located at Device Number = 0 0000b and Function Number = 000b. For a non-ARI device, function 0 is located at Function Number = 000b using the PF's Device Number.)

i. If the optional ARI Extended Capability structure is found in the current function, check that all other functions (including all other PFs and all other VFs) implement the ARI Extended Capability structure. (For an ARI device, there can be up to 256 functions.)

j. If the optional TPH Extended Capability structure is found in the current function:
 i. Check that all VFs associated with the same PF as the current function, also implement the TPH Extended Capability structure, and that they all report the same values for the following fields:
 a. The No ST Mode Supported field should be checked for identical values.
 b. The Interrupt Vector Mode Supported field should be checked for identical values.
 c. The Device Specific Mode Supported field should be checked for identical values.
 d. The Extended TPH Requester Supported field should be checked for identical values.
 e. The ST Table Location field should be checked for identical values.
 f. The ST Table Size field should be checked for identical values.

k. For Base 3.x or later testing, if the optional Readiness Time Reporting Extended Capability structure is found in the current function, and the Valid field (Readiness Time Reporting 1 register) returns 1:
 i. Check that all VFs associated with the same PF as the current function, also implement the Readiness Time Reporting Extended Capability structure, and that they all report the same values for the following fields:
 a. The Valid field should be checked for identical values.
 b. If the Immediate Readiness field returns 0, then the Reset Time field should be checked for identical values.
 c. The FLR Time field should be checked for identical values.
 d. If the Immediate Readiness on Return to D0 field returns 0, then the D3hot to D0 Time field should be checked for identical values.

5. For a non-VF, if the Multi-Function Device bit (Header Type register) returns 0 and it does not implement an ARI Extended Capability structure, perform the following checks and if any are not as stated, this is recorded as a failure, but the test continues:

a. Check that the current function number is zero. (For a non-ARI device, function 0 is located at Function Number = 000b using the current Device Number.)
b. Check that the device does not respond to configuration requests to all other Function Numbers with the same Bus Number and Device Number. (For the purposes of this test, not responding means that reading back a WORD at location 00h (Vendor ID) returns FFFFh or 0001h (CRS Software Visibility notification).) (Note: VFs will return Vendor ID of FFFFh, so they will not be considered as another function by this test.) If the device responds to configuration requests to any other Function Number with the same Bus Number and Device Number, then a warning message is issued, but this is not treated in itself as a failure.
c. Check that the function does not implement a Virtual Channel Extended Capability structure with Extended Capability ID of 0009h.
d. Check that the function does not implement a Multi-Function Virtual Channel Extended Capability structure (Extended Capability ID of 0008h).

6. For a non-VF, if the Multi-Function Device bit (Header Type register) returns 0 and it does implement an ARI Extended Capability structure, perform the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. Check that the current function number is zero. (For an ARI device, function 0 is located at Device Number = 0 0000b and Function Number = 000b.)
 b. For an ARI device, read a WORD at offset 04h in the ARI Extended Capability structure.
 i. If the Next Function Number (ARI Capability register) is zero, check that the function does not implement a Virtual Channel Extended Capability structure with Extended Capability ID of 0009h.
 ii. If the Next Function Number (ARI Capability register) is zero, check that the function does not implement a Multi-Function Virtual Channel Extended Capability structure (Extended Capability ID of 0008h).
7. For Base 2.x or later testing: if the current function's Multi-Function bit returns 1 and the current function's Device/Port Type is one of: 0000b (Endpoint), 0001b (Legacy Endpoint), 1001b (Root Complex Integrated Endpoint), 0101b (Switch Upstream Port), or 0111b (PCI Express to PCI/PCI-X Bridge), perform the following checks.
 a. For a non-VF, if the function implements a PCI Power Management Capability structure, the No_Soft_Reset field (Power Management Control/Status register) should return 1. If it does not, a warning message is issued, but this is not treated in itself as a failure.
 b. If the function under test's Device/Port Type is one of: 0000b (Endpoint), 0001b (Legacy Endpoint), or 1001b (Root Complex Integrated Endpoint):
 i. Read a DWORD at offset 04h (Device Capabilities register) from the function under test and record the value as the expected value for the field checks for this register. Check all implemented functions in that device, that they return the same expected value in their Device Capabilities register for all the following fields and if any are not as stated, a warning message is issued, but this is not treated in itself as a failure:
 a. Function Level Reset Capability should return 1
 c. For Base 3.1 or later testing: if the function under test reports the Capability Version field (PCI Express Capabilities register) is 2h or greater and the Emergency Power Reduction Supported field (Device Capabilities 2 register) is non-zero:
 i. Read a WORD at offset 0Ah (Device Status register) and record the value as the expected value for the field checks for this register. Check all implemented functions in that device which also have Emergency Power Reduction Supported field non-zero, that

they return the same expected value in their Device Status register for all the following fields and if any are not as stated, this is recorded as a failure, but the test continues:
 a. Emergency Power Reduction Detected

d. If the function under test reports the Capability Version field (PCI Express Capabilities register) is 2h or greater:
 i. Read a DWORD at offset 24h (Device Capabilities 2 register) and record the value as the expected value for the field checks for this register. Check all implemented functions in that device that they return the same expected value in their Device Capabilities 2 register for all the following fields and if any are not as stated, this is recorded as a failure, but the test continues:
 a. Extended FMT Field Supported
 ii. For Base 3.1 or later testing: read a DWORD at offset 24h (Device Capabilities 2 register) and record the value as the expected value for the field checks for this register. Check all implemented functions in that device that they return either the same expected value or else zero in their Device Capabilities 2 register for all the following fields and if any are not as stated, this is recorded as a failure, but the test continues:
 a. Emergency Power Reduction Supported
 iii. For Base 3.1 or later testing: read a DWORD at offset 24h (Device Capabilities 2 register) and record the value as the expected value for the field checks for this register. Check all implemented functions in that device that they return the same expected value in their Device Capabilities 2 register for all the following fields and if any are not as stated, this is recorded as a failure, but the test continues:
 a. Emergency Power Reduction Initialization Required

8. For Base 2.x or later testing: if the current function's Multi-Function bit returns 1 and the current function's Device/Port Type is one of: 0000b (Endpoint), 0001b (Legacy Endpoint), 0101b (Switch Upstream Port), or 0111b (PCI Express to PCI/PCI-X Bridge).
 a. Read a DWORD at offset 0Ch (Link Capabilities register) and record the value as the expected value for the field checks for this register. Check all implemented functions in that device that they return the same expected value in their Link Capabilities register for all the following fields and if any are not as stated, this is recorded as a failure, but the test continues:
 i. Max Link Speed/Supported Link Speeds
 ii. Maximum Link Width
 iii. Active State Power Management (ASPM) Support
 iv. L0s Exit Latency
 v. L1 Exit Latency
 vi. Port Number
 vii. If the function contains an ARI Extended Capability: Clock Power Management
 b. For Base 3.x or later testing, if the function under test reports the Capability Version field (PCI Express Capabilities register) is 2h or greater:
 i. Read a DWORD at offset 2Ch (Link Capabilities 2 register) and record the value as the expected value for the field checks for this register. Check all implemented functions in that device that they return the same expected value in their Link Capabilities 2 register for all the following fields and if any are not as stated, this is recorded as a failure, but the test continues:
 a. Supported Link Speeds Vector
 b. Crosslink Supported

c. Lower SKP OS Generation Supported Speeds Vector
d. Lower SKP OS Reception Supported Speeds Vector

9. If the current function's Multi-Function bit returns 1 and the current function's Device/Port Type is one of: 0000b (Endpoint), 0001b (Legacy Endpoint), 0101b (Switch Upstream Port), or 0111b (PCI Express to PCI/PCI-X Bridge), perform the following checks and if any are not as stated, this is recorded as a failure, but the test continues.
 a. Read a WORD at offset 12h (Link Status register) and record the value as the expected value for the field checks for this register. Check all implemented functions in that device that they return the same expected value in their Link Status register for all the following fields and if any are not as stated, this is recorded as a failure, but the test continues:
 i. Slot Clock Configuration
10. For Base 3.x or later: if the current function's Multi-Function bit returns 1 and the current function's Device/Port Type is one of: 0000b (Endpoint), 0001b (Legacy Endpoint), 0101b (Switch Upstream Port), or 0111b (PCI Express to PCI/PCI-X Bridge), perform the following checks and if any are not as stated, this is recorded as a failure, but the test continues.
 a. If the function under test reports the Capability Version field (PCI Express Capabilities register) is 2h or greater:
 i. Read a WORD at offset 32h (Link Status 2 register) and record the value as the expected value for the field checks for this register. Check all implemented functions in that device that they return the same expected value in their Link Status 2 register for all the following fields and if any are not as stated, this is recorded as a failure, but the test continues:
 a. Current De-emphasis Level
 b. If the optional PTM Extended Capability structure is found in the current function, check that all other functions (including all VFs) do not implement the PTM Extended Capability structure. (For an ARI device, there can be up to 256 functions.)
11. For a non-VF, if the Multi-Function bit returns 1 and the current function number is non-zero, perform the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. For a non-ARI device, check that the device does respond to configuration requests to Function Number = 000b with the same Bus Number and Device Number. (For the purposes of this test, responding means that reading back a WORD at location 00h (Vendor ID) returns any value other than FFFFh or 0001h (CRS Software Visibility notification).)
 b. For an ARI device, check that the device does respond to configuration requests to the Device Number/Function Number = 00h with the same Bus Number. (For the purposes of this test, responding means that reading back a WORD at location 00h (Vendor ID) returns any value other than FFFFh or 0001h (CRS Software Visibility notification).)
 c. For an ARI device, read a WORD at offset 04h in the ARI Extended Capability structure and if the Next Function Number (ARI Capability register) is non-zero, check that the device does respond to configuration requests to the Device Number/Function Number given by the value returned in Next Function Number (ARI Capability register) with the same Bus Number. (For the purposes of this test, responding means that reading back a WORD at location 00h (Vendor ID) returns any value other than FFFFh or 0001h (CRS Software Visibility notification).)
 d. For a non-ARI device, check that the function at Function Number = 000b with the same Bus Number and Device Number also has the Multi-Function bit return 1.

e. For an ARI device, check that the function at Device Number/Function Number = 00h with the same Bus Number also has the Multi-Function bit return 1.
f. For Base 2.x or later testing, if the current function's Device/Port Type is one of: 0000b (Endpoint), 0001b (Legacy Endpoint), 0101b (Switch Upstream Port), or 0111b (PCI Express to PCI/PCI-X Bridge), and if the function under test reports the Capability Version field (PCI Express Capabilities register) is 2h or greater:
 i. Read a DWORD at offset 24h (Device Capabilities 2 register) from the function under test and record the value as the expected value for the field checks for this register. Check function 0 that it returns the same expected value in its Device Capabilities 2 register for all the following and if any are not as stated, this is recorded as a failure, but the test continues:
 a. LTR Mechanism Supported
 b. OBFF Supported
g. If the current function's Device/Port Type is one of: 0000b (Endpoint), 0001b (Legacy Endpoint), 0101b (Switch Upstream Port), or 0111b (PCI Express to PCI/PCI-X Bridge):
 i. Check that the current function does not implement a Virtual Channel Extended Capability with Extended Capability ID of 0002h. If it does implement one, this is recorded as a failure, but the test continues.
h. Check that the current function does not implement a Multi-Function Virtual Channel Extended Capability structure (Extended Capability ID of 0008h). If it does implement one, this is recorded as a failure, but the test continues.
i. If the optional Virtual Channel Extended Capability structure with Extended Capability ID of 0009h is found in the current function, check that function 0 implements a Multi-Function Virtual Channel Extended Capability structure (Extended Capability ID of 0008h). (For an ARI device, function 0 is located at Device Number = 0 0000b and Function Number = 000b. For a non-ARI device, function 0 is located at Function Number = 000b using the current Device Number.)
j. If the current function's Device/Port Type is one of: 0000b (Endpoint), 0001b (Legacy Endpoint), 0101b (Switch Upstream Port), or 0111b (PCI Express to PCI/PCI-X Bridge), and if the optional Multicast Extended Capability structure is found in the current function, check that all other functions (including function 0 but excluding VFs) implement the Multicast Extended Capability structure. (For an ARI device, there can be up to 256 functions.)
k. For Base 4.x or later testing, if the current function's Device/Port Type is one of: 0000b (Endpoint), 0001b (Legacy Endpoint), 0101b (Switch Upstream Port), or 0111b (PCI Express to PCI/PCI-X Bridge), and if the optional Data Link Feature Extended Capability structure is found in the current function:
 i. Read the Data Link Feature Capabilities register and the Data Link Feature Status register from the function under test and record these values as the expected values for the checks for these registers.
 ii. Check that all other functions (including function 0 but excluding VFs) implement the Data Link Feature Extended Capability structure. If any do not implement one, this is recorded as a failure, but the test continues.
 iii. For every other function that implements the Data Link Feature Extended Capability structure, check that they return the same expected value in their registers for all the following and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The Data Link Feature Capabilities register reports the same expected value as from the function under test.

b. The Data Link Feature Status register reports the same expected value as from the function under test.

l. If the optional ARI Extended Capability structure is found in the current function, check that all other functions (including function 0 and all VFs) implement the ARI Extended Capability structure. (For an ARI device, there can be up to 256 functions.)

12. For a non-VF, if the Multi-Function bit returns 1 and the current function number is zero (for an ARI device, function 0 is located at Device Number = 0 0000b and Function Number = 000b; for a non-ARI device, function 0 is located at Function Number = 000b using the current Device Number), perform the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. Check that the device does respond to configuration requests to at least one of Function Number 1 to 7 with the same Bus Number and Device Number. (For the purposes of this test, responding means that reading back a WORD at location 00h (Vendor ID) returns any value other than FFFFh or 0001h (CRS Software Visibility notification).) (Note: VFs will return Vendor ID = FFFFh, so they will not be considered as another function by this test.)
 b. For an ARI device, read a WORD at offset 04h in the ARI Extended Capability structure and check that the Next Function Number (ARI Capability register) is non-zero.
 c. For an ARI device, check that the device does respond to configuration requests to the Device Number/Function Number given by the value returned in Next Function Number (ARI Capability register) with the same Bus Number. (For the purposes of this test, responding means that reading back a WORD at location 00h (Vendor ID) returns any value other than FFFFh or 0001h (CRS Software Visibility notification).) (Note: VFs will return Vendor ID = FFFFh, so they will not be considered as another function by this test.)
 d. Check all implemented functions (excluding VFs) in that device that they must have the Multi-Function bit return 1.
 e. For Base 2.x or later testing, if the current function's Device/Port Type is one of: 0000b (Endpoint), 0001b (Legacy Endpoint), 0101b (Switch Upstream Port), or 0111b (PCI Express to PCI/PCI-X Bridge), and if the function under test reports the Capability Version field (PCI Express Capabilities register) is 2h or greater:
 i. Read a DWORD at offset 24h (Device Capabilities 2 register) from the function under test and record the value for the field checks for this register. Check all implemented functions that they return the same expected value in their Device Capabilities 2 register for all the following and if any are not as stated, this is recorded as a failure, but the test continues:.
 a. LTR Mechanism Supported
 b. OBFF Supported
 f. If the optional Virtual Channel Extended Capability structure with Extended Capability ID of 0002h is found in function 0, check that function 0 does not implement either a Virtual Channel Extended Capability structure with Extended Capability ID of 0009h or a Multi-Function Virtual Channel Extended Capability structure (Extended Capability ID of 0008h) and that no other function implements a Virtual Channel Extended Capability structure with Extended Capability ID of 0009h. (For an ARI device, function 0 is located at Device Number = 0 0000b and Function Number = 000b. For a non-ARI device, function 0 is located at Function Number = 000b using the current Device Number.)
 g. Check all implemented functions in that device for the Device Serial Number Extended Capability structure and if the optional Device Serial Number Extended Capability structure is found, check that either only function 0 implements this Device Serial Number Extended Capability structure or that all other functions (excluding VFs) that implement the Device

Serial Number Extended Capability structure, return the same expected value for the PCI Express Device Serial Number field (64 bits) as function 0 does. (For an ARI device, function 0 is located at Device Number = 0 0000b and Function Number = 000b. For a non-ARI device, function 0 is located at Function Number = 000b using the current Device Number. For an ARI device, there can be up to 256 functions.)

h. If the current function's Device/Port Type is one of: 0000b (Endpoint), 0001b (Legacy Endpoint), 0101b (Switch Upstream Port), or 0111b (PCI Express to PCI/PCI-X Bridge), and if the optional Multicast Extended Capability structure is found in the current function, check that all other functions (excluding VFs) implement the Multicast Extended Capability structure. (For an ARI device, there can be up to 256 functions.)

i. For Base 4.x or later testing, if the current function's Device/Port Type is one of: 0000b (Endpoint), 0001b (Legacy Endpoint), 0101b (Switch Upstream Port), or 0111b (PCI Express to PCI/PCI-X Bridge), and if the optional Data Link Feature Extended Capability structure is found in the current function:
 i. Read the Data Link Feature Capabilities register and the Data Link Feature Status register from the function under test and record these values as the expected values for the checks for these registers.
 ii. Check that all other functions (including function 0 but excluding VFs) implement the Data Link Feature Extended Capability structure. If any do not implement one, this is recorded as a failure, but the test continues.
 iii. For every other function that implements the Data Link Feature Extended Capability structure, check that they return the same expected value in their registers for all the following and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The Data Link Feature Capabilities register reports the same expected value as from the function under test.
 b. The Data Link Feature Status register reports the same expected value as from the function under test.

j. If the optional ARI Extended Capability structure is found in the current function, check that all other functions (including all VFs) implement the ARI Extended Capability structure. (For an ARI device, there can be up to 256 functions.)

13. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- ❑ For a VF at the same Bus Number as its associated PF, the function number is zero.
- ❑ For a VF at the same Bus Number as its associated PF, there is no function at function number is zero.
- ❑ For all VFs and their associated PF, the LTR Mechanism Supported field is not the same (for Base 2.x or later testing only).
- ❑ For all VFs and their associated PF, the OBFF Supported field is not the same (for Base 2.x or later testing only).

- For all VFs and their associated PF, the Emergency Power Reduction Supported field is not the same (for Base 3.1 or later testing only).
- For all VFs and their associated PF, the Emergency Power Reduction Initialization Required field is not the same (for Base 3.1 or later testing only).
- For all VFs and their associated PF, the 10-Bit Tag Completer Supported field is not the same (for Base 4.x or later testing only).
- For all VFs, the 10-Bit Tag Requester Supported field is not the same as their associated PF's VF 10-Bit Tag Requester Supported field (for Base 4.x or later testing only).
- For a VF, a Device Serial Number Extended Capability structure is present, and this Extended Capability structure returns a different Device Serial Number field value then function 0 does (for Base 3.1 or later testing only).
- For a VF that implements an ARI Extended Capability structure, that device does not implement it in all functions (including all PFs and VFs).
- For a VF that implements a TPH Extended Capability structure, all other VFs associated with the same PF, do not implement the TPH Extended Capability structure.
- For all VFs associated with the same PF, that implements a TPH Extended Capability structure, all other VFs do not report the same value for each of the individual TPH Requester Capability register fields: No ST Mode Supported; Interrupt Vector Mode Supported; Device Specific Mode Supported; Extended TPH Requester Supported; ST Table Location; ST Table Size.
- For a VF that implements a Readiness Time Reporting Extended Capability structure, all other VFs associated with the same PF, do not implement the Readiness Time Reporting Extended Capability structure (for Base 3.x or later testing only).
- For all VFs associated with the same PF, that implements a Readiness Time Reporting Extended Capability structure with the Valid field reporting 1, all other VFs do not report the same value for each of the individual Readiness Time Reporting 1 and Readiness Time Reporting 2 register fields (for Base 3.x or later testing only): Valid field; Reset Time field (only if Immediate Readiness is 0); FLR Time; D3hot to D0 Time field (only if Immediate Readiness on Return to D0 is 0).
- For a non-VF, the Multi-Function bit is 0 and the function number is non-zero.
- For a non-VF, the Multi-Function bit is 1 and the device has not implemented function 0 as a function that has the Multi-Function bit set to 1.
- For a non-VF in a non-ARI device, the Multi-Function bit is 1 and there is not at least one other PCI Express function implemented.
- For a non-VF in an ARI device, in function 0 the Multi-Function bit is 1 and function 0 reports a Next Function Number field value of zero.
- For a non-VF in an ARI device, a function other than 0 reports a non-zero Next Function Number field value, but at that address there is no implemented function.
- For a multi-function device associated with an upstream port, the Emergency Power Reduction Detected field is not the same in all implemented functions that have the Emergency Power Reduction Supported field also non-zero (for Base 3.1 or later testing only).

- For a multi-function device associated with an upstream port, the Extended FMT Field Supported field is not the same in all implemented functions (for Base 2.x or later testing only).
- For a multi-function device associated with an upstream port, the LTR Mechanism Supported field is not the same in all implemented functions (for Base 2.x or later testing only).
- For a multi-function device associated with an upstream port, the OBFF Supported field is not the same in all implemented functions (for Base 2.x or later testing only).
- For a multi-function device associated with an upstream port, the Emergency Power Reduction Supported field is non-zero and not the same in all implemented functions that have the field also non-zero (for Base 3.1 or later testing only).
- For a multi-function device associated with an upstream port, the Emergency Power Reduction Initialization Required field is not the same in all implemented functions (for Base 3.1 or later testing only).
- For a multi-function device associated with an upstream port, all implemented functions do not report the same value for each of the individual Link Capabilities register fields: Max Link Speed/Supported Link Speeds; Maximum Link Width; Active State Power Management (ASPM) Support; L0s Exit Latency; L1 Exit Latency; Port Number.
- For a multi-function ARI device associated with an upstream port, all implemented functions do not report the same value for each of the individual Link Capabilities register fields: Clock Power Management.
- For a multi-function device associated with an upstream port, all implemented functions do not report the same value for each of the individual Link Capabilities 2 register fields: Supported Link Speeds Vector; Crosslink Supported; Lower SKP OS Generation Supported Speeds Vector; Lower SKP OS Reception Supported Speeds Vector.
- For a multi-function device associated with an upstream port, all implemented functions do not report the same value for each of the individual Link Status register fields: Slot Clock Configuration.
- For a multi-function device associated with an upstream port, all implemented functions do not report the same value for each of the individual Link Status 2 register fields: Current De-emphasis Level (for Base 3.x or later testing only).
- For a multi-function device associated with an upstream port, more than one implemented function implements a PTM Extended Capability structure (for Base 3.x or later testing only).
- For a non-VF, a single-function device implements either a Virtual Channel Extended Capability structure with Extended Capability ID of 0009h or a Multi-Function Virtual Channel Extended Capability structure (Extended Capability ID of 0008h).
- For a non-VF, a multi-function device associated with an Upstream Port implements a Virtual Channel Extended Capability structure with Extended Capability ID of 0002h in a function other than function 0.
- For a non-VF, a multi-function device implements a Multi-Function Virtual Channel Extended Capability structure (Extended Capability ID of 0008h) in a function other than function 0.
- For a non-VF, a multi-function device implements a Virtual Channel Extended Capability structure with Extended Capability ID of 0009h in any function other than function 0, but does

not implement a Multi-Function Virtual Channel Extended Capability structure (Extended Capability ID of 0008h) in function 0.

- For a non-VF, a multi-function device implements a Virtual Channel Extended Capability structure with Extended Capability ID of 0009h in any function (including function 0), when it also implements a Virtual Channel Extended Capability structure with Extended Capability ID of 0002h in function 0.
- For a non-VF, a multi-function device implements both a Multi-Function Virtual Channel Extended Capability structure (Extended Capability ID of 0008h) and a Virtual Channel Extended Capability structure with Extended Capability ID of 0002h in function 0.
- For a non-VF, a Device Serial Number Extended Capability structure is present, this Extended Capability structure is not in function 0, or any additional functions with this Extended Capability structure return a different Device Serial Number field value then function 0 does.
- For a non-VF, a multi-function device associated with an Upstream Port that implements a Multicast Extended Capability structure in any function, does not implement it in all functions.
- For a non-VF, a multi-function device associated with an Upstream Port that implements a Data Link Feature Extended Capability structure in any function, does not implement it in all functions (for Base 4.x or later testing only).
- For a non-VF, a multi-function device associated with an Upstream Port that implements a Data Link Feature Extended Capability structure in any function, does not report the same Data Link Feature Capabilities and Data Link Feature Status register values in all functions that implement that capability (for Base 4.x or later testing only).
- For a non-VF, a multi-function device that implements an ARI Extended Capability structure in any function, does not implement it in all functions.

The test *warns* if:

- For a non-VF in a non-ARI device, the Multi-Function bit is 0 and the device responds to configuration requests to another function.
- For a non-VF, which is an Endpoint, Legacy Endpoint, Switch Upstream Port, or PCI Express to PCI/PCI-X Bridge, the Multi-Function bit is 1, and the Function Level Reset Capability field is not set.
- For a non-VF, which is an Endpoint, Legacy Endpoint, Switch Upstream Port, or PCI Express to PCI/PCI-X Bridge, the Multi-Function bit is 1, that implements a PCI Power Management Capability structure, and the No_Soft_Reset field is not set.

2.2.38. TD_1_28 Vital Product Data Capability Structure

The test verifies that if the function under test reports a VPD Capability structure, it is implemented as defined in the relevant specifications. (Only Read operations of the VPD area are performed. Write operations are not performed as they would cause VPD data to be over-written.)

Relevant Specifications

- *PCI Express Base Specification*
- *PCI Local Bus Specification, Revision 3.0 (Base 3.x or earlier only)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Capability ID field for each of the function's Capability structures. Determine how many instances of the Capability ID of 03h (Vital Product Data Capability) are found.
3. If the Capability ID of 03h is found in a Capability structure, the following steps are performed for each instance of that Capability structure. If the Capability ID of 03h is not found in a Capability structure, the test skips to step 10.
4. The Next Capability Pointer field must be 00h or greater than 3Fh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
5. The following register field characteristic checks are performed:

 Vital Product Data Capability Header (Offset 00h) — WORD

 a. Capability ID — RO
 b. Next Capability Pointer — RO

 VPD Address Register (Offset 02h) — WORD

 a. VPD Address — RW

 VPD Data Register (Offset 04h) — DWORD

 a. VPD Data — RW

6. For this test, bits 15-0 of the WORD at offset 02h in the capability are written at the same time. Bits 14-0 are the DWORD aligned address in the VPD storage component of the VPD data (the bottom two bits must be zero). Bit 15 is a flag that tells the system to either read from or write to the supplied address. Bit 15 also tells when the requested operation has completed.
7. Test software writes 0000h to the WORD at offset 02h and then test software monitors bit 15 until it is set by hardware to indicate that the VPD Data register contains valid data. If bit 15 does not return a value of one within 1 second, the test fails and is terminated. When bit 15 returns one, the DWORD at offset 04h is read. It must contain four bytes of data from the VPD storage component. The following checks are performed on the 4 bytes of returned data:
 a. Byte 0 must return 82h (Identifier String tag matching criteria set out for VPD). If not, the test fails and is terminated, otherwise it continues.
 b. Bytes 2-1 must contain the length of the data items (length value is in bytes designated as [length]). The [length] must not exceed 7FFFh minus 3. If the [length] does exceed this value, the test fails and is terminated, otherwise it continues.
 c. Bytes 3 to [length] must contain the data.
 d. Test software continues to read data four bytes at a time until Byte [length] has been read.

e. Test software checks that each byte returned from byte 3 to [length] (Product Name for this first data item) is a valid ASCII code (0x00-0x7F). If not, the test fails and is terminated, otherwise it continues.

8. Test software reads the next byte to determine the next Data Type.

(For these steps, test software checks each byte. It does this by writing the byte address divided by four and rounded down, then shifted left by 2 make it a DWORD aligned address, to the WORD at offset 02h, and then test software monitors bit 15 until it is set by hardware to indicate that the VPD Data register contains valid data. If bit 15 does not return a value of one within 1 second, the test fails and is terminated. When bit 15 returns one, the DWORD at offset 04h is read. It contains four bytes of data from the VPD storage component. These four bytes are used as the four bytes to be checked. Once these four bytes have been checked, the process is repeated to read the next four bytes.)

a. If the returned value is 78h (End Tag), then the test passes and terminates, otherwise it continues.
b. Test software initializes the Checksum [CHK] to 00h. ([CHK] is a byte value used to calculate the checksum of the VDR-R Tag structure, by adding each byte read. Any carries out of [CHK] are dropped.) Initialize the "RV" Byte Address [RVBA] to 00h. ([RVBA] is used to determine if the checksum keyword has been detected, and to locate the actual checksum byte.)
c. The returned value must be 90h (VPD-R) or 91h (VPD-W). If not, the test fails and is terminated, otherwise record the current Tag type (VPD-R or VDP-W) and continue.
d. If the current TAG type is VPD-R, then update [CHK] by adding the returned value to it (the byte read in step 8).
e. The next two bytes are read and combined into a WORD (first byte read is lower byte of WORD) that indicate the byte length of this data item ([length]). The [length] must not exceed 7FFFh minus the current byte offset. If the [length] does exceed this value, the test fails and is terminated, otherwise it continues.
f. If the current TAG type is VPD-R, then update [CHK] by adding each of the two bytes to it (the two bytes read in step e).
g. Test software reads the next byte and checks that it (1st letter of field name) is a valid ASCII code (0x00-0x7F). If not, the test fails and is terminated, otherwise it continues.
h. If the current TAG type is VPD-R, then update [CHK] by adding the returned value to it (the byte read in step g).
i. Test software reads the next byte and checks that it (2nd letter of field name) is a valid ASCII code (0x00-0x7F). If not, the test fails and is terminated, otherwise it continues.
j. If the current TAG type is VPD-R, then update [CHK] by adding the returned value to it (the byte read in step i).
k. The WORD (1st letter of field name, 2nd letter of field name) is checked that it is one of the following sets:
 i. If this current Tag type is VPR-R then ASCII (PN, EC, FG, LC, MN, PG, SN, Vx, CP, RV) – where x is any ASCII character between 0 and Z. If RV (checksum) is detected, then this is recorded.
 ii. If this current Tag type is VPR-W, then ASCII (Vx, Yx, RW) – where x is any ASCII character between 0 and Z. If RW (remaining WORDs) is detected, then this is recorded.

iii. Test software reads the next byte and this value indicates the length of the field [field length].
iv. If the current TAG type is VPD-R, then update [CHK] by adding the returned value to it (the byte read in step iii).
v. Test software continues to read and check data until either [field length] is reached or [length] is reached. If [length] is reached before [field length] is reached, the test fails and is terminated. If [field length] is reached before [length] is reached, the current field name that was recorded is cleared and the test repeats steps 8g-8k to record the new current field name. If the current field name is not "RV" or "RW", then the read data is checked that it is a valid ASCII code (0x00-0x7F) and if not a valid ASCII code, the test fails and is terminated. If the current TAG type is VPD-R, then update [CHK] by adding the returned value to it (each byte read in this step). If the current TAG type is VPD-R, and the byte read is the first byte of "RV", then this byte address is recorded in [RVBA]. If the current TAG type is VPD-R and the value in [RVBA] is non-zero, and if the byte address of the byte just read is equal to [RVBA] + 3, then the byte just read is the checksum byte, so verify that the value in [CHK] is 00h and if not, the test fails and is terminated.

l. If the current Tag type is VPD-R and both [length] and [field length] are reached, without detecting a field type of "RV" (the value in [RVBA] is still 0), the test fails and is terminated.

9. If the current byte address is greater than 7FFFh (maximum VPD Address size), the test fails and is terminated, otherwise test software repeats step 8 until an End Tag is found.

10. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- ❑ Configuration Space cannot be read.
- ❑ A non-zero Next Capability Pointer is less than or equal to 3Fh, or the lower 2 bits are non-zero.
- ❑ The Flag field does not return 1 upon an attempt to read VPD data.
- ❑ The Tag field cannot be read or is not correct.
- ❑ The VPD area does not begin with a valid Product Name.
- ❑ The VPD area contains a VPD-R Tag type, but it does not contain a RV (checksum) field.
- ❑ The VPD area contains a VPD-R Tag type, but the calculated checksum is not 00h.
- ❑ The VPD area contains a VPD-R Tag type, with reserved or invalid field names.
- ❑ The VPD area contains a VPD-W Tag type, with reserved or invalid field names.
- ❑ The VPD area contains field lengths that exceed the size of the Tag length.
- ❑ The End Tag does not exist.
- ❑ Any of the register field characteristic tests fail.

2.2.39. TD_1_32 PCI-X Capability Structure

The test verifies that if the function under test reports a PCI-X Capability structure, it is implemented as defined in the relevant specifications. (Only a Bridge with a PCI-X bus can implement this Capability structure.)

Relevant Specifications

- *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0*
- *PCI-X Addendum to the PCI Local Bus Specification, Revision 2.0a*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Capability ID field for each of the function's Capability structures. Determine how many instances of the Capability ID of 07h (PCI-X Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Capability ID of 07h is found in a Capability structure for a device type that is neither a PCI Express to PCI/PCI-X Bridge nor a PCI/PCI-X to PCI Express Bridge (a device with a PCI-X bus), the test terminates with failure.
4. If the Capability ID of 07h is found in a Capability structure, the following steps are performed on that Capability structure. If the Capability ID of 07h is not found in a Capability structure, the test skips to step 10.
5. The Next Capability Pointer field must be 00h or greater than 3Fh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
6. Test software reads the WORD from offset 02h (PCI-X Secondary Status register) and performs the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The PCI-X Capabilities List Item Version field has a valid encoding (00b, 01b, or 10b).
7. Test software reads the DWORD from offset 10h (PCI-X Bridge ECC Control and Status register) and performs the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The ECC Error Phase field has a valid encoding (000b to 101b).
8. The following register field characteristic checks are performed:

 PCI-X Capability Header (Offset 00h) — WORD

 a. Capability ID RO

b. Next Capability Pointer	RO

PCI-X Secondary Status Register (Offset 02h) — WORD

a. 64-Bit Device	RO
b. 133 MHz Capable	RO
c. Split Completion Discarded	RW1C
d. Unexpected Split Completion	RW1C
e. Split Completion Overrun	RW1C
f. Split Request Delayed	RW1C
g. Secondary Bus Mode and Frequency	RO
h. Reserved_11-10	RO-Zero
i. PCI-X Capabilities List Item Version	RO
j. PCI-X 266 Capable	RO
k. PCI-X 533 Capable	RO

PCI-X Bridge Status Register (Offset 04h) — DWORD

a. Function Number	RO
b. Device Number	RO
c. Bus Number	RO
d. 64-bit Device	
(for PCI Express to PCI/PCI-X Bridge)	RO-Zero
(for PCI/PCI-X to PCI Express Bridge)	RO
e. 133 MHz Capable	
(for PCI Express to PCI/PCI-X Bridge)	RO-Zero
(for PCI/PCI-X to PCI Express Bridge)	RO
f. Split Completion Discarded	
(for PCI Express to PCI/PCI-X Bridge)	RO-Zero
(for PCI/PCI-X to PCI Express Bridge)	RW1C
g. Unexpected Split Completion	RW1C
h. Split Completion Overrun	RW1C
i. Split Request Delayed	RW1C
j. Reserved_28-22	RO-Zero
k. Device ID Messaging Capable	RO
l. PCI-X 266 Capable	
(for PCI Express to PCI/PCI-X Bridge)	RO- Zero
(for PCI/PCI-X to PCI Express Bridge)	RO
m. PCI-X 533 Capable	
(for PCI Express to PCI/PCI-X Bridge)	RO-Zero
(for PCI/PCI-X to PCI Express Bridge)	RO

Upstream Split Transaction Control Register (Offset 08h) — DWORD

a. Split Transaction Capacity	RO
b. Split Transaction Commitment Limit	RW

Downstream Split Transaction Control Register (Offset 0Ch) — DWORD

a. Split Transaction Capacity	RO
b. Split Transaction Commitment Limit	RW

PCI-X Bridge ECC Control and Status Register (Offset 10h) — DWORD

a. Select Secondary ECC registers	RO

b. Error Present in Other ECC Register Bank — RO-Zero
c. Additional Correctable ECC Error — RW1C
d. Additional Uncorrectable ECC Error — RW1C
e. ECC Error Phase — RW1C
f. ECC Error Corrected — RO
g. Syndrome — RO
h. Error First (or only) Command — RO
i. Error Second Command — RO
j. Error Upper Attributes — RO
k. ECC Control Update Enable — RO-Zero
l. Reserved_29 — RO-Zero
m. Disable Single-Bit-Error Correction — RW or RO
n. ECC Mode — RW or RO

PCI-X Bridge ECC First Address (Offset 14h) — DWORD

a. First 32 bits of Address — RO

PCI-X Bridge ECC Second Address (Offset 18h) — DWORD

a. Second 32 bits of Address — RO

PCI-X Bridge ECC Attribute (Offset 1Ch) — DWORD

a. ECC Attribute — RO

9. The following default value checks are performed:

PCI-X Secondary Status Register Default Value (Offset 02h) — WORD

a. Split Completion Discarded — 0
b. Unexpected Split Completion — 0
c. Split Completion Overrun — 0
d. Split Request Delayed — 0

PCI-X Bridge Status Register Default Value (Offset 04h) — DWORD

a. Split Completion Discarded — 0
b. Unexpected Split Completion — 0
c. Split Completion Overrun — 0
d. Split Request Delayed — 0

Upstream Split Transaction Control Register Default Value (Offset 08h) — DWORD

a. Split Transaction Commitment Limit (value returned from Split Transaction Capacity field)

Downstream Split Transaction Control Register Default Value (Offset 0Ch) — DWORD

a. Split Transaction Commitment Limit (value returned from Split Transaction Capacity field)

PCI-X Bridge ECC Control and Status Register Default Value (Offset 10h) — DWORD

a. Select Secondary ECC registers
 (for PCI Express to PCI/PCI-X Bridge) — 1
 (for PCI/PCI-X to PCI Express Bridge) — 0
b. Additional Correctable ECC Error — 0
c. Additional Uncorrectable ECC Error — 0
d. ECC Error Phase — 000b

10. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):

a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- Configuration Space cannot be read.
- For devices other than a PCI Express to PCI/PCI-X Bridge or a PCI/PCI-X to PCI Express Bridge, the PCI-X capability is present.
- More than one PCI-X capability structure is present.
- A non-zero Next Capability Pointer field is less than or equal to 3Fh, or the lower 2 bits are non-zero.
- The PCI-X Capabilities List Item Version field contains a reserved value.
- The ECC Error Phase field contains a reserved value.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

2.2.40. TD_1_30 Root Complex Link Declaration Extended Capability Structure

The test verifies that if the function under test reports a PCI Express Root Complex Link Declaration Extended Capability structure, it is implemented as defined in the relevant specifications. (A Root Complex Link Declaration Extended Capability structure can only be implemented in a Root Port, a Root Complex Integrated Endpoint, or an RCRB. An RCRB can only be implemented in a Root Port or a Root Complex Integrated Endpoint and it cannot reside in a function's Extended Configuration space.)

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.

2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0005h (Root Complex Link Declaration Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Extended Capability ID of 0005h is found in an Extended Capability structure not in an RCRB, the device type must be a Root Port, or a Root Complex Integrated Endpoint (Root Complex Link Declaration Extended Capability structure can only be found in a Root Port, a Root Complex Integrated Endpoint, or an RCRB and an RCRB structure may not be found in Extended Configuration Space of a device). If not, the test terminates with a failure.
4. If the Extended Capability ID of 0005h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0005h is not found in an Extended Capability structure, the test skips to step 14.
5. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
6. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
7. A DWORD is read from offset 04h (Element Self Description) and the following checks are performed:
 a. If the device type is a Root Port or a Root Complex Integrated Endpoint, the Element Type field must be 0h (Configuration Space Element). All other encodings are recorded as a failure, but the test continues.
 b. If this is an RCRB, the Element Type field must be 1h (System Egress Port or internal sink) or 2h (Internal Root Complex Link). All other encodings are recorded as a failure, but the test continues.
 c. The Number of Link Entries field must be non-zero. If not, this is recorded as a failure, but the test continues.
 d. The Component ID field must be non-zero. If not, this is recorded as a failure, but the test continues.
8. Set the Number of Link Entries [NLE] to the value in the Number of Link Entries field.
9. The Link Entry counter [LE] is set to 1.
10. If [LE] is less than or equal to [NLE] the following testing is done:
 a. A DWORD is read from offset (10h + 10h * ([LE] -1)) (the Link Entry [LE] register) and if at least one of the Link Valid field or the Associate RCRB Header field returns 1 the following checks are performed, otherwise skip to step 11:
 i. The Target Component ID field must be non-zero. If not, this is recorded as a failure, but the test continues.
 ii. If the Associate RCRB Header field returns 1, then all the following must be true: the Link Type field must return 0 (link entry points to memory space); the Element Type field (Element Self Description register) must return 0h (Configuration Space Element); the Device/Port Type field (PCI Express Capabilities register) must be 0100b (Root Port) or 1001b (Root Complex Integrated Endpoint). If any are not this is recorded as a failure, but the test continues.
11. Increment [LE] by adding 1 and repeat step 10, until [LE] is greater than [NLE].

12. The following register field characteristic checks are performed:

Root Complex Link Declaration Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID — RO
b. Capability Version — RO
c. Next Capability Offset — RO

Element Self Description Register (Offset 04h) — DWORD

a. Element Type — RO
b. RsvdP_7-4 — RO-Zero
c. Number of Link Entries
 (for non-FLR testing) — HwInit
 (for FLR testing) — RO
d. Component ID
 (for non-FLR testing) — HwInit
 (for FLR testing) — RO
e. Port Number
 (for non-FLR testing) — HwInit
 (for FLR testing) — RO

Reserved Register (Offset 08h) — DWORD

a. Reserved_31-0 — RO-Zero

Reserved Register (Offset 0Ch) — DWORD

a. Reserved_31-0 — RO-Zero

13. For each Link Entry register set instance Number [n] (from 1 to [NLE]), the following register field characteristic checks and register field default value checks are performed:

Link Description Register in Link Entry (n) (Offset 10h + 10h * ([LE] -1)) — WORD

a. Link Valid
 (for non-FLR testing) — HwInit
 (for FLR testing) — RO
b. Link Type
 (for non-FLR testing) — HwInit
 (for FLR testing) — RO
c. Associate RCRB Header
 (for non-FLR testing) — HwInit
 (for FLR testing) — RO
d. RsvdP_15-3 — RO-Zero
e. Target Component ID
 (for non-FLR testing) — HwInit
 (for FLR testing) — RO
f. Target Port Number
 (for non-FLR testing) — HwInit
 (for FLR testing) — RO

Reserved Register in Link Entry (n) (Offset 14h + 10h * ([LE] -1)) — DWORD

a. Reserved_31-0 — RO-Zero

Link Address Register in Link Entry (n) (Offset 18h + 10h * ([LE] -1)) — 2 DWORDS

a. N

(if Link Type is 0)	RO-Zero
(if Link Type is 1)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO

b. RsvdP_11-3 — RO-Zero

c. Link Address Lower (bits 31-12)

(for non-FLR testing)	HwInit
(for FLR testing)	RO

d. Link Address Upper (bits 63-32)

(for non-FLR testing)	HwInit
(for FLR testing)	RO

14. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
15. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one Root Complex Link Declaration Extended Capability structure is present.
- ❑ The Root Complex Link Declaration Extended Capability structure is present in any function other than a Root Port or a Root Complex Integrated Endpoint.
- ❑ The Capability Version field does not report 1h.
- ❑ The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- ❑ The Element Type field is not one of the defined values.
- ❑ The Number of Link Entries field is zero.
- ❑ The Component ID field is zero.
- ❑ The Port Number field is zero, but the Element Type field is not 1h.
- ❑ For any Link Entry with Link Valid field or Associate RCRB field reporting 1, the Target Component ID field is zero.
- ❑ For any Link Entry with Associate RCRB field reporting 1, any of the following occur: the Link Type field is 1; the Element Type field is not 0h; device type is neither a Root Port nor a Root Complex Integrated Endpoint.
- ❑ Any of the register field characteristic tests fail.

2.2.41. TD_1_31 Root Complex Internal Link Control Extended Capability Structure

The test verifies that if the function under test reports a PCI Express Root Complex Internal Link Control Extended Capability structure, it is implemented as defined in the relevant specifications. (A Root Complex Internal Link Control Extended Capability structure can only be implemented in an RCRB. An RCRB can only be implemented in a Root Port or a Root Complex Integrated Endpoint and it cannot reside in a function's Extended Configuration space.)

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0006h (Root Complex Internal Link Control Extended Capability) are found.
3. If the Extended Capability ID of 0006h is found in an Extended Capability structure in Extended Configuration Space, the test terminates with a failure.
4. If the Extended Capability ID of 0006h is found in an Extended Capability structure for an RCRB, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0006h is not found in an Extended Capability structure for an RCRB, the test skips to step 6.
5. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0005h (Root Complex Link Declaration Extended Capability) are found. If none are found, then the test terminates with a failure. Otherwise the following checks are performed:
 a. In the Root Complex Link Declaration Capability (offset 04h), the Element Type field (Element Self Descriptor register) must be 2h (Internal Root Complex Link). If not, this is recorded as a failure, but the test continues.
6. If the Extended Capability ID of 0006h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0006h is not found in an Extended Capability structure, the test skips to step 13.

7. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
8. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
9. A DWORD is read from offset 04h (Root Complex Link Capabilities register) and the following checks are performed:
 a. For Base 1.x testing: the Max Link Speed/Supported Link Speeds field must be 0000b or 0001b. All other encodings are reserved and are recorded as a failure, but the test continues.
 b. For Base 2.x testing: the Max Link Speed/Supported Link Speeds field must be 0000b, 0001b, or 0010b. All other encodings are reserved and are recorded as a failure, but the test continues.
 c. For Base 3.x testing: the Max Link Speed/Supported Link Speeds field must be 0000b, 0001b, 0010b, or 0011b. All other encodings are reserved and are recorded as a failure, but the test continues.
 d. For Base 4.x testing: the Max Link Speed/Supported Link Speeds field must be 0000b, 0001b, 0010b, 0011b, or 0100b. All other encodings are reserved and are recorded as a failure, but the test continues.
 e. The Maximum Link Width field must be 00 0000b, 00 0001b, 00 0010b, 00 0100b, 00 1000b, 00 1100b, 01 0000b, or 10 0000b. All other encodings are reserved and are recorded as a failure, but the test continues.
 f. For Base 3.x or later testing, if the ASPM Optionality Compliance field returns 1, the following tests are performed:
 i. If the Active State Power Management (ASPM) Support field returns 00b or 10b, then the L0s Exit Latency field should return 111b. If it does not, a warning message is issued, but this is not treated in itself as a failure.
 g. For Base 3.x testing: the Supported Link Speeds Vector field must be 000 0000b, 000 0001b, 000 0010b, 000 0011b, 000 0100b, 000 0101b, 000 0110b, or 000 0111b. All other encodings are reserved and are recorded as a failure, but the test continues.
 h. For Base 4.x testing: the Supported Link Speeds Vector field must be 000 0000b, 000 0001b, 000 0010b, 000 0011b, 000 0100b, 000 0101b, 000 0110b, 000 0111b, 000 1000b, 000 1001b, 000 1010b, 000 1011b, 000 1100b, 000 1101b, 000 1110b, or 000 1111b. All other encodings are reserved and are recorded as a failure, but the test continues.
 i. For Base 3.x or later testing: for the Supported Link Speeds Vector field, determine the most significant bit value that is set to 1 and record it in Most Significant Bit [MSB]. All bits from [MSB] to 0 must also be 1. If not, this is recorded as a failure, but the test continues.
10. A WORD is read from offset 0Ah (Root Complex Link Status register) and the following checks are performed:
 a. For Base 1.x testing: the Current Link Speed field must be 0000b or 0001b. All other encodings are reserved and are recorded as a failure, but the test continues.
 b. For Base 2.x testing: the Current Link Speed field must be 0000b, 0001b or 0010b. All other encodings are reserved and are recorded as a failure, but the test continues.
 c. For Base 3.x testing: the Current Link Speed field must be 0000b, 0001b, 0010b, or 0011b. All other encodings are reserved and are recorded as a failure, but the test continues.
 d. For Base 4.x testing: the Current Link Speed field must be 0000b, 0001b, 0010b, 0011b, or 0100b. All other encodings are reserved and are recorded as a failure, but the test continues.

e. The Current Link Speed field must be equal or less than the Max Link Speed/Supported Link Speeds field (Root Complex Link Capabilities register). If not, this is recorded as a failure, but the test continues.
f. The Negotiated Link Width field must be 00 0000b, 00 0001b, 00 0010b, 00 0100b, 00 1000b, 00 1100b, 01 0000b, or 10 0000b. All other encodings are reserved and are recorded as a failure, but the test continues.
g. The Negotiated Link Width field must be equal or less than the Maximum Link Width field (Root Complex Link Capabilities register). If not, this is recorded as a failure, but the test continues.

11. The following register field characteristic checks are performed:

Root Complex Internal Link Control Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

Root Complex Link Capabilities Register (Offset 04h) — DWORD

a. Max Link Speed/Supported Link Speeds	RO
b. Maximum Link Width	RO
c. Active State Power Management (ASPM) Support	RO
d. L0s Exit Latency	RO
e. L1 Exit Latency	RO
f. Supported Link Speeds Vector (For Base 3.x or later testing)	RO
g. RsvdP_31-25 (For Base 3.x or later testing)	RO-Zero
h. RsvdP_31-18 (For Base 2.x or earlier testing)	RO-Zero

Root Complex Link Control Register (Offset 08h) — WORD

a. Active State Power Management (ASPM) Control (if Active State Power Management (ASPM) Support is non-zero)	RW
(if Active State Power Management (ASPM) Support is 00b)	RO-Zero
b. RsvdP_6-2	RO-Zero
c. Extended Sync	RW or RO-Zero
d. RsvdP_15-8	RO-Zero

Root Complex Link Status Register (Offset 0Ah) — WORD

a. Current Link Speed	RO
b. Negotiated Link Width	RO
c. RsvdZ_15-10	RO-Zero

12. The following default value checks are performed:

Root Complex Link Control Register Default Value (Offset 08h) — WORD

a. Extended Sync	0

13. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):

a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

14. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated (excluding step 3) using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ The Root Complex Internal Link Control Extended Capability structure is present in Extended Configuration Space.
- ❑ The Capability Version field does not report 1h.
- ❑ The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- ❑ The Current Link Speed field is not equal or less than the reported the Max Link Speed/Supported Link Speeds field.
- ❑ The Current Link Speed field or the Max Link Speed/Supported Link Speeds field is not one of the defined values.
- ❑ The Negotiated Link Width field is not equal or less than the reported the Maximum Link Width field.
- ❑ The Negotiated Link Width field or the Maximum Link Width field is not one of the defined values.
- ❑ The Supported Link Speeds Vector field is not one of the allowed values.
- ❑ The Supported Link Speeds Vector field does not also support all lower speeds.
- ❑ Any of the register field characteristic tests fail.
- ❑ Any of the default value tests fail.

The test *warns* if:

- ❑ When the ASPM Optionality Compliance field returns 1 (for Base 3.x or later testing only) and the Active State Power Management (ASPM) Support field returns 00b or 10b (meaning L0s is not supported), the L0s Exit Latency field returns any value other than 111b.

2.2.42. TD_1_34 RCRB Header Extended Capability Structure

The test verifies that if the function under test reports a PCI Express RCRB Header Extended Capability structure, it is implemented as defined in the relevant specifications. (An RCRB Header can only be implemented in Root Port or a Root Complex Integrated Endpoint and it cannot reside in a function's Extended Configuration space.)

Relevant Specifications

- ❑ *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 000Ah (RCRB Header Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Extended Capability ID of 000Ah is found in an Extended Capability structure in Extended Configuration Space, the test terminates with a failure.
4. If the Extended Capability ID of 000Ah is found in an Extended Capability structure for an RCRB, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 000Ah is not found in an Extended Capability structure, the test skips to step 10.
5. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
6. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
7. A WORD is read from offset 04h (Vendor ID) and the following checks are performed and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The Vendor ID register must return a valid value assigned by the PCI-SIG. (For the purposes of this test program, reads of the Vendor ID register must not return 0000h, FFFFh, or 0001h (CRS Software Visibility notification).)
8. The following register field characteristic checks are performed:

RCRB Header Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

Vendor ID Register (Offset 04h) — WORD RO

Device ID Register (Offset 064h) — WORD RO

RCRB Capabilities Register (Offset 08h) — DWORD

a. CRS Software Visibility	RO
b. RsvdP_31-1	RO-Zero

RCRB Control Register (Offset 0Ch) — DWORD

a. CRS Software Visibility Enable
 (if CRS Software Visibility is 1) RW
 (if CRS Software Visibility is 0) RO-Zero
b. RsvdP_31-1 RO-Zero

Reserved Register (Offset 10h) — DWORD

a. RsvdZ_31-0 RO-Zero

9. The following default value checks are performed:

RCRB Control Register Default Value (Offset 0Ch) — DWORD

a. CRS Software Visibility Enable 0

10. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
11. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one RCRB Header Extended Capability structure is present.
- ❑ The RCRB Header Extended Capability structure is present in Extended Configuration space.
- ❑ The Capability Version field does not report 1h.
- ❑ The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- ❑ The Vendor ID field returns 0000h, FFFFh, or 0001h.
- ❑ Any of the register field characteristic tests fail.
- ❑ Any of the default value tests fail.

2.2.43. TD_1_29 Root Complex Event Collector Endpoint Association Extended Capability Structure

The test verifies that if the function under test reports a PCI Express Root Complex Event Collector Endpoint Association Extended Capability structure, it is implemented as defined in the relevant specifications. (A Root Complex Link Declaration Extended Capability structure can only be implemented in a Root Complex Event Collector.)

Relevant Specifications

- ❑ *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0007h (Root Complex Event Collector Endpoint Association Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Extended Capability ID of 0007h is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
4. If the device type is Root Complex Event Collector, then the Extended Capability ID of 0007h must be found in an Extended Capability structure, otherwise the test terminates with a failure.
5. If the Extended Capability ID of 0007h is found in an Extended Capability structure, the device type must be Root Complex Event Collector. If not, this is recorded as a failure, but the test continues.
6. If the Extended Capability ID of 0007h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0007h is not found in an Extended Capability structure, the test skips to step 11.
7. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
8. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
9. A DWORD is read from offset 04h (Association Bitmap for Root Complex Integrated Endpoints) and the following checks are performed and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The bit position corresponding to the Root Complex Event Collector's Device Number must return 1.
 b. Starting at bit 0, and proceeding to bit 31, for each bit that returns 1, the following checks are performed:
 i. If the bit position corresponds to the Root Complex Event Collector's Device Number then this bit position is skipped, and the test continues with the next bit position that returns 1.
 ii. Test software reads location 00h of the Device Number corresponding to the bit position (Bus Number is the same as the Root Complex Event Collector's Bus Number, and Function Number is 00h) and checks that is returns a Vendor ID field that is not FFFFh.

iii. Test software checks for a PCI Express Capability structure for the Device Number corresponding to the bit position, and if it finds one it checks that the device type is Root Complex Integrated Endpoint.
iv. The test repeats step b, until all bit positions have been checked.

10. The following register field characteristic checks are performed:

RC Event Collector Endpoint Association Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID — RO
b. Capability Version — RO
c. Next Capability Offset — RO

Association Bitmap for RC Integrated Endpoints Register (Offset 04h) — DWORD

(all bits) — RO

11. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
12. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one Root Complex Event Collector Endpoint Association Extended Capability structure is present.
- ❑ An RCRB contains a Root Complex Event Collector Endpoint Association Extended Capability structure.
- ❑ The Root Complex Event Collector Endpoint Association Extended Capability structure is present in any function with a device type other than Root Complex Event Collector.
- ❑ A Root Complex Event Collector does not implement a Root Complex Event Collector Endpoint Association Extended Capability structure.
- ❑ The Capability Version field does not report 1h.
- ❑ The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- ❑ The Association Bitmap for Root Complex Endpoints register has the bit position corresponding to the Root Complex Event Collector's Device Number return 0.
- ❑ The Association Bitmap for Root Complex Endpoints register has the bit position corresponding to Device Number that is not a Root Complex Integrated Endpoint return 1.
- ❑ Any of the register field characteristic tests fail.

2.2.44. TD_1_35 Configuration Access Correlation Extended Capability Structure

The test verifies that a Base 2.x or later function under test does not implement the deprecated PCI Express Configuration Access Correlation Extended Capability.

Note: Section B.2 in Appendix B contains the previous test description for this test, as used by previous versions of the test procedure document.

Relevant Specifications

- *PCI Express Base Specification*
- *ECN Trusted Configuration Space (to Base 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 000Ch (Configuration Access Correlation Extended Capability) are found. For Base 2.x or later testing: if one or more is found, the test terminates with a failure. Otherwise the test passes.
3. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- One or more Configuration Access Correlation Extended Capability structures are present (for Base 2.x or later testing only).

2.2.45. TD_1_39 Function Level Reset

The test verifies that if a function reports support for Function Level Reset (FLR), the function under test, behaves as defined in the relevant specifications and if it is part of a multi-function device, it is not affected by Function Level Resets in the other functions in the device.

Relevant Specifications

- *PCI Express Base Specification*

- *ECN Function Level Reset (to Base 1.1)*
- *Single Root I/O Virtualization and Sharing Specification (Base 3.x or earlier only)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types with functions that support Function Level Reset and are part of a multi-function device.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Since this test uses the function under test as well as any other functions (both ARI and non-ARI), PFs, and VFs within the device under test, the test must ensure that all the necessary initialization of the hierarchy is done so that the device under test's ARI functions and VFs are visible at this point. This requires that the test re-execute the detection algorithm described in Section 1.4.1.
3. Read a DWORD located at offset 04h (Device Capabilities register) in the PCI Express Capability structure. If bit 28 (Function Level Reset Capability field) is 0, the test is terminated (this is not a failure and the test result is reported as skipped).
4. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 000Eh (ARI Extended Capability) are found. If one is found, this function is part of an ARI device.
5. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0010h (SR-IOV Extended Capability) are found. If one is found, this function is a PF and may contain VFs.
 a. Read the WORD at offset 0Eh (TotalVFs register) in the SR-IOV Extended Capability and if it is non-zero, then this PF contains associated VFs.
6. Read a byte from location 0Eh (Header Type register) in the Configuration Space. If the Multi-Function Device bit (Header Type register) returns 1, this function is part of a multi-function device.
7. For this test, the current function is the function under test. Function 0 is Function Number = 000b for a non-ARI device. Function 0 is Device Number/Function Number = 00h for an ARI device. For non-ARI functions, other functions are the complete range of Function Number 000b to 111b (excluding the current function) that return a Vendor ID field that is not FFFFh. For ARI functions, other functions are the complete range of Device Number/Function Number 00h to FFh (excluding the current function) that return a Vendor ID field that is not FFFFh. For PFs with VFs, other functions also include all VFs associated with that PF.
8. If the current function is not a VF, read a byte located at offset 04h (Device Capabilities register) in the PCI Express Capability structure and take the value in bits 2-0 (Max_Payload_Size

Supported field) and write it to offset 08h (Device Control register) bits 7-5 (Max_Payload_Size field).

9. If the current function is not a VF, read a WORD from offset 10h (Link Control register) and then re-write this WORD with all the following fields set to all 1's: Read Completion Boundary (RCB); Common Clock Configuration; Extended Synch; Enable Clock Power Management; Hardware Autonomous Width Disable. (Note: Active State Power Management (ASPM) Control field is not tested as it may affect the function's ASPM state.)
10. Modify some non-sticky field in the current function to a non-default value. Any of the following fields can be used as long as they are implemented as RW in the target: Memory Space Enable (Command register); I/O Space Enable (Command register); Bus Master Enable (Command register); Interrupt Disable (Command register). If none of these fields are implemented as RW in the target, then other non-sticky RW fields can be used. If test software cannot find any non-sticky RW field in the target, then this step is skipped.
11. For the current function, if the Capability Version field (PCI Express Capabilities register) is 2h or greater, then read a WORD from offset 30h (Link Control 2 register) and then re-write this WORD with all the following fields set to all 1's: Hardware Autonomous Speed Disable.
12. If the current function supports either a VC Extended Capability (Extended Capability ID of 0002h or 0009h) or a MFVC Extended Capability (Extended Capability ID of 0008h), then for each implemented VC, test software writes the current function's TC/VC Map field so that only the TC bit matching the VC number is 1 and the other TCs are 0 (for VC0: TC0=1, TC1-7=0; for VC7: TC0-6=0, TC7=1).
13. For the current function only, read the following register fields and record their current value:

Device Capabilities Register (Offset 04h) – DWORD

a. Captured Slot Power Limit Value
b. Captured Slot Power Limit Scale

Device Control Register (Offset 08h) – WORD

a. Max_Payload_Size

Link Control Register (Offset 10h) – WORD

a. Active State Power Management (ASPM) Control
b. Read Completion Boundary (RCB)
c. Common Clock Configuration
d. Extended Synch
e. Enable Clock Power Management
f. Hardware Autonomous Width Disable

Link Control 2 Register (Offset 30h) – WORD (if PCI Express Capability Version > 1)

a. Hardware Autonomous Speed Disable

Virtual Channel Extended Capability Structure (if present)

a. TC/VC Map field in all VC Resource Control registers

Multi-Function Virtual Channel Extended Capability Structure (if present)

a. TC/VC Map field in all VC Resource Control registers

Secondary PCI Express Extended Capability Structure (if present)

a. All Lane Equalization Control Entry registers

Physical Layer 16.0 GT/s Extended Capability Structure (if present)

a. All 16.0 GT/s Lane Equalization Control Entry registers (if present)

Margining Extended Capability Structure (if present)

a. All Margining Lane Control registers (if present)

SR-IOV Extended Capability Structure (if present)

a. ARI Capable Hierarchy

14. For the current function, read a byte from location 0Eh (Header Type register) in the Configuration Space. If the Multi-Function Device bit is 0, skip to step 19.
15. For each other function in the device, read a DWORD located at offset 04h (Device Capabilities register) in the PCI Express Capability structure. If bit 28 (Function Level Reset Capability field) is 1, write a WORD to offset 08h (Device Control register) with bit 15 (Initiate Function Level Reset field) set to 1. After writing each individual function, test software waits 100 ms before writing the next function. After the last function is written, test software waits 100 ms before proceeding.
16. If a non-sticky RW field was found in step 10, test software verifies the same non-sticky field (from step 10) in the current function only is not reset to its default value. If the value has changed, the test fails.
17. Repeat steps 2-6, to recheck the number of functions in the device. If the number of functions in the device has changed and the current function is still present, this is recorded as a failure, and the test continues. If current function is no longer present, this is recorded as a failure, and the test terminates.
18. For the current function only, read all the register fields listed in step 13 and check that their values are the same as the previously record value. If any value has changed, the test fails.
19. For the current function, read a DWORD located at offset 04h (Device Capabilities register) in the PCI Express Capability structure. If bit 28 (Function Level Reset Capability field) is 1, write a WORD to offset 08h (Device Control register) with bit 15 (Initiate Function Level Reset field) set to 1. After writing, test software waits 100 ms before proceeding.
20. Repeat steps 2-6, to recheck the number of functions in the device. If the number of functions in the device has changed and the current function is still present, this is recorded as a failure, and the test continues. If current function is no longer present, this is recorded as a failure, and the test terminates.
21. If a non-sticky RW field was found in step 10, test software verifies the same non-sticky field (from step 10) in the current function only is reset to its default value. If the value has not changed to the default value, the test fails, and is terminated (as the FLR cannot be confirmed to have happened).
22. For the current function only, read all the register fields listed in step 13 and check that their values are the same as the previously record value. If any value has changed, this is recorded as a failure, but the test continues.
23. Since a FLR to a PF will disable all VFs, the test must ensure that all the necessary initialization of the hierarchy is done so that the device under test's ARI functions and VFs are visible again at this point. This requires that the test re-execute the detection algorithm described in Section 1.4.1.

24. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- ❑ The number of functions in the device has changed following a Function Level Reset.
- ❑ Configuration Space registers cannot be read following a Function Level Reset.
- ❑ A non-sticky register field value has changed following the Function Level Reset to another function.
- ❑ A non-sticky register field value has not changed following the Function Level Reset to the function.
- ❑ Any of the listed register fields values have changed following the Function Level Reset to another function.
- ❑ Any of the listed register fields values have changed following the Function Level Reset to the function.

2.2.46. TD_1_42 ACS Extended Capability Structure

The test verifies that if the PCI Express function under test reports an ACS Extended Capability structure, it is implemented as defined in the relevant specifications.

Relevant Specifications

- ❑ *PCI Express Base Specification*
- ❑ *ECN Access Control Services (to Base 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 000Dh (ACS Extended Capability) are found. If more than one is found, the test terminates with a failure.

3. If the Extended Capability ID of 000Dh is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
4. If the Extended Capability ID of 000Dh is found in an Extended Capability structure, in a function where the Multi-Function Device field (Header Type register) returns 0 (a single function device), the device type must be an Endpoint, a Legacy Endpoint, a Root Complex Integrated Endpoint, a Root Port, or a Switch Downstream Port. If not, this is recorded as a failure and the test is terminated, otherwise the following tests are performed:
 a. For an Endpoint or a Legacy Endpoint, check that the function implements a SR-IOV Extended Capability structure (Extended Capability ID of 0010h). If not, this is recorded as a failure and the test is terminated.
5. If the Extended Capability ID of 000Dh is found in an Extended Capability structure, in a function where the Multi-Function Device field (Header Type register) returns 1 (a multi-function device), the device type must be an Endpoint, a Legacy Endpoint, a Root Complex Integrated Endpoint, a Switch Upstream Port, a Root Port, or a Switch Downstream Port. If not, this is recorded as a failure and the test is terminated.
6. If the Extended Capability ID of 000Dh is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 000Dh is not found in an Extended Capability structure, the test skips to step 20.
7. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
8. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
9. A WORD is read from offset 04h (ACS Capability register).
10. If the device type is a Root Port or a Switch Downstream Port, the ACS Source Validation field must be 1. For other device types it must be 0. If not, this is recorded as a failure, but the test continues.
11. If the device type is a Root Port or a Switch Downstream Port, the ACS Translation Blocking field must be 1. For other device types it must be 0. If not, this is recorded as a failure, but the test continues.
12. If the device type is a Switch Downstream Port, the ACS P2P Request Redirect field must be 1. If not, this is recorded as a failure, but the test continues.
13. If the device type is a Switch Downstream Port, the ACS Upstream Forwarding field must be 1. For Switch Upstream Port and Endpoint device types the field must be 0. If not, this is recorded as a failure, but the test continues.
14. If the device type is a Switch Downstream Port, the ACS Direct Translated P2P field must be 1. If not, this is recorded as a failure, but the test continues.
15. If the ACS P2P Request Redirect field is 1, then the ACS P2P Completion Redirect field must be 1. If not, this is recorded as a failure, but the test continues.
16. A WORD is read from offset 06h (ACS Control register).

17. If the ACS P2P Egress Control field is 1:
 a. For a Root Port or Switch Downstream Port, if the Egress Control Vector Size field is not 00h, then the Egress Control Vector Size field value must be greater than or equal to the Port Number field (Link Capabilities register) value. If not, this is recorded as a failure, but the test continues.
 b. Calculate the Egress Vector Size [EVS] value as follows: if the Egress Control Vector Size field is 00h, then [EVS] = 8. If the Egress Control Vector Size field is not 00h, then [EVS] = (the Egress Control Vector Size field value divided by 32, rounded up to the next integer number).
 c. If the function under test is part of an ARI device, the [EVS] value must be any power of 2 between 8 and 256. If not, this is recorded as a failure and the test skips to step 18.
 d. Test software reads [EVS] DWORDs starting from offset 08h (Egress Control Vector register). It constructs the Egress Control Vector value by combining all the read DWORDs into a single value such that, the last DWORD read is the most significant DWORD of the vector, down to the first DWORD read which is the least significant DWORD of the vector. The vector can be up to 256 bits long and the least significant bit of the vector represents port/function 0.
 e. For a Root Port or Switch Downstream Port, if the Egress Control Vector Size field is not 00h and the Egress Control Vector Size field value is greater than or equal to the Port Number field (Link Capabilities register) value, the bit in the Egress Control Vector corresponding to the Port Number field (Link Capabilities register) value must be RO-Zero. If not, this is recorded as a failure, but the test continues. The rest of the Egress Control Vector must be RW for the number of bits indicated in the Egress Control Vector Size (however, if the function under test is a Root Port a bit corresponding to an internal port may also be RO-Zero). If not, this is recorded as a failure, but the test continues. Any remaining bits must be RO-Zero (RsvdP). If not, this is recorded as a failure, but the test continues.
 f. For a function in a non-ARI device, the bit corresponding to the current function number of the function under test must be RO-zero. If not, this is recorded as a failure, but the test continues. The rest of the Egress Control Vector must be RW for the number of bits indicated in the Egress Control Vector Size field. If not, this is recorded as a failure, but the test continues. Any remaining bits must be RO-Zero (RsvdP). If not, this is recorded as a failure, but the test continues.

18. The following register field characteristic checks are performed:

ACS Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

ACS Capability Register (Offset 04h) — WORD

a. ACS Source Validation	RO
b. ACS Translation Blocking	RO
c. ACS P2P Request Redirect	RO
d. ACS P2P Completion Redirect	RO
e. ACS Upstream Forwarding	RO
f. ACS P2P Egress Control	RO
g. ACS Direct Translated P2P	RO

h. RsvdP_7 RO-Zero
i. Egress Control Vector Size
(for non-FLR testing) HwInit
(for FLR testing) RO

ACS Control Register (Offset 06h) — WORD

a. ACS Source Validation Enable
(if ACS Source Validation is 0) RO-Zero
(if ACS Source Validation is 1) RW
b. ACS Translation Blocking Enable
(if ACS Translation Blocking is 0) RO-Zero
(if ACS Translation Blocking is 1) RW
c. ACS P2P Request Redirect Enable
(if ACS P2P Request Redirect is 0) RO-Zero
(ACS P2P Request Redirect is 1) RW
d. ACS P2P Completion Redirect Enable
(if ACS P2P Completion Redirect is 0) RO-Zero
(if ACS P2P Completion Redirect is 1) RW
e. ACS Upstream Forwarding Enable
(if ACS Upstream Forwarding is 0) RO-Zero
(if ACS Upstream Forwarding is 1) RW
f. ACS P2P Egress Control Enable
(if ACS P2P Egress Control is 0) RO-Zero
(if ACS P2P Egress Control is 1) RW
g. ACS Direct Translated P2P Enable
(if ACS Direct Translated P2P is 0) RO-Zero
(if ACS Direct Translated P2P is 1) RW
h. RsvdP_15-7 RO-Zero

19. The following default value checks are performed:

ACS Control Register Default Value (Offset 06h) — WORD

a. ACS Source Validation Enable 0
b. ACS Translation Blocking Enable 0
c. ACS P2P Request Redirect Enable 0
d. ACS P2P Completion Redirect Enable 0
e. ACS Upstream Forwarding Enable 0
f. ACS P2P Egress Control Enable 0
g. ACS Direct Translated P2P Enable 0

20. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
21. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is

itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- More than one ACS Extended Capability structure is present.
- An RCRB contains an ACS Extended Capability structure.
- The ACS Extended Capability structure is present in any function other than the following: Root Port; Switch Downstream Port; Root Complex Integrated Endpoint; single function Endpoint device without a SR-IOV Extended Capability structure; multi-function Endpoint device; multi-function Switch with Upstream Port.
- The Capability Version field does not report 1h.
- The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- The device is a Root Port and it does not report the following fields as 1: ACS Source Validation; ACS Translation Blocking.
- The device is a Switch Downstream Port and it does not report the following fields as 1: ACS Source Validation; ACS Translation Blocking; ACS P2P Request Redirect; ACS Upstream Forwarding; ACS Direct Translated P2P.
- The device is a Switch Upstream Port or an Endpoint and it reports the following fields as 1: ACS Source Validation; ACS Translation Blocking; ACS Upstream Forwarding.
- The function reports the ACS P2P Request Redirect field as 1, but does not report the ACS P2P Completion Redirect field as 1.
- The function reports the ACS P2P Egress Control field as 1 but the Egress Control Vector is not implemented correctly, either in terms of the vector size, or the vector bit attributes.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

2.2.47. TD_1_43 ARI Extended Capability Structure

The test verifies that if the function under test reports an Alternate Routing ID (ARI) Extended Capability structure, it is implemented as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *ECN Alternate Routing-ID Interpretation (to Base 2.0 and Base 1.1)*
- *ECN Access Control Services (to Base 1.1)*
- *Single Root I/O Virtualization and Sharing Specification (Base 3.x or earlier only)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 000Eh (ARI Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Extended Capability ID of 000Eh is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
4. If the Extended Capability ID of 000Eh is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 000Eh is not found in an Extended Capability structure, the test skips to step 14.
5. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
6. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
7. The device type must be an Endpoint, a Legacy Endpoint, or a Switch Upstream Port (but not a Root Complex Integrated Endpoint). If not, this is recorded as a failure and the test is terminated.
8. A WORD is read from offset 04h (ARI Capability register).
9. If the MFVC Function Groups Capability field reports 1, then the function number must be 0. If not, this is recorded as a failure, but the test continues.
10. If the ACS Function Groups Capability field reports 1, then the function number must be 0. If not, this is recorded as a failure, but the test continues.
11. If the Next Function Number field is non-zero, it must be a value greater than the current function number. If not, this is recorded as a failure, but the test continues.
12. The following register field characteristic checks are performed:

ARI Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

ARI Capability Register (Offset 04h) — WORD

a. MFVC Function Groups Capability	RO
b. ACS Function Groups Capability	RO
c. RsvdP_7-2	RO-Zero
d. Next Function Number (for non-VFs)	RO

ARI Control Register (Offset 06h) –– WORD

a. MFVC Function Groups Enable
 (if MFVC Function Groups Capability is 0
 or function number is non-zero) RO-Zero
 (if MFVC Function Groups Capability is 1 and function number is zero) RW
b. ACS Function Groups Enable
 (if ACS Function Groups Capability is 0 or function number is non-zero) RO-Zero
 (if ACS Function Groups Capability is 1 and function number is zero) RW
c. RsvdP_3-2 RO-Zero
d. Function Group
 (if function 0 of the device reports both MFVC Function Groups Capability
 and ACS Function Groups Capability as 0) RO-Zero
 (if function 0 of the device reports either MFVC Function Groups Capability
 or ACS Function Groups Capability as 1) RW
e. RsvdP_15-7 RO-Zero

13. The following default value checks are performed:

ARI Control Register Default Value (Offset 06h) –– WORD

a. MFVC Function Groups Enable 0
b. ACS Function Groups Enable 0
c. Function Group 000b

14. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
15. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one ARI Extended Capability structure is present.
- ❑ An RCRB contains an ARI Extended Capability structure.
- ❑ The ARI Extended Capability structure is present in any function other than the following: Endpoint; Legacy Endpoint; Switch Upstream Port.
- ❑ The Capability Version field does not report 1h.
- ❑ The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- ❑ A function other than 0, reports the MFVC Function Groups Capability field as 1.
- ❑ A function other than 0, reports the ACS Function Groups Capability field as 1.
- ❑ A function reports a non-zero Next Function Number field that is lower than the function's number.

- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

2.2.48. TD_1_44 DPA Extended Capability Structure

The test verifies that if the function under test reports a DPA Extended Capability structure, it is implemented as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *ECN Dynamic Power Allocation (to Base 2.0)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0016h (DPA Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. For Base 1.x testing: if the Extended Capability ID of 0016h is found in an Extended Capability structure, the test terminates with a failure.
4. For Base 2.x or later testing: if the Extended Capability ID of 0016h is found in an Extended Capability structure for a VF, the test terminates with a failure.
5. For Base 2.x or later testing: if the Extended Capability ID of 0016h is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
6. For Base 2.x or later testing: if the Extended Capability ID of 0016h is found in an Extended Capability structure for a device type that is not an Endpoint, not a Legacy Endpoint, and not a Root Complex Integrated Endpoint, then the test terminates with a failure.
7. For Base 2.x or later testing: if the Extended Capability ID of 0016h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0016h is not found in an Extended Capability structure, the test skips to step 22.
8. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.

9. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
10. A DWORD is read from offset 04h (DPA Capability register).
11. The Transition Latency Unit field must return a valid value (00b, 01b, or 10b). If not, this is recorded as a failure, but the test continues.
12. A DWORD is read from offset 08h (DPA Latency Indicator register).
13. The value returned in the Substate_Max field is used to determine the upper implemented bit. All bits in the DPA Latency Indicator register above the upper implemented bit must return 0. If not, this is recorded as a failure, but the test continues.
14. The following register field characteristic checks are performed:

DPA Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

DPA Capability Register (Offset 04h) — DWORD

a. Substate_Max	RO
b. RsvdP_7-5	RO-Zero
c. Transition Latency Unit	RO
d. RsvdP_11-10	RO-Zero
e. Power Allocation Scale	RO
f. RsvdP_15-14	RO-Zero
g. Transition Latency Value 0	RO
h. Transition Latency Value 1	RO

DPA Latency Indicator Register (Offset 08h) — DWORD

a. (bits [Substate_Max] to 0)	RO
b. (if [Substate_Max] is less than 31: bits 31 to [Substate_Max] + 1)	RO-Zero

DPA Status Register (Offset 0Ch) – WORD

a. Substate Status	RO
b. RsvdZ_7-5	RO-Zero
c. Substate Control Enabled	RW1C
d. RsvdZ_15-9	RO-Zero

DPA Control Register (Offset 0Eh) — WORD

a. Substate Control	RW
b. RsvdP_15-5	RO-Zero

15. The following default value checks are performed:

DPA Status Register Default Value (Offset 0Ch) — WORD

a. Substate Status	0 0000b
b. Substate Control Enabled	1

DPA Control Register Default Value (Offset 0Eh) — WORD

a. Substate Control	0

16. Determine the number of implemented substates and set the SubState Maximum [SSMax] to the value in the Substate_Max field plus 1. The SubState [SS] value will be used to hold the desired substate.
17. Create the value of the previous DPA Power Allocation Array byte and set [PrvDPA] to FFh, in order to set it to the maximum possible value.
18. Read byte starting at offset 10h (DPA Power Allocation Array).
 a. Test software records the byte value in Current DPA [CurDPA], which is the holder of the current DPA Power Allocation Array byte.
 b. Verify that [CurDPA] is less than or equal to [PrvDPA]. If not, then a warning message is issued, but this is not treated in itself as a failure and the test continues.
 c. Verify that [CurDPA] is non-zero. If it is zero, then a warning message is issued, but this is not treated in itself as a failure and the test continues.
 d. Write to the byte with an inverted data pattern.
 e. Read the same byte again.
 f. Verify that the returned value still matches the value in [CurDPA] (this verifies the array is RO). If not, this is recorded as a failure, but the test continues.
 g. Copy [CurDPA] to [PrvDPA], to prepare for the next byte.
19. Repeat step 18 by continuing to read and check subsequent bytes until [SSMax] bytes are read and checked.
20. Test software tests each supported substate can be reached as follows:
 a. If [SSMax] is greater than 1, then set the desired substate value [SS] to 1. If [SSMax] is 1, then set the desired substate value [SS] to 0.
 b. Read the Substate Status field and record the value (to be called previous substate).
 c. Test software calculates the Transition Latency Delay [TLD] as follows for the desired substate [SS]:
 i. Use [SS] as a bit index into the DPA Latency Indicator register and determine if the corresponding bit returns 0 or 1.
 ii. If the bit returned 0, then [TLD] is the value returned in the Transition Latency Value 0 field multiplied by the factor returned in the Transition Latency Unit field.
 iii. If the bit returned 1, then [TLD] is the value returned in the Transition Latency Value 1 field multiplied by the factor returned in the Transition Latency Unit field.
 d. Write [SS] to the Substate Control field.
 e. Delay for a period of time equal to [TLD].
 f. Read the Substate Status field to verify the function's current substate.
 i. If the Substate Control Enabled field returns 1, then if the Substate Status field does not return the same value as [SS], a failure is recorded and the test skips to step 22, otherwise the test continues.
 ii. If the Substate Control Enabled field returns 0, then if the Substate Status field does not return the same value as the previous substate, a failure is recorded and the test skips to step 22, otherwise the test continues.
 g. Increment [SS] and repeat steps b-g until [SSMax] is reached.
 h. If [SSMax] is greater than 1, then set the desired substate value [SS] to 0.
 i. If [SSMax] is greater than 1, then repeat steps b-f just once more and then terminate.
21. Write the Substate Control Enabled field with 1 (to clear the RW1C field) and repeat step 20 (this verifies that substate control can be disabled).

22. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
23. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one DPA Extended Capability structure is present.
- ❑ A VF contains a DPA Extended Capability structure.
- ❑ An RCRB contains a DPA Extended Capability structure.
- ❑ The DPA Extended Capability structure is present in any function other than the following: Endpoint; Legacy Endpoint; Root Complex Integrated Endpoint.
- ❑ The Capability Version field does not report 1h.
- ❑ The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- ❑ The Transition Latency Unit field returns a reserved value.
- ❑ The DPA Transition Latency register returns a non-zero bit for an unsupported substate.
- ❑ Any of the register field characteristic tests fail.
- ❑ Any of the default value tests fail.
- ❑ The function is unable to reach a supported substate, in the latency time reported.
- ❑ Clearing the Substate Control Enable field does not prevent substate transitions from occurring.

The test *warns* if:

- ❑ The DPA Power Allocation Array returns a higher value for a supported substate, then the preceding substate.
- ❑ The DPA Power Allocation Array returns a 0W value for a supported substate.

2.2.49. TD_1_45 Resizable BAR Extended Capability Structure

The test verifies that if the function under test reports a Resizable BAR Extended Capability structure, it is implemented as defined in the relevant specifications.

Relevant Specifications

- ❑ *PCI Express Base Specification*
- ❑ *ECN Resizable BAR Capability (to Base 2.0)*
- ❑ *ECN Expanded Resizable BARS (to Base 3.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Test software writes 0 to both the Memory Space Enable field and the Bus Master Enable field in the Command register (this disables responses to memory cycles targeting the function's BAR spaces and prevents the function from generating any requests).
3. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0015h (Resizable BAR Extended Capability) are found. If more than one is found, the test terminates with a failure.
4. For Base 1.x testing: if the Extended Capability ID of 0015h is found in an Extended Capability structure, the test terminates with a failure.
5. For Base 2.x or later testing: if the Extended Capability ID of 0015h is found in an Extended Capability structure for a VF, the test terminates with a failure.
6. For Base 2.x or later testing: if the Extended Capability ID of 0015h is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
7. For Base 2.x or later testing: if the Extended Capability ID of 0015h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0015h is not found in an Extended Capability structure, the test skips to step 21.
8. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
9. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
10. The following register field characteristic checks are performed:

 Resizable BAR Extended Capability Header (Offset 00h) — DWORD

 a. PCI Express Extended Capability ID — RO
 b. Capability Version — RO
 c. Next Capability Offset — RO

11. A DWORD is read from offset 08h (Resizable BAR Control register 0).

12. The Number of Resizable BARs field (Resizable BAR Control register 0) must return a valid value (01h to 06h). If not, this is recorded as a failure, and the test is terminated.
13. The number of Resizable BARs Maximum [RBMax] is the value from the Number of Resizable BARs (Resizable BAR Control register 0) minus 1.
14. A DWORD is read from offset 04h (Resizable BAR Capability register 0).
15. Continue reading subsequent DWORDs until offset ([RBMax] * 08h) + 08h (Resizable BAR Control register [RBMax]) is read.
16. For each Resizable BAR register set instance Number [n] (from 0 to [RBMax]), the following register field characteristic checks are performed:

Resizable BAR Capability Register [n] (Offset [n] * 08h + 04h) — DWORD

a. RsvdP_3-0	RO-Zero
b. (bits 31-4)	
(For Base 3.1 or later testing)	RO
c. (bits 23-4)	
(For Base 3.0 or earlier testing)	RO
d. RsvdP_31-24	
(For Base 3.0 or earlier testing)	RO-Zero

Resizable BAR Control Register [n] (Offset [n] * 08h + 08h) — DWORD

a. BAR Index	RO
b. RsvdP_4-3	RO-Zero
c. Number of Resizable BARs	
(for [n] = 0)	RO
(for [n] not 0)	RO-Zero
d. BAR Size	
(bits 4-0)	RW
(For Base 4.x or later testing)	
(if Resizable BAR Control[31:22] is non-zero: bit 5)	RW
(if Resizable BAR Control[31:22] is zero: bit 5)	RW or RO-Zero
(For Base 3.1 testing: bit 5)	RW or RO-Zero(only values corresponding to supported BAR sizes are used)
e. RsvdP_15-14	
(For Base 3.1 or later testing)	RO-Zero
f. (bits 31-16)	
(For Base 3.1 or later testing)	RO
g. RsvdP_31-13	
(For Base 3.0 or earlier testing)	RO-Zero

17. For each Resizable BAR register set instance Number [n] (from 0 to [RBMax]), the following default value checks are performed

Resizable BAR Control Register [n] (Offset [n] * 08h + 08h) — DWORD

a. BAR Size	
(For Base 3.1 or later testing: bit 5)	0

18. Set the current resizable BAR number [nBAR] to 0.

19. Test software tests each resizable BAR as follows:
 a. Check that the Resizable BAR Capability register [nBAR] has bits 23 to 4 return a non-zero value. If not, the test fails and testing continues with the next resizable BAR.
 b. Check that the BAR Index field in Resizable BAR Control register [nBAR] returns a valid value (0 to 5). If not, the test fails, and testing continues with the next resizable BAR.
 c. Check that the BAR location indicated by the value returned in the BAR Index field in Resizable BAR Control register [nBAR] is a Memory Space BAR, by ensuring that the BAR is a valid BAR and that the BAR's bit 0 returns 0. If not, the test fails, and testing continues with the next resizable BAR.
 d. Read the Type field, of the BAR location indicated by the value returned in the BAR Index field of the Resizable BAR Control register [nBAR], and if it is 00b (32 bit BAR), then the following checks are performed and if any are not as stated, this is recorded as a failure, and testing continues with the next resizable BAR.
 i. The Resizable BAR Capability register [nBAR] bits 23-16 must return 0.
 ii. For Base 3.1 or later testing only: the Resizable BAR Capability register [nBAR] bits 31-24 must return 0.
 iii. For Base 3.1 or later testing only: the Resizable BAR Control register [nBAR] bits 31-16 must return 0.
 e. Test the resizable BAR controls as follows:
 i. Set the value of maximum resizable BAR bits [RBbitmax] to 24.
 ii. For Base 3.1 or later testing only: write 10 000b to BAR Size field bits 5-0. Then read back BAR Size field bit 5, and if returns 1, set [RBbitmax] to 48
 iii. Set the value of resizable BAR capability bit number [RBbit] to 4.
 iv. Set the value of Resizable BAR Size [RBSize] to 00 0000b.
 v. If [RBbit] is less than or equal to 31 and the Resizable BAR Capability register [nBAR] bit [RBbit] returns a 1 or if [RBbit] is greater than 31 and less than or equal to 47 and the Resizable BAR Control register [nBAR] bit ([RBbit] – 16) returns 1, then write the [RBSize] value to the BAR Size field of Resizable BAR Control register [nBAR]. Otherwise go to step xi.
 vi. Read back the BAR Size field of Resizable BAR Control register [nBAR] and check that it returns the value written. If not, then the test fails and testing continues with the next resizable BAR.
 vii. If the Type field, of the BAR location indicated by the value returned in the BAR Index field in the Resizable BAR Control register [nBAR], is 00b (32 bit BAR), then read back that 32 bit BAR location and verify that bits ([RBbit] + 15) to 4 return 0. If not, then the test fails and testing continues with the next resizable BAR. (This tests that BAR bits that are changed from RW to RO are automatically cleared to 0 by the hardware.)
 viii. If the Type field, of the BAR location indicated by the value returned in the BAR Index field in the Resizable BAR Control register [nBAR], is 10b (64 bit BAR), then read back that 64 bit BAR location (BAR Index returns the address of the lower 32 bits of the BAR) and verify that bits ([RBbit] + 15) to 4 return 0. If not, then the test fails and testing continues with the next resizable BAR. (This tests that BAR bits that are changed from RW to RO are automatically cleared to 0 by the hardware.)
 ix. If the Type field, of the BAR location indicated by the value returned in the BAR Index field in the Resizable BAR Control register [nBAR], is 00b (32 bit BAR), then write FFFF FFFFh to that 32 bit BAR location. Read back the same 32 bit BAR location and verify that bits 31 to ([RBbit] + 16) return 1, and that bits ([RBbit] + 15) to 4 return 0. If not, then the test fails and testing continues with the next resizable BAR.

x. If the Type field, of the BAR location indicated by the value returned in the BAR Index field in the Resizable BAR Control register [nBAR], is 10b (64 bit BAR), then write FFFF FFFF FFFF FFFFh to that 64 bit BAR location (BAR Index returns the address of the lower 32 bits of the BAR). Read back the same 64 bit BAR location and verify that bits 63 to ([RBbit] + 16) return 1, and that bits ([RBbit] + 15) to 4 return 0. If not, then the test fails and testing continues with the next resizable BAR.
xi. Increment [RBbit] by 1. Increment [RBSize] by 1.
xii. If [RBbit] is less than [RBbitmax], then repeat steps v to xii. If [RBbit] is equal to [RBbitmax], go to the next step.

20. Increment [nBAR] by 1. If the new value of [nBAR] is less than or equal to [RBMax], then repeat steps 19-20. Otherwise go to the next step.
21. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
22. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- More than one Resizable BAR Extended Capability structure is present.
- A VF contains a Resizable BAR Extended Capability structure.
- An RCRB contains a Resizable BAR Extended Capability structure.
- The Capability Version field does not report 1h.
- The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- The Number of Resizable BARs field in the Resizable BAR Control register 0 returns a reserved value.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.
- Any implemented Resizable BAR Capability register returns a zero value.
- Any implemented Resizable BAR Control register returns a reserved value in the BAR Index field.
- Any implemented Resizable BAR Control register returns a non-memory BAR value in the BAR Index field.
- Any implemented Resizable BAR Control register returns a 32 bit memory BAR value in the BAR Index field, but the corresponding Resizable BAR Capability register returns a value indicating support for 4 GB or greater BAR size.

- Any implemented Resizable BAR Control register returns a 32 bit memory BAR value in the BAR Index field, but the corresponding Resizable BAR Control register bits 31-16 returns a value indicating support for 256 TB or greater BAR size (for Base 3.1 or later testing only).
- Any implemented Resizable BAR Control register does not allow valid values to be written to the BAR Size field.
- Any implemented Resizable BAR Control register does not force the corresponding BAR bits to be cleared to 0, when writing a value to the BAR Size field that will make the BAR bits change from RW to RO.
- Any implemented Resizable BAR Control register does not force the corresponding BAR bits to become RO, when writing a value to the BAR Size field that will make the BAR bits change from RW to RO.

2.2.50. TD_1_69 VF Resizable BAR Extended Capability Structure

The test verifies that if the function under test reports a VF Resizable BAR Extended Capability structure, it is implemented as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *Single Root I/O Virtualization and Sharing Specification (Base 3.x or earlier only)*
- *ECN VF Resizable BAR Capability (to SR-IOV 1.1)*
- *ECN Expanded Resizable BARS (to Base 3.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. If the function under test is a PF, test software writes 0 to both the VF Enable field and the VF MSE field in the SR-IOV Control register (this allows the System Page Size register to be updated, and disables responses to memory cycles targeting the VF BAR spaces).
3. Set the value of Page Size bit [PSbit] to 0.
4. If the function under test is a PF, test software writes 00000001h to the System Page Size register (this sets the VF BAR size granularity to 4 KB).

5. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0024h (VF Resizable BAR Extended Capability) are found. If more than one is found, the test terminates with a failure.
6. For Base 1.x testing: if the Extended Capability ID of 0024h is found in an Extended Capability structure, the test terminates with a failure.
7. For Base 2.x or later testing: if the Extended Capability ID of 0024h is found in an Extended Capability structure for a VF, the test terminates with a failure.
8. For Base 2.x or later testing: if the Extended Capability ID of 0024h is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
9. For Base 2.x or later testing: if the Extended Capability ID of 0024h is found in an Extended Capability structure for a function that is not a PF, the test terminates with a failure.
10. For Base 2.x or later testing: if the Extended Capability ID of 0024h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0024h is not found in an Extended Capability structure, the test skips to step 28.
11. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
12. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
13. The following register field characteristic checks are performed:

 VF Resizable BAR Extended Capability Header (Offset 00h) — DWORD

 a. PCI Express Extended Capability ID — RO
 b. Capability Version — RO
 c. Next Capability Offset — RO

14. A DWORD is read from offset 08h (VF Resizable BAR Control register 0).
15. The Number of VF Resizable BARs field (VF Resizable BAR Control register 0) must return a valid value (01h to 06h). If not, this is recorded as a failure, and the test is terminated.
16. The number of resizable VF BARs [RBMax] is the value from the Number of VF Resizable BARs (VF Resizable BAR Control register 0) minus 1.
17. A DWORD is read from offset 04h (VF Resizable BAR Capability register 0).
18. Continue reading subsequent DWORDs until offset ([RBMax] * 08h) + 08h (VF Resizable BAR Control register [RBMax]) is read.
19. For each VF Resizable BAR register set instance Number [n] (from 0 to [RBMax]), the following register field characteristic checks are performed:

 VF Resizable BAR Capability Register [n] (Offset [n] * 08h + 04h) — DWORD

 a. RsvdP_3-0 — RO-Zero
 b. (bits 31-4)
 (For Base 3.1 or later testing) — RO
 c. (bits 23-4)
 For Base 3.0 or earlier testing) — RO

d. RsvdP_31-24
(For Base 3.0 or earlier testing) RO-Zero

VF Resizable BAR Control Register [n] (Offset [n] * 08h + 08h) — DWORD

a. VF BAR Index RO
b. RsvdP_4-3 RO-Zero
c. Number of VF Resizable BARs
(for [n] = 0) RO
(for [n] not 0) RO-Zero
d. VF BAR Size RW
(only values corresponding to supported VF BAR sizes are used)
e. RsvdP_15-14 RO-Zero
f. (bits 31-16)
(For Base 3.1 or later testing) RO
g. RsvdP_31-16
(For Base 3.0 or earlier testing) RO-Zero

20. Set the current resizable VF BAR number [nBAR] to 0.
21. Test software tests each resizable VF BAR as follows:
 a. Check that the VF Resizable BAR Capability register [nBAR] has bits 23 to 4 return a non-zero value. If not, the test fails and testing continues with the next resizable VF BAR.
 b. Check that the VF BAR Index field in VF Resizable BAR Control register [nBAR] returns a valid value (0 to 5). If not, the test fails, and testing continues with the next resizable VF BAR.
 c. Check that the BAR location indicated by the value returned in the VF BAR Index field in VF Resizable BAR Control register [nBAR] is a Memory Space VF BAR, by ensuring that the VF BAR is a valid VF BAR and that the VF BAR's bit 0 returns 0. If not, the test fails, and testing continues with the next resizable VF BAR.
 d. Read the Type field, of the VF BAR location indicated by the value returned in the VF BAR Index field of the VF Resizable BAR Control register [nBAR], and if it is 00b (32 bit BAR), then the following checks are performed and if any are not as stated, this is recorded as a failure, and testing continues with the next resizable VF BAR.
 i. The VF Resizable BAR Capability register [nBAR] bits 23-16 must return 0.
 ii. For Base 3.1 or later testing only: the VF Resizable BAR Capability register [nBAR] bits 31-24 must return 0.
 iii. For Base 3.1 or later testing only: the VF Resizable BAR Control register [nBAR] bits 31-16 must return 0.
 e. Test the resizable VF BAR controls as follows:
 i. Set the value of maximum resizable VF BAR bits [RBbitmax] to 24.
 ii. For Base 3.1 or later testing only: write 10 000b to VF BAR Size field bits 5-0. Then read back VF BAR Size field bit 5, and if returns 1, set [RBbitmax] to 48
 iii. Set the value of resizable VF BAR capability bit number [RBbit] to 4.
 iv. Set the value of VF Resizable BAR Size [RBSize] to 00 0000b.
 v. If [RBbit] is less than or equal to 31 and the VF Resizable BAR Capability register [nBAR] bit [RBbit] returns a 1 or if [RBbit] is greater than 31 and less than or equal to 47 and the VF Resizable BAR Control register [nBAR] bit ([RBbit] – 16) returns 1, then write the [RBSize] value to the VF BAR Size field of VF Resizable BAR Control register [nBAR]. Otherwise go to step xi.

vi. Read back the VF BAR Size field of VF Resizable BAR Control register [nBAR] and check that it returns the value written. If not, then the test fails and testing continues with the next resizable VF BAR.
vii. If [PSbit] - [RBbit] is a positive value greater than 4 then set most significant Read Only bit [RObit] to ([PSbit] + 11), otherwise set [RObit] to ([RBbit] + 15). (This is used to check that the resulting VF BAR size always respects the current system page size setting.)
viii. If the Type field, of the VF BAR location indicated by the value returned in the VF BAR Index field in the VF Resizable BAR Control register [nBAR], is 00b (32 bit VF BAR), then read back that 32 bit VF BAR location and verify that bits [RObit] to 4 return 0. If not, then the test fails and testing continues with the next resizable VF BAR. (This tests that VF BAR bits that are changed from RW to RO are automatically cleared to 0 by the hardware.)
ix. If the Type field, of the VF BAR location indicated by the value returned in the VF BAR Index field in the VF Resizable BAR Control register [nBAR], is 10b (64 bit VF BAR), then read back that 64 bit VF BAR location (VF BAR Index returns the address of the lower 32 bits of the VF BAR) and verify that bits [RObit] to 4 return 0. If not, then the test fails and testing continues with the next resizable VF BAR. (This tests that VF BAR bits that are changed from RW to RO are automatically cleared to 0 by the hardware.)
x. If the Type field, of the VF BAR location indicated by the value returned in the VF BAR Index field in the VF Resizable BAR Control register [nBAR], is 00b (32 bit VF BAR), then write FFFF FFFFh to that 32 bit VF BAR location. Read back the same 32 bit VF BAR location and verify that bits 31 to ([RObit] + 1) return 1, and that bits [RObit] to 4 return 0. If not, then the test fails and testing continues with the next resizable VF BAR.
xi. If the Type field, of the VF BAR location indicated by the value returned in the VF BAR Index field in the VF Resizable BAR Control register [nBAR], is 10b (64 bit VF BAR), then write FFFF FFFF FFFF FFFFh to that 64 bit VF BAR location (VF BAR Index returns the address of the lower 32 bits of the VF BAR). Read back the same 64 bit VF BAR location and verify that bits 63 to ([RObit] + 1) return 1, and that bits [RObit] to 4 return 0. If not, then the test fails and testing continues with the next resizable VF BAR.
xii. Increment [RBbit] by 1. Increment [RBSize] by 1.
xiii. If [RBbit] is less than [RBbitmax], then repeat steps v to xiii. If [RBbit] is equal to [RBbitmax], go to the next step.

22. Increment [nBAR] by 1. If the new value of [nBAR] is less than or equal to [RBMax], then repeat steps 20-21. Otherwise go to the next step.
23. Increment [PSbit] by 1. If the new value of [PSbit] is greater than 31, then skip to step 28.
24. Read a DWORD from offset 1Ch (Supported Page Sizes register).
25. If bit [PSbit] in the Supported Page Sizes register returns 0, then repeat step 23.
26. If bit [PSbit] in the Supported Page Sizes register returns 1, then write a DWORD to the System Page Size register with bit [PSbit] set to 1, and all bits other than [PSbit] set to 0.
27. Repeat steps 20-22.
28. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.

b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

29. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one VF Resizable BAR Extended Capability structure is present.
- ❑ A VF contains a VF Resizable BAR Extended Capability structure.
- ❑ An RCRB contains a VF Resizable BAR Extended Capability structure.
- ❑ A function that is not a PF contains a VF Resizable BAR Extended Capability structure.
- ❑ The Capability Version field does not report 1h.
- ❑ The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- ❑ The Number of VF Resizable BARs field in the VF Resizable BAR Control register 0 returns a reserved value.
- ❑ Any of the register field characteristic tests fail.
- ❑ Any of the default value tests fail.
- ❑ Any implemented VF Resizable BAR Capability register returns a zero value.
- ❑ Any implemented VF Resizable BAR Control register returns a reserved value in the VF BAR Index field.
- ❑ Any implemented VF Resizable BAR Control register returns a non-memory VF BAR value in the VF BAR Index field.
- ❑ Any implemented VF Resizable BAR Control register returns a 32 bit memory VF BAR value in the VF BAR Index field, but the corresponding VF Resizable BAR Capability register returns a value indicating support for 4 GB or greater VF BAR size.
- ❑ Any implemented VF Resizable BAR Control register returns a 32 bit memory VF BAR value in the VF BAR Index field, but the corresponding VF Resizable BAR Control register bits 31-16 returns a value indicating support for 256 TB or greater VF BAR size (for Base 3.1 or later testing only).
- ❑ Any implemented VF Resizable BAR Control register does not allow valid values to be written to the VF BAR Size field.
- ❑ Any implemented VF Resizable BAR Control register does not force the corresponding VF BAR bits to be cleared to 0, when writing a value to the VF BAR Size field that will make the VF BAR bits change from RW to RO.
- ❑ Any implemented VF Resizable BAR Control register does not force the corresponding VF BAR bits to become RO, when writing a value to the VF BAR Size field that will make the VF BAR bits change from RW to RO.

- Any implemented resizable VF BAR returns a size that does not respect the current System Page Size setting.

2.2.51. TD_1_46 Multicast Extended Capability Structure

The test verifies that if the function under test reports a Multicast (MC) Extended Capability structure, it is implemented as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *ECN Multicast (to Base 2.0)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Test software writes 0 to both the Memory Space Enable field and the Bus Master Enable field in the Command register (this disables responses to memory cycles targeting the function's BAR spaces and prevents the function from generating any requests).
3. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0012h (Multicast Extended Capability) are found. If more than one is found, the test terminates with a failure.
4. For Base 1.x testing: if the Extended Capability ID of 0012h is found in an Extended Capability structure, the test terminates with a failure.
5. For Base 2.x or later testing: if the Extended Capability ID of 0012h is found in an Extended Capability structure for a device type that is a PCI Express to PCI/PCI-X Bridge or a PCI/PCI-X to PCI Express Bridge, the test terminates with failure.
6. For Base 2.x or later testing: if this is a Root Complex Integrated Endpoint, then the following tests are performed:
 a. If the Extended Capability ID of 0012h is not found in an Extended Capability structure, the test logs a warning, but the test continues.
7. For Base 2.x or later testing: if the Extended Capability ID of 0012h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0012h is not found in an Extended Capability structure, the test skips to step 15.

8. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
9. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
10. A WORD is read from offset 04h (Multicast Capability register).
11. Set the MC Groups Maximum [MCGMax] to the value read from the MC_Max_Group field (Multicast Capability register).
12. For Root Ports and Switch Ports only: if the MC_ECRC_Regeneration_Supported field returns 1, then the function must support an Advanced Error Reporting Extended Capability and the function must have the ECRC Check Capable field (Advanced Error Capabilities and Control register) return 1. If not, this is recorded as a failure, but the test continues.
13. The following register field characteristic checks are performed:

Multicast Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

Multicast Capability Register (Offset 04h) — WORD

a. MC_Max_Group	
(for VFs)	RO-Zero
(otherwise)	RO
b. RsvdP_7-6	RO-Zero
c. MC_Window_Size_Requested	
(for VFs)	RO-Zero
(for non-Root Ports, and non-Switch Ports excluding VFs)	RO
(for Root Ports and Switch Ports)	RO-Zero
d. RsvdP_14	RO-Zero
e. MC_ECRC_Regeneration_Supported	
(for VFs, non-Root Ports, and non-Switch Ports)	RO-Zero
(for Root Ports and Switch Ports)	RO

Multicast Control Register (Offset 06h) — WORD

a. MC_Num_Group	
(for VFs)	RO-Zero
(otherwise)	RW
b. RsvdP_14-6	RO-Zero
c. MC_Enable	RW

Multicast Base Address Register (Offset 08h) — 2 DWORDS

a. MC_Index_Position	
(for VFs)	RO-Zero
(otherwise)	RW
b. RsvdP_11-6	RO-Zero
c. MC_Base_Address	
(for VFs)	RO-Zero
(otherwise)	RW

MC_Receive Register (Offset 10h) — 2 DWORDS

a. (bits [MCGMax] to 0)	RW
b. (if [MCGMax] is less than 63: bits 63 to [MCGMax] + 1)	RO-Zero

MC_Block_All Register (Offset 18h) — 2 DWORDS

a. (bits [MCGMax] to 0)	RW
b. (if [MCGMax] is less than 63: bits 63 to [MCGMax] + 1)	RO-Zero

MC_Block_Untranslated Register (Offset 20h) — 2 DWORDS

a. (bits [MCGMax] to 0)	
(for Root Ports and Switch Ports)	RW
(for Endpoint with ATS Extended Capability)	RW
(for Endpoint without ATS Extended Capability)	RW or RO-Zero
b. (if [MCGMax] is less than 63: bits 63 to [MCGMax] + 1)	RO-Zero

MC_Overlay_BAR Register (Offset 28h) — 2 DWORDS

(for Root Ports or Switch Ports)

a. MC_Overlay_Size	RW
b. MC_Overlay_BAR	RW

14. The following default value checks are performed:

Multicast Control Register Default Value (Offset 06h) — WORD

a. MC_Num_Group	00 0000b
b. MC_Enable	0

Multicast Base Address Register Default Value (Offset 08h) — 2 DWORDS

a. MC_Index_Position	00 0000b
b. MC_Base_Address	0

MC_Receive Register Default Value (Offset 10h) — 2 DWORDS

a. (Bits 0 to MC_Max_Group)	0

MC_Block_All Register Default Value (Offset 18h) — 2 DWORDS

a. (Bits 0 to MC_Max_Group)	0

MC_Block_Untranslated Register Default Value (Offset 20h) — 2 DWORDS

a. (Bits 0 to MC_Max_Group)	0

MC_Overlay_BAR Register Default Value (Offset 28h) — 2 DWORDS

(for Root Ports or Switch Ports)

a. MC_Overlay_Size	00 0000b
b. MC_Overlay_BAR	0

15. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
16. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is

itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- More than one Multicast Extended Capability structure is present.
- The Multicast Extended Capability structure is present in a PCI Express to PCI/PCI-X Bridge or a PCI/PCI-X to PCI Express Bridge.
- The Capability Version field does not report 1h.
- The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- The MC_ECRC_Regeneration_Supported field is 1, but the ECRC Check Capable field (Advanced Error Reporting Extended Capability structure) returns 0, or no Advanced Error Reporting Extended Capability structure is present.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

The test *warns* if:

- A Root Complex Integrated Endpoint and the Multicast Extended Capability structure is not present.

2.2.52. TD_1_47 LTR Extended Capability Structure

The test verifies that if the function under test reports a Latency Tolerance Reporting (LTR) Extended Capability structure, it is implemented as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *ECN Latency Tolerance Reporting (to Base 2.0)*
- *ECN Root Complex Integrated Endpoint & IOV Updates (to Base 3.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.

2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0018h (LTR Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. For Base 1.x testing: if the Extended Capability ID of 0018h is found in an Extended Capability structure, the test terminates with a failure.
4. For Base 2.x or later testing: if the Extended Capability ID of 0018h is found in an Extended Capability structure for a VF, the test terminates with a failure.
5. For Base 2.x or later testing: if the Extended Capability ID of 0018h is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
6. For Base 2.x or later testing: if the Extended Capability ID of 0018h is found in an Extended Capability structure for a device type that is not an Endpoint, not a Legacy Endpoint, not a Root Complex Integrated Endpoint, and not a Switch Upstream Port, the test terminates with failure.
7. For Base 2.x or later testing: if the Extended Capability ID of 0018h is found in an Extended Capability structure for a function associated with an upstream port and the function is not function 0, the test terminates with failure.
8. For Base 2.x or later testing: if the Extended Capability ID of 0018h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0018h is not found in an Extended Capability structure, the test skips to step 13.
9. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
10. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
11. The following register field characteristic checks are performed:

LTR Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

Max Snoop Latency Register (Offset 04h) — WORD

a. Max Snoop LatencyValue	RW
b. Max Snoop LatencyScale Note: This test only writes permitted values of 000b to 101b.	RW
c. RsvdP_15-13	RO-Zero

Max No-Snoop Latency Register (Offset 06h) — WORD

a. Max No-Snoop LatencyValue	RW
b. Max No-Snoop LatencyScale Note: This test only writes permitted values of 000b to 101b.	RW
c. RsvdP_15-13	RO-Zero

12. The following default value checks are performed:

Max Snoop Latency Register Default Value (Offset 04h) — WORD

a. Max Snoop LatencyValue	0
b. Max Snoop LatencyScale	000b

Max No-Snoop Latency Register Default Value (Offset 06h) — WORD

a. Max No-Snoop LatencyValue 0
b. Max No-Snoop LatencyScale 000b

13. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
14. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one LTR Extended Capability structure is present.
- ❑ A VF contains a LTR Extended Capability structure.
- ❑ An RCRB contains a LTR Extended Capability structure.
- ❑ The LTR Extended Capability structure is present in any function other than the following: Endpoint; Legacy Endpoint; Root Complex Integrated Endpoint; Switch Upstream Port.
- ❑ For a multi-function device associated with an upstream port, the LTR Extended Capability structure is present in a function other than function 0.
- ❑ The Capability Version field does not report 1h.
- ❑ The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- ❑ Any of the register field characteristic tests fail.
- ❑ Any of the default value tests fail.

2.2.53. TD_1_48 TPH Requester Extended Capability Structure

The test verifies that if the function under test reports a TLP Processing Hints (TPH) Requester Extended Capability structure, it is implemented as defined in the relevant specifications.

Relevant Specifications

- ❑ *PCI Express Base Specification*
- ❑ *ECN TLP Processing Hints (to Base 2.0)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Test software writes 0 to the Bus Master Enable field in the Command register (this prevents the function from generating any requests).
3. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0017h (TPH Requester Extended Capability) are found. If more than one is found, the test terminates with a failure.
4. If the Extended Capability ID of 0017h is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
5. For Base 1.x testing: if the Extended Capability ID of 0017h is found in an Extended Capability structure, the test terminates with a failure.
6. For Base 2.x or later testing: if the Extended Capability ID of 0017h is found in an Extended Capability structure for a device type that is a PCI Express to PCI/PCI-X Bridge or a PCI/PCI-X to PCI Express Bridge, the test terminates with failure.
7. For Base 2.x or later testing: if the Extended Capability ID of 0017h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0017h is not found in an Extended Capability structure, the test skips to step 14.
8. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
9. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
10. Test software reads a DWORD from offset 04h (TPH Requester Capability register) and performs the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The No ST Mode Supported field must be 1.
 b. If the Interrupt Vector Mode Supported field reports 1, then the ST Table Location field must be 01b or 10b.
 c. If both the Interrupt Vector Mode Supported field and the Device Mode Supported field report 0, then the ST Table Location field must be 00b.
 d. The ST Table Location field must report a valid value (00b, 01b, 10b).
 e. If the ST Table Location field reports 01b, then the ST Table Size field must be less than 64 (000 0100 0000b).
 f. If the ST Table Location field reports 10b, then the function must implement a MSI-X Capability structure.
11. The following register field characteristic checks are performed:

TPH Requester Extended Capability Header (Offset 00h) — DWORD

a.	PCI Express Extended Capability ID	RO
b.	Capability Version	RO
c.	Next Capability Offset	RO

TPH Requester Capability Register (Offset 04h) — DWORD

a.	No ST Mode Supported	RO
b.	Interrupt Vector Mode Supported	RO
c.	Device Specific Mode Supported	RO
d.	RsvdP_7-3	RO-Zero
e.	Extended TPH Requester Supported	RO
f.	ST Table Location	RO
g.	RsvdP_15-11	RO-Zero
h.	ST Table Size	RO
i.	RsvdP_31-27	RO-Zero

TPH Requester Control Register (Offset 08h) — DWORD

a.	ST Mode Select	
	(if both Interrupt Vector Mode Supported and Device Specific Mode Supported are 0)	RO-Zero
	(if either Interrupt Vector Mode Supported or Device Specific Mode supported are non-zero)	RW
b.	RsvdP_7-3	RO-Zero
c.	TPH Requester Enable	
	(bit 0)	RW
	(bit 1)	
	(if Extended TPH Requester Supported is 1)	RW
	(if Extended TPH Requester Supported is 0)	RW or RO-Zero
d.	RsvdP_31-10	RO-Zero

12. The following default value checks are performed:

TPH Requester Control Register Default Value (Offset 08h) — DWORD

a.	ST Mode Select	000b
b.	TPH Requester Enable	
	(bit 0)	0b
	(bit 1)	0b

13. If ST Table Location is 01b, the following is performed:
 a. Set the ST Table Size [STS] to the value in the ST Table Size field.
 b. Every TPH ST Table Entry is a WORD, with the lower 16 bits of the read DWORD as the lower entry.
 c. Test software reads DWORDs starting from offset 0Ch (TPH ST Table) until the DWORD that contains the last TPH ST Table Entry is read.
 d. For each TPH ST Table Entry register set instance Number [n] (from 0 to [STS]), the following register field characteristic checks are performed:

ST Table Entries Registers (n) (Offset 0Ch + 2 * n) — WORD

a.	ST Lower	RW
b.	ST Upper	

(if Extended TPH Requester Supported is 1)	RW
(if Extended TPH Requester Supported is 0)	RO-Zero

e. For each TPH ST Table Entry register set instance Number [n] (from 0 to [STS]), the following default value checks are performed:

ST Table Entries Registers (n) Default Value (Offset 0Ch + 2 * n) — WORD

a. ST Lower	00h
b. ST Upper	00h

f. If [STS] is an even number, then the upper 16 bits of the last read DWORD (Offset 0Ch + 2 * [STS]) must be RO-Zero.

14. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
15. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one TPH Requester Extended Capability structure is present.
- ❑ An RCRB contains a TPH Requester Extended Capability structure.
- ❑ The TPH Extended Capability structure is present in a PCI Express to PCI/PCI-X Bridge or a PCI/PCI-X to PCI Express Bridge.
- ❑ The Capability Version field does not report 1h.
- ❑ The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- ❑ The function does not report the No ST Mode Supported field as 1.
- ❑ The function reports the Interrupt Vector Mode Supported field as 1, but does not report that ST Table Location is in the TPH Requester Extended Capability structure or in the MSI-X Table.
- ❑ The function reports the ST Table Location as in either the MSI-X Table or the TPH Requester Extended Capability structure, but does not report either the Interrupt Vector Mode Supported field as 1 or the Device Specific Mode Supported field as 1.
- ❑ The function reports an invalid ST Table Location field value.
- ❑ The function reports the ST Table Location as in the TPH Requester Extended Capability structure, but reports an invalid ST Table Size field (greater than 64 ST Table Entries).
- ❑ The function reports the ST Table Location as in the MSI-X Table, but does not implement a MSI-X Capability structure.
- ❑ Any of the register field characteristic tests fail.

- Any of the default value tests fail.

2.2.54. TD_1_54 ATS Extended Capability Structure

The test verifies that if the function under test reports an Address Translation Services (ATS) Extended Capability structure, it is implemented as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *Address Translation Services Revision 1.1 (Base 3.x or earlier only)*
- *Single Root I/O Virtualization and Sharing Specification (Base 3.x or earlier only)*
- *ECN PASID Translation (to ATS 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Test software writes 0 to the Bus Master Enable field in the Command register (this prevents the function from generating any requests).
3. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 000Fh (ATS Extended Capability) are found. If more than one is found, the test terminates with a failure.
4. If the Extended Capability ID of 000Fh is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
5. For Base 4.0 or later testing: if the Extended Capability ID of 000Fh is found in an Extended Capability structure for a device type that is not an Endpoint, not a Legacy Endpoint, and not a Root Complex Integrated Endpoint, then the test terminates with a failure.
6. If the Extended Capability ID of 000Fh is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 000Fh is not found in an Extended Capability structure, the test skips to step 12.
7. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
8. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.

9. A WORD is read from offset 04h in the ATS Extended Capability structure (ATS Capability register)
 a. The Page Aligned Request field should return 1. If it does not a warning message is issued, but this is not treated in itself as a failure.

10. The following register field characteristic checks are performed:

ATS Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

ATS Capability Register (Offset 04h) — WORD

a. Invalidate Queue Depth	
(for VFs)	RO-Zero
(otherwise)	RO
b. Page Aligned Request	RO
c. RsvdZ_15-6	
(For Base 2.x or earlier testing)	RO-Zero
d. Global Invalidate Supported	
(For Base 3.x or later testing)	
(if PASID Extended Capability is supported)	RO
(otherwise)	RO-Zero
e. RsvdP_15-7	
(For Base 3.x or later testing)	RO-Zero

ATS Control Register (Offset 06h) — WORD

a. Smallest Translation Unit (STU)	
(for VFs)	RO-Zero
(otherwise)	RW
b. RsvdP_14-5	RO-Zero
c. Enable	RW

11. The following default value checks are performed:

ATS Control Register Default Value (Offset 06h) — WORD

a. Smallest Translation Unit (STU)	0 0000b
b. Enable	0

12. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

13. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one ATS Extended Capability structure is present.

- An RCRB contains an ATS Extended Capability structure.
- The ATS Extended Capability structure is in any function other than the following: Endpoint; Legacy Endpoint; Root Complex Integrated Endpoint (for Base 4.0 or later testing only).
- The Capability Version field does not report 1h.
- The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

The test *warns* if:

- The Page Aligned Request field is not set.

2.2.55. TD_1_55 Page Request Extended Capability Structure

The test verifies that if the function under test reports a Page Request Extended Capability structure, it is implemented as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *Address Translation Services Revision 1.1 (Base 3.x or earlier only)*
- *ECN PASID Translation (to ATS 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Test software writes 0 to the Bus Master Enable field in the Command register (this prevents the function from generating any requests).
3. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0013h (Page Request Extended Capability) are found. If more than one is found, the test terminates with a failure.

4. If the Extended Capability ID of 0013h is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
5. If the Extended Capability ID of 0013h is found in an Extended Capability structure for a device type that is not an Endpoint, not a Legacy Endpoint, and not a Root Complex Integrated Endpoint, then the test terminates with a failure.
6. If the Extended Capability ID of 0013h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0013h is not found in an Extended Capability structure, the test skips to step 11.
7. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
8. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
9. The following register field characteristic checks are performed:

Page Request Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

Page Request Control Register (Offset 04h) — WORD

a. Enable	RW
b. Reset	RO-Zero
c. RsvdP_15-2	RO-Zero

Page Request Status Register (Offset 06h) — WORD

a. Response Failure	RW1C
b. Unexpected Page Request Group Index	RW1C
c. RsvdZ_7-2	RO-Zero
d. Stopped (The Enable field must be written with 0 before this field is tested.)	RO
e. RsvdZ_15-9 (For Base 2.x or earlier testing)	RO-Zero
f. RsvdZ_14-9 (For Base 3.x or later testing)	RO-Zero
g. PRG Response PASID Required (For Base 3.x or later testing) (if PASID Extended Capability is supported) (otherwise)	 RO RO-Zero

Outstanding Page Request Capacity Register (Offset 08h) — DWORD

(all bits) RO

Outstanding Page Request Allocation Register (Offset 0Ch) — DWORD

(all bits) RW

(The Enable field must be written with 0 before this register is tested. Only values up to the value returned in the Outstanding Page Request Capacity register can be written.)

10. The following default value checks are performed:

 Page Request Control Register Default Value (Offset 04h) — WORD

 a. Enable 0

 Page Request Status Register Default Value (Offset 06h) — WORD

 a. Response Failure 0
 b. Unexpected Page Request Group Index 0
 c. Stopped 1

 Outstanding Page Request Allocation Register Default Value (Offset 0Ch) — DWORD

 (This register defaults to 0000 0000h.)

11. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
12. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one Page Request Extended Capability structure is present.
- ❑ An RCRB contains a Page Request Extended Capability structure.
- ❑ The Page Request Extended Capability structure is present in any function other than the following: Endpoint; Legacy Endpoint; Root Complex Integrated Endpoint.
- ❑ The Capability Version field does not report 1h.
- ❑ The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- ❑ Any of the register field characteristic tests fail.
- ❑ Any of the default value tests fail.

2.2.56. TD_1_56 SR-IOV Extended Capability Structure

The test verifies that if the function under test reports a SR-IOV Extended Capability structure, it is implemented as defined in the relevant specifications.

Relevant Specifications

- ❑ *PCI Express Base Specification*
- ❑ *Single Root I/O Virtualization and Sharing Specification (Base 3.x or earlier only)*
- ❑ *ECN Root Complex Integrated Endpoint & IOV Updates (to SRIOV 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0010h (SR-IOV Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Extended Capability ID of 0010h is found in an Extended Capability structure for a VF, the test terminates with a failure.
4. If the Extended Capability ID of 0010h is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
5. If the Extended Capability ID of 0010h is found in an Extended Capability structure for a device type that is not an Endpoint, not a Legacy Endpoint, and not a Root Complex Integrated Endpoint, then the test terminates with a failure.
6. If the Extended Capability ID of 0010h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0010h is not found in an Extended Capability structure, the test skips to step 21.
7. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
8. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
9. Test software reads a DWORD from offset 04h (SR-IOV Capabilities register) and performs the following checks:
 a. For all device types (except Root Complex Integrated Endpoints), in the lowest numbered PF in the device, if the function implements a PCI Power Management Capability structure, and the No_Soft_Reset field (Power Management Control/Status register) is 1, the ARI Capable Hierarchy Preserved field should return 1. If it does not, a warning message is issued, but this is not treated in itself as a failure.
 b. For device type of Root Complex Integrated Endpoint, the ARI Capable Hierarchy Preserved field should return 0. If it does not, a warning message is issued, but this is not treated in itself as a failure.
 c. For Base 4.x or later testing: if the function under test reports the 10-Bit Tag Requester Supported field (Device Capabilities 2 register) as 0, the VF 10-Bit Tag Requester Supported field must return 0. If not, this is recorded as a failure, but the test continues.

10. Test software reads a WORD from offset 0Ch (InitialVFs register) and also reads a WORD from offset 0Eh (TotalVFs register) and performs the following checks:
 a. The InitialVFs register value must be less than or equal to the TotalVFs register value. If not, this is recorded as a failure, but the test continues.
11. For Base 3.x or later testing: test software reads a WORD from offset 10h (NumVFs register) and if it returns a non-zero value, the following checks are performed:
 a. Test software reads a WORD from offset 14h (First VF Offset register) and if a value of 0000h is returned a failure is recorded, but the test continues.
12. Test software reads a DWORD from offset 1Ch (Supported Page Sizes register) and performs the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The Supported Page Sizes register value must have at least all the following bits return 1: (bit 10; bit 8; bit 6; bit 4; bit 1; bit 0).
13. For the DWORD from offset 20h (System Page Size register) test software performs the following checks:
 a. Test software writes the VF Enable field to 0.
 b. Set the value of Page Size bit [PSbit] to 0.
 c. If bit [PSbit] in the Supported Page Sizes register returns 1, then write a DWORD to the System Page Size register with bit [PSbit] set to 1, and all bits other than [PSbit] set to 0.
 d. If bit [PSbit] in the Supported Page Sizes register returns 1, read back the DWORD from the System Page Size and verify that bit [PSbit] returns 1 and all bits other than [PSbit] return 0. If not, a failure is recorded, but the test continues.
 e. Increment [PSbit] by 1 and repeat steps c-e for all values of [PSbit] up to and including 31.
14. Starting at offset 24h the next 6 DWORDs are read. These are the VF BAR0 to VF BAR5 registers. (Some VF BAR registers may occupy 2 DWORDs if they are 64 bit VF BARs.)
 a. Each VF BAR n must have bit 0 = 0 (Memory Space BAR). If not, this is recorded as a failure and testing continues with the next VF BAR.
 b. Offset 38h (VF BAR 5) must not have both bit 0 = 0 (Memory Space BAR) and the Type field = 10b (64 bit addressing). If not, this is recorded as a failure, but the test continues.
15. Test software writes the VF MSE field to 0 (to disable all VF memory space).
16. For each VF BAR test software writes FFFF FFFFh to the VF BAR and then reads back the same register. If it returns 0000 0000h, then this is an empty VF BAR. Empty VF BARs are excluded from further testing.
17. For each non-empty VF BAR that has bit 0 = 0 (Memory Space BAR):
 a. Test software writes the VF Enable field to 0.
 b. Set value [PSbit] to 0.
 c. If bit [PSbit] in the Supported Page Sizes register returns 0, then skip to step m.
 d. If bit [PSbit] in the Supported Page Sizes register returns 1, then write a DWORD to the System Page Size register with bit [PSbit] set to 1, and all bits other than [PSbit] set to 0.
 e. Test software writes FFFF FFFFh to the VF BAR and then reads back the same register. Bits 6-4 must be 0 (MEMORY BAR size must be 128 Bytes or larger). If not, this is recorded as a failure and the test skips to step m.
 f. If the Type field returns 00b, then starting at bit 4 determine the least significant bit value that is set to 1 and record it in Least Significant Bit [LSB]. [LSB] must be less than or equal

to 31. If not, this is recorded as a failure and test skips to step m. All bits from 31 to [LSB] must also be 1. If not, this is recorded as a failure and the test skips to step m. This same [LSB] value is used in subsequent tests of this same VF BAR.

g. If the Type field returns 10b, test software writes FFFF FFFFh to the immediate next higher Configuration Space location (this is the upper half of a 64 bit VF BAR) then starting at bit 4 of the lower 32 bit VF BAR determine the least significant bit value that is set to 1 and record it in Least Significant Bit [LSB]. [LSB] must be less than or equal to 63. If not, this is recorded as a failure and the test skips to step m. All bits from 63 to [LSB] must also be 1. If not, this is recorded as a failure and the test skips to step m.
h. [LSB] must be equal or greater than ([PSbit] + 12) (VF BAR must be aligned to the current System Page Size boundary setting). If not, this is recorded as a failure and the test skips to step m.
i. Test software writes 5555 5555h (for 32 bit VF BAR) or 5555 5555 5555 5555h (for 64 bit VF BAR) to the VF BAR and then reads back the same register. Bits 31-[LSB] (for 32 bit VF BAR) or Bits 63-[LSB] (for 64 bit VF BAR) must return the written value. If not, this is recorded as a failure and the test skips to step m. Bits [LSB]-4 must return all 0. If not, this is recorded as a failure and the test skips to step m.
j. Test software writes AAAA AAAAh (for 32 bit VF BAR) or AAAA AAAA AAAA AAAAh (for 64 bit VF BAR) to the VF BAR and then reads back the same register. Bits 31-[LSB] (for 32 bit VF BAR) or Bits 63-[LSB] (for 64 bit VF BAR) must return the written value. If not, this is recorded as a failure and the test skips to step m. Bits [LSB]-4 must return all 0. If not, this is recorded as a failure and the test skips to step m.
k. Test software writes CCCC CCCCh (for 32 bit VF BAR) or CCCC CCCC CCCC CCCCh (for 64 bit VF BAR) to the VF BAR and then reads back the same register. Bits 31-[LSB] (for 32 bit VF BAR) or Bits 63-[LSB] (for 64 bit VF BAR) must return the written value. If not, this is recorded as a failure and the test skips to step m. Bits [LSB]-4 must return all 0. If not, this is recorded as a failure and the test skips to step m.
l. Test software writes 0000 0000h (for 32 bit VF BAR) or 0000 0000 0000 0000h (for 64 bit VF BAR) to the VF BAR and then reads back the same register. Bits 31-[LSB] (for 32 bit VF BAR) or Bits 63-[LSB] (for 64 bit VF BAR) must return the written value. If not, this is recorded as a failure and the test skips to step m. Bits [LSB]-4 must return all 0. If not, this is recorded as a failure and the test skips to step m.
m. Increment [PSbit] by 1 and repeat steps c-m for all values of [PSbit] up to and including 31.

18. If the TotalVFs register returns a value greater than 0 and the VF Migration Capable field (SR-IOV Capabilities register) returns 1, test software reads a DWORD from offset 3Ch (VF Migration State Array Offset register) and performs the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The VF Migration State BIR field must return one of the following values: 000b to 101b.
 b. The BAR pointed to by VF Migration State BIR field value is read and bit 0 of that BAR must be 0 (Memory BAR).

19. The following register field characteristic checks are performed:

SR-IOV Extended Capability Header (Offset 00h) –– DWORD

a.	PCI Express Extended Capability ID	RO
b.	Capability Version	RO
c.	Next Capability Offset	RO

SR-IOV Capabilities Register (Offset 04h) — DWORD

a. VF Migration Capable — RO

b. ARI Capable Hierarchy Preserved
(For Base 2.x or later testing)
(for RC Integrated Endpoints) — RO
(for all except for RC Integrated Endpoints, lowest numbered PF in the device) — RO
(for all except for RC Integrated Endpoints, all other PFs in the device) — RO-Zero

c. VF 10-Bit Tag Requester Supported
(for Base 4.x or later testing) — HwInit

d. RsvdP_20-3
(For Base 4.x or later testing) — RO-Zero

e. RsvdP_20-2
(For Base 2.x or Base 3.x testing) — RO-Zero

f. RsvdP_20-1
(For Base 1.x testing) — RO-Zero

g. VF Migration Interrupt Message Number — RO

SR-IOV Control Register (Offset 08h) — WORD

a. VF Enable — RW

b. VF Migration Enable
(if VF Migration Capable is 1 and VF Enable is written with 0) — RW
(if VF Migration Capable is 1 and VF Enable is written with 1) — RO
(if VF Migration Capable is 0) — RO-Zero
(The VF Enable field must be written with 0 before this field is tested as RW. When the VF Enable field is written with 1, the field will become RO.)

c. VF Migration Interrupt Enable
(For Base 1.x testing) — RW
(For Base 2.x or later testing: if VF Migration Capable is 1) — RW
(For Base 2.x or later testing: if VF Migration Capable is 0) — RW or RO

d. VF MSE — RW

e. ARI Capable Hierarchy
(for RC Integrated Endpoints) — RO-Zero
(for all except for RC Integrated Endpoints, lowest numbered PF in the device)
(for non-FLR testing) — RW
(for FLR testing) — RWS
(for all except for RC Integrated Endpoints, all other PFs in the device) — RO-Zero
(For the lowest numbered PF in the device, the test must restore this field to its previous value when the test completes.)

f. VF 10-Bit Tag Requester Enable
(For Base 4.x or later testing)
(with VF 10-Bit Tag Requester Supported as 1) — RW
(with VF 10-Bit Tag Requester Supported as 0) — RW or RO-Zero

g. RsvdP_15-6
(For Base 4.x or later testing) — RO-Zero

h. RsvdP_15-5

(For Base 3.x or earlier testing) RO-Zero

SR-IOV Status Register (Offset 0Ah) — WORD

a. VF Migration Status RW1C
b. RsvdZ_15-1 RO-Zero

InitialVFs Register (Offset 0Ch) — WORD RO

TotalVFs Register (Offset 0Eh) — WORD RO

NumVFs Register (Offset 10h) — WORD RW

(The VF Enable field must be written with 0 before this register is tested. Only values up to the value returned in the TotalVFs register can be written.)

Function Dependency Link Register (Offset 12h) — BYTE RO

Reserved Register (Offset 13h) — BYTE

a. RsvdP_7-0 RO-Zero

First VF Offset Register (Offset 14h) — WORD RO

VF Stride Register (Offset 16h) — WORD RO

Reserved Register (Offset 18h) — WORD

a. RsvdP_15-0 RO-Zero

VF Device ID Register (Offset 1Ah) — WORD RO

Supported Page Sizes Register (Offset 1Ch) — DWORD

(all bits) RO

VF BAR (n) (lower 32) Register (Offset 24h + n * 04h) — DWORD

(for non-empty VF BARs)

a. bit 0 RO-Zero
b. Type RO
c. Prefetchable RO

Values of [n] between 0 and 5 are to be tested. If Type field of VF BAR (n) is 10b (64 bit addressing), then increment [n] by 2, otherwise increment [n] by 1.

VF Migration State Array Offset Register (Offset 3Ch) — DWORD

a. VF Migration State BIR
 (if TotalVFs is greater than 0 and VF Migration Capable is 1) RO
 (if VF Migration Capable is 0) RO-Zero
b. VF Migration State Offset
 (if TotalVFs is greater than 0 and VF Migration Capable is 1) RO
 (if VF Migration Capable is 0) RO-Zero

VF Migration State Array ([table] + [n-1]) — BYTE

(only if TotalVFs is greater than 0 and VF Migration Capable is 1)

a. VF Migration State RW
b. RsvdP_7-2 RO-Zero

(The NumVFs register must be written with the value returned by the TotalVFs register, and then the VF Enable field must be written with 1 before this register is tested.)

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by VF Migration State BIR field) plus the offset (value in the VF Migration State Offset field multiplied by 8). All values of [n-1] between 0 and the value in the NumVFs field minus 1 must be tested.

20. The following default value checks are performed:

SR-IOV Control Register Default Value (Offset 08h) — WORD

a. VF Enable	0
b. VF Migration Enable	0
c. VF Migration Interrupt Enable	0
d. VF MSE	0
e. ARI Capable Hierarchy	0
f. VF 10-Bit Tag Requester Enable (For Base 4.x or later testing)	0

SR-IOV Status Register Default Value (Offset 0Ah) — WORD

a. VF Migration Status	0

System Page Size Register Default Value (Offset 20h) — DWORD

(This register defaults to 0000 0001h.)

VF Migration State Array Default Value ([table] + [n-1]) — BYTE

(only if TotalVFs is greater than 0 and VF Migration Capable is 1)

a. VF Migration State	
(for [n-1] less than or equal to InitialVFs value minus 1)	11b
(for [n-1] greater than InitialVFs value minus 1)	00b

(After returning the function to its default state test software must wait 1 second, then it must write the NumVFs register with the value returned by the TotalVFs register, and then it must write the VF Enable field with 1 before this array is read.)

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the VF Migration State BIR field value) plus the offset (value in the VF Migration State Offset field multiplied by 8). All values of [n-1] between 0 and the value in the NumVFs field minus 1 must be tested.

21. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
22. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one SR-IOV Extended Capability structure is present.
- ❑ A VF contains a SR-IOV Extended Capability structure.

- An RCRB contains a SR-IOV Extended Capability structure.
- The SR-IOV Extended Capability structure is present in any function other than the following: Endpoint; Legacy Endpoint; Root Complex Integrated Endpoint.
- The Capability Version field does not report 1h.
- The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- The VF 10-Bit Tag Requester Supported field is set when the 10-Bit Tag Requester Supported field is clear (for Base 4.x or later testing only).
- The InitialVFs register is greater than the TotalVFs register.
- The First VF Offset register is 0000h when the NumVFs register is greater than zero (for Base 3.x or later testing only).
- The Supported Page Sizes register does not have one of the following bits set: (bit 10; bit 8; bit 6; bit 4; bit 1; bit 0).
- The System Page Size register does not have all bits writeable that correspond to bits that return 1 in the Supported Page Sizes register.
- A VF BAR claims less than 128 Bytes of memory space.
- A VF BAR is not aligned to the current System Page Size boundary setting.
- A VF BAR does not return contiguous 1's across all implemented address bits.
- A VF BAR does not implement RW bits across all implemented address bits.
- The VF Migration State BIR field returns a reserved value, when the TotalVFs register is greater than 0 and the VF Migration Capable field is 1.
- The VF Migration State BIR field value points to an I/O Space BAR, when the TotalVFs register is greater than 0 and the VF Migration Capable field is 1.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

The test *warns* if:

- A device type other than a Root Complex Integrated Endpoint which is the lowest numbered PF in the device, the No_Soft_Reset field is set and the ARI Capable Hierarchy Preserved field is not set.
- A Root Complex Integrated Endpoint, which is a PF, the ARI Capable Hierarchy Preserved field is set.

2.2.57. TD_1_57 MR-IOV Extended Capability Structure

The test verifies that if the function under test reports a MR-IOV Extended Capability structure, it is implemented as defined in the relevant specifications.

Only a brief sub-set of MR-IOV testing will be implemented in the compliance test suite at this time.

Note: A comprehensive test description is provided in Section A.1 in Appendix A, for informational purposes only.

Relevant Specifications

- *Multi-Root I/O Virtualization and Sharing Specification Revision 1.0*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0011h (MR-IOV Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Extended Capability ID of 0011h is found in an Extended Capability structure for a VF, the test terminates with a failure.
4. If the Extended Capability ID of 0011h is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
5. If the Extended Capability ID of 0011h is found in an Extended Capability structure, the device type must be PCI Express Endpoint, Legacy Endpoint, Root Complex Integrated Endpoint, Switch Upstream Port, or Switch Downstream Port. If not, the test terminates with a failure.
6. If the Extended Capability ID of 0011h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0011h is not found in an Extended Capability structure, the test skips to step 9.
7. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
8. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
9. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
10. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is

itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- More than one MR-IOV Extended Capability structure is present.
- A VF contains a MR-IOV Extended Capability structure.
- An RCRB contains a MR-IOV Extended Capability structure.
- The MR-IOV Extended Capability structure is present in any function other than the following: Endpoint; Legacy Endpoint; Root Complex Integrated Endpoint; Switch Upstream Port; Switch Downstream Port.
- The Capability Version field does not report 1h.
- The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- The MR-IOV Extended Capability structure is present in a VF.

2.2.58. TD_1_58 Secondary PCI Express Extended Capability Structure

The test verifies that if the function under test reports a Secondary PCI Express Extended Capability structure, it is implemented as defined in the relevant specifications.

The test will only run for Base 3.x or later testing.

Relevant Specifications

- *PCI Express Base Specification*
- *ECN Separate Refclk Independent SSC Architecture (SRIS) (to Base 3.0)*
- *ECN SR-IOV Table Updates (to SR-IOV 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0019h (Secondary

PCI Express Extended Capability) are found. If more than one is found, the test terminates with a failure.

3. For Base 2.x or earlier testing: if the Extended Capability ID of 0019h is found in an Extended Capability structure, the test terminates with a failure.
4. For Base 3.x or later testing: if the Extended Capability ID of 0019h is found in an Extended Capability structure for a VF, the test terminates with a failure.
5. For Base 3.x or later testing: if this is an RCRB, then the following tests are performed:
 a. If the RCRB does not contains a Root Complex Internal Link Control Extended Capability structure (Extended Capability ID of 0006h), then if the Extended Capability ID of 0019h is found in an Extended Capability structure, the test terminates with a failure.
 b. If the RCRB contains a Root Complex Internal Link Control Extended Capability structure (Extended Capability ID of 0006h) then:
 i. If the RCRB under test reports the Max Link Speed field (Root Complex Link Capabilities register) of 0011b or greater or the Supported Link Speeds Vector field (Root Complex Link Capabilities register) of 000 0100b or greater, then if the Extended Capability ID of 0019h is not found for an Extended Capability structure, the test terminates with a failure.
6. For Base 3.x or later testing: if this is not an RCRB, then the following tests are performed:
 a. If the device type is a Root Complex Integrated Endpoint or a Root Complex Event Collector, then if the Extended Capability ID of 0019h is found in an Extended Capability structure, the test terminates with a failure.
 b. If the device type is neither a Root Complex Integrated Endpoint nor a Root Complex Event Collector, and if the function under test is associated with an Upstream Port and is not function 0, then if the Extended Capability ID of 0019h is found in an Extended Capability structure, the test terminates with a failure.
 c. If the device type is neither a Root Complex Integrated Endpoint nor a Root Complex Event Collector, and if the function under test is associated with an Upstream Port and is function 0, or if the function under test is associated with a Downstream Port, then:
 i. If the function under test reports the Max Link Speed field (Link Capabilities register) of 0011b or greater, then if the Extended Capability ID of 0019h is not found for an Extended Capability structure, the test terminates with a failure.
 ii. If the function under test reports the Capability Version field (PCI Express Capabilities register) is 2h or greater:
 a. If the function under test reports the Supported Link Speeds Vector field (Link Capabilities 2 register) of 000 0100b or greater, then if the Extended Capability ID of 0019h is not found for an Extended Capability structure, the test terminates with a failure.
 b. If the function under test reports the Lower SKP OS Generation Supported Speeds Vector field (Link Capabilities 2 register) of 000 0001b or greater, then if the Extended Capability ID of 0019h is not found for an Extended Capability structure, the test terminates with a failure.
7. For Base 3.x or later testing: if the Extended Capability ID of 0019h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0019h is not found in an Extended Capability structure, the test skips to step 13.

8. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
9. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
10. The following register field characteristic checks are performed:

Secondary PCI Express Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID — RO
b. Capability Version — RO
c. Next Capability Offset — RO

Link Control 3 Register (Offset 04h) — DWORD

a. Perform Equalization
 (for Upstream Ports with Crosslink Supported as 0) — RO-Zero
 (for Upstream Ports with Crosslink Supported as 1 and Max Link Speed/Supported Link Speeds is 0011b or greater) — RW
 (for Upstream Ports with Crosslink Supported as 1 and Max Link Speed/Supported Link Speeds is less than 0011b) — RW or RO-Zero
 (for Downstream Ports with Max Link Speed/Supported Link Speeds is 0011b or greater) — RW
 (for Downstream Ports with Max Link Speed/Supported Link Speeds is less than 0011b) — RW or RO-Zero
 Note: This test must not write 1 to the Retrain Link field (Link Control register), when this field is 1. Also, the test must restore this field to 0 when the test completes.
b. Link Equalization Request Interrupt Enable
 (for Upstream Ports with Crosslink Supported as 0) — RO-Zero
 (for Upstream Ports with Crosslink Supported as 1 and Max Link Speed/Supported Link Speeds is 0011b or greater) — RW
 (for Upstream Ports with Crosslink Supported as 1 and Max Link Speed/Supported Link Speeds is less than 0011b) — RW or RO-Zero
 (for Downstream Ports and Max Link Speed/Supported Link Speeds is 0011b or greater) — RW
 (for Downstream Ports with Max Link Speed/Supported Link Speeds is less than 0011b) — RW or RO-Zero
c. RsvdP_8-2 — RO-Zero
d. Enable Lower SKP OS Generation Vector
 (if Lower SKP OS Generation Supported Speeds Vector (bit 0) is 1: bit 0) — RW
 (if Lower SKP OS Generation Supported Speeds Vector (bit 0) is 0: bit 0) — RW or RO-Zero
 (if Lower SKP OS Generation Supported Speeds Vector (bit 1) is 1: bit 1) — RW
 (if Lower SKP OS Generation Supported Speeds Vector (bit 1) is 0: bit 1) — RW or RO-Zero
 (if Lower SKP OS Generation Supported Speeds Vector (bit 2) is 1: bit 2) — RW

(if Lower SKP OS Generation Supported Speeds Vector (bit 2) is 0: bit 2) RW or RO-Zero
(For Base 4.x or later testing:
if Lower SKP OS Generation Supported Speeds Vector (bit 3) is 1: bit 3) RW
(For Base 4.x or later testing:
if Lower SKP OS Generation Supported Speeds Vector (bit 3) is 0: bit 3) RW or RO-Zero
(For Base 4.x or later testing: bits 6-4) RO-Zero
(For Base 3.x testing: (bits 6-3) RO-Zero

e. RsvdP_31-16 RO-Zero

Lane Error Status Register (Offset 08h) — DWORD

a. (bits [Maximum Link Width-1] - 0)
(if Max Link Speed/Supported Link Speeds is 0011b or greater) RW1CS
(if Max Link Speed/Supported Link Speeds is less than 0011b) RW1CS or RO-Zero

b. (if [Maximum Link Width] is less than 32:
bits 31 - [Maximum Link Width]) RO-Zero

11. The following default value checks are performed:

Link Control 3 Register Default Value (Offset 04h) — DWORD

a. Perform Equalization
(for all except Upstream Ports with Crosslink Supported as 0) 0
Note: This test must not write 1 to the Retrain Link field (Link Control register), when this field is 1.

b. Link Equalization Request Interrupt Enable
(for all except Upstream Ports with Crosslink Supported as 0) 0

c. Enable Lower SKP OS Generation Vector 000 0000b

12. For each Lane Equalization Control Entry register set instance Number [n] (from 0 to the value in Maximum Link Width - 1), the following register field characteristic checks are performed:

Lane Equalization Control Entry Register (n) (Offset 0Ch + n * 02h) – WORD

a. Downstream Port 8.0 GT/s Transmitter Preset
(for Upstream Ports with Crosslink Supported as 0) RO-Zero
(for Upstream Ports with Crosslink Supported as 1)
(for non-FLR testing) HwInit
(for FLR testing) RO
(for Downstream Ports) HwInit

b. Downstream Port 8.0 GT/s Receiver Preset Hint
(for Upstream Ports with Crosslink Supported as 0) RO-Zero
(for Upstream Ports with Crosslink Supported as 1)
(for non-FLR testing) HwInit
(for FLR testing) RO
(for Downstream Ports) HwInit

c. RsvdP_7 RO-Zero

d. Upstream Port 8.0 GT/s Transmitter Preset
(for Upstream Ports with Crosslink Supported as 0) RO
(for Upstream Ports with Crosslink Supported as 1)

(for non-FLR testing)	HwInit
(for FLR testing)	RO
(for Downstream Ports)	HwInit

e. Upstream Port 8.0 GT/s Receiver Preset Hint

(for Upstream Ports with Crosslink Supported as 0)	RO
(for Upstream Ports with Crosslink Supported as 1)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
(for Downstream Ports)	HwInit

f. RsvdP_15 RO-Zero

13. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
14. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one Secondary PCI Express Extended Capability structure is present.
- ❑ A VF contains a Secondary PCI Express Extended Capability structure.
- ❑ An RCRB that does not correspond to a Root Complex Internal Link and the Secondary PCI Express Extended Capability structure is present.
- ❑ An RCRB that corresponds to a Root Complex Internal Link and that supports 8.0 GT/s or greater, and the Secondary PCI Express Extended Capability structure is not present.
- ❑ A Root Complex Integrated Endpoint or a Root Complex Event Collector, and the Secondary PCI Express Extended Capability structure is present.
- ❑ An upstream port function other than 0, and the Secondary PCI Express Extended Capability structure is present.
- ❑ A device type that supports 8.0 GT/s or greater, and the Secondary PCI Express Extended Capability structure is not present.
- ❑ A device type that reports a non-zero value in the Lower SKP OS Generation Supported Speeds Vector, and the Secondary PCI Express Extended Capability structure is not present.
- ❑ The Capability Version field does not report 1h.
- ❑ The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- ❑ Any of the register field characteristic tests fail.
- ❑ Any of the default value tests fail.

2.2.59. TD_1_59 Protocol Multiplexing Extended Capability Structure

The test verifies that if the function under test reports a Protocol Multiplexing Extended Capability structure, it is implemented as defined in the relevant specifications.

The test will only run for Base 3.x or later testing.

Relevant Specifications

- *PCI Express Base Specification*
- *ECN SR-IOV Table Updates (to SR-IOV 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 001Ah (Protocol Multiplexing Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. For Base 2.x or earlier testing: if the Extended Capability ID of 001Ah is found in an Extended Capability structure, the test terminates with a failure.
4. For Base 3.x or later testing: if the Extended Capability ID of 001Ah is found in an Extended Capability structure for a VF, the test terminates with a failure.
5. For Base 3.x or later testing: if the Extended Capability ID of 001Ah is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
6. For Base 3.x or later testing: if the Extended Capability ID of 001Ah is found in an Extended Capability structure for a device type that is a Root Complex Integrated Endpoint or a Root Complex Event Collector, the test terminates with a failure.
7. For Base 3.x or later testing: if the Extended Capability ID of 001Ah is found in an Extended Capability structure for a function associated with an upstream port and the function is not function 0, the test terminates with a failure.
8. For Base 3.x or later testing: if the Extended Capability ID of 001Ah is found in an Extended Capability structure, the following tests are performed:

a. If the Capability Version field (PCI Express Capabilities register) is 1h or less (Link Capabilities 2 register is not supported), the test terminates with a failure.

9. For Base 3.x or later testing: if the Extended Capability ID of 001Ah is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 001Ah is not found in an Extended Capability structure, the test skips to step 16.
10. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
11. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
12. A DWORD is read from offset 04h (PMUX Capability register) and the following checks are performed:
 a. For Base 3.x testing: the PMUX Supported Link Speeds field must be 0000 0001b, 0000 0010b, 0000 0011b, 0000 0100b, 0000 0101b, 0000 0110b, or 0000 0111b. All other encodings are reserved and are recorded as a failure, but the test continues.
 b. For Base 4.x testing: the PMUX Supported Link Speeds field must be 000 0001b, 000 0010b, 000 0011b, 000 0100b, 000 0101b, 000 0110b, 000 0111b, 000 1000b, 000 1001b, 000 1010b, 000 1011b, 000 1100b, 000 1101b, 000 1110b, or 000 1111b. All other encodings are reserved and are recorded as a failure, but the test continues.
 c. If the Supported Link Speeds Vector field (Link Capabilities 2 register) bit 0 (2.5 GT/s) returns 0, then the PMUX Supported Link Speeds field (PMUX Capability register) bit 0 (2.5 GT/s) must be 0. If not, this is recorded as a failure, but the test continues.
 d. If the Supported Link Speeds Vector field (Link Capabilities 2 register) bit 1 (5.0 GT/s) returns 0, then the PMUX Supported Link Speeds field (PMUX Capability register) bit 1 (5.0 GT/s) must be 0. If not, this is recorded as a failure, but the test continues.
 e. If the Supported Link Speeds Vector field (Link Capabilities 2 register) bit 2 (8.0 GT/s) returns 0, then the PMUX Supported Link Speeds field (PMUX Capability register) bit 2 (8.0 GT/s) must be 0. If not, this is recorded as a failure, but the test continues.
 f. For Base 4.x or later testing: if the Supported Link Speeds Vector field (Link Capabilities 2 register) bit 3 (16.0 GT/s) returns 0, then the PMUX Supported Link Speeds field (PMUX Capability register) bit 3 (16.0 GT/s) must be 0. If not, this is recorded as a failure, but the test continues.
13. The following register field characteristic checks are performed:

PMUX Extended Capability Header (Offset 00h) –– DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

PMUX Capability Register (Offset 04h) –– DWORD

a. PMUX Protocol Array Size	RO
b. RsvdP_7-6	RO-Zero
c. PMUX Supported Link Speeds	RO
d. RsvdP_31-16	RO-Zero

PMUX Control Register (Offset 08h) –– DWORD

a. PMUX Channel 0 Assignment

(for PMUX Protocol Array Size equal to 0)
(bits 5-0) RW or RO-Zero

(for PMUX Protocol Array Size equal to 1)
(bit 0) RW
(bits 5-1) RW or RO-Zero

(for PMUX Protocol Array Size equal to or between 3 and 2)
(bits 1-0) RW
(bits 5-2) RW or RO-Zero

(for PMUX Protocol Array Size equal to or between 7 and 4)
(bits 2-0) RW
(bits 5-3) RW or RO-Zero

(for PMUX Protocol Array Size equal to or between 15 and 8)
(bits 3-0) RW
(bits 5-4) RW or RO-Zero

(for PMUX Protocol Array Size equal to or between 31 and 16)
(bits 4-0) RW
(bit 5) RW or RO-Zero

(for PMUX Protocol Array Size greater than 31)
(bits 5-0) RW

b. RsvdP_7-6 RO-Zero

c. PMUX Channel 1 Assignment
(for PMUX Protocol Array Size equal to 0)
(bits 5-0) RW or RO-Zero

(for PMUX Protocol Array Size equal to 1)
(bit 0) RW
(bits 5-1) RW or RO-Zero

(for PMUX Protocol Array Size equal to or between 3 and 2)
(bits 1-0) RW
(bits 5-2) RW or RO-Zero

(for PMUX Protocol Array Size equal to or between 7 and 4)
(bits 2-0) RW
(bits 5-3) RW or RO-Zero

(for PMUX Protocol Array Size equal to or between 15 and 8)
(bits 3-0) RW
(bits 5-4) RW or RO-Zero

(for PMUX Protocol Array Size equal to or between 31 and 16)
(bits 4-0) RW

(bit 5) RW or RO-Zero

(for PMUX Protocol Array Size greater than 31)
(bits 5-0) RW

d. RsvdP_15-14 RO-Zero

e. PMUX Channel 2 Assignment
(for PMUX Protocol Array Size equal to 0)
(bits 5-0) RW or RO-Zero

(for PMUX Protocol Array Size equal to 1)
(bit 0) RW
(bits 5-1) RW or RO-Zero

(for PMUX Protocol Array Size equal to or between 3 and 2)
(bits 1-0) RW
(bits 5-2) RW or RO-Zero

(for PMUX Protocol Array Size equal to or between 7 and 4)
(bits 2-0) RW
(bits 5-3) RW or RO-Zero

(for PMUX Protocol Array Size equal to or between 15 and 8)
(bits 3-0) RW
(bits 5-4) RW or RO-Zero

(for PMUX Protocol Array Size equal to or between 31 and 16)
(bits 4-0) RW
(bit 5) RW or RO-Zero

(for PMUX Protocol Array Size greater than 31)
(bits 5-0) RW

f. RsvdP_23-22 RO-Zero

g. PMUX Channel 3 Assignment
(for PMUX Protocol Array Size equal to 0)
(bits 5-0) RW or RO-Zero

(for PMUX Protocol Array Size equal to 1)
(bit 0) RW
(bits 5-1) RW or RO-Zero

(for PMUX Protocol Array Size equal to or between 3 and 2)
(bits 1-0) RW
(bits 5-2) RW or RO-Zero

(for PMUX Protocol Array Size equal to or between 7 and 4)
(bits 2-0) RW

(bits 5-3)	RW or RO-Zero
(for PMUX Protocol Array Size equal to or between 15 and 8)	
(bits 3-0)	RW
(bits 5-4)	RW or RO-Zero
(for PMUX Protocol Array Size equal to or between 31 and 16)	
(bits 4-0)	RW
(bit 5)	RW or RO-Zero
(for PMUX Protocol Array Size greater than 31)	
(bits 5-0)	RW
h. RsvdP_31-30	RO-Zero

PMUX Status Register (Offset 0Ch) — DWORD

a. PMUX Channel 0 Disabled: Link Speed	RO
b. PMUX Channel 0 Disabled: Link Width	RO
c. PMUX Channel 0 Disabled: Protocol Specific	RO
d. RsvdZ_7-3	RO-Zero
e. PMUX Channel 1 Disabled: Link Speed	RO
f. PMUX Channel 1 Disabled: Link Width	RO
g. PMUX Channel 1 Disabled: Protocol Specific	RO
h. RsvdZ_15-11	RO-Zero
i. PMUX Channel 2 Disabled: Link Speed	RO
j. PMUX Channel 2 Disabled: Link Width	RO
k. PMUX Channel 2 Disabled: Protocol Specific	RO
l. RsvdZ_23-19	RO-Zero
m. PMUX Channel 3 Disabled: Link Speed	RO
n. PMUX Channel 3 Disabled: Link Width	RO
o. PMUX Channel 3 Disabled: Protocol Specific	RO
p. RsvdZ_ 31-27	RO-Zero

14. The following default value checks are performed:

PMUX Control Register Default Value (Offset 08h) — DWORD

a. PMUX Channel 0 Assignment	00 0000b
b. PMUX Channel 1 Assignment	00 0000b
c. PMUX Channel 2 Assignment	00 0000b
d. PMUX Channel 3 Assignment	00 0000b

PMUX Status Register Default Value (Offset 0Ch) — DWORD

a. PMUX Channel 0 Disabled: Link Speed	0
b. PMUX Channel 0 Disabled: Link Width	0
c. PMUX Channel 0 Disabled: Protocol Specific	0
d. PMUX Channel 1 Disabled: Link Speed	0
e. PMUX Channel 1 Disabled: Link Width	0
f. PMUX Channel 1 Disabled: Protocol Specific	0
g. PMUX Channel 2 Disabled: Link Speed	0
h. PMUX Channel 2 Disabled: Link Width	0
i. PMUX Channel 2 Disabled: Protocol Specific	0

j. PMUX Channel 3 Disabled: Link Speed 0
k. PMUX Channel 3 Disabled: Link Width 0
l. PMUX Channel 3 Disabled: Protocol Specific 0

Note: PMUX Status bits for a channel must all return 0 when that channel's Control assignment bit is 0. Also, each channels Control assignment bit is required to default to 0.

15. If the PMUX Protocol Array Size field is non-zero, then for each PMUX Protocol Array Entry register set instance Number [n] (from 1 to the value in PMUX Protocol Array Size), the following register field characteristic checks are performed:

PMUX Protocol Array Entry (n) (Offset 10h + n * 04h) – DWORD

a. Protocol ID RO
b. Authority ID RO

16. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
17. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- More than one Protocol Multiplexing Extended Capability structure is present.
- A VF contains a Protocol Multiplexing Extended Capability structure.
- An RCRB contains a Protocol Multiplexing Extended Capability structure.
- A Root Complex Integrated Endpoint or a Root Complex Event Collector, and the Protocol Multiplexing Extended Capability structure is present.
- An upstream port function other than 0, and the Protocol Multiplexing Extended Capability structure is present.
- The Capability Version field of the PCI Express Capability register is less than 2h, and the Protocol Multiplexing Extended Capability structure is present.
- The Capability Version field does not report 1h.
- The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- The PMUX Supported Link Speeds field is not one of the defined values.
- The PMUX Supported Link Speeds field reports support for a link speed that is not supported in the value reported in the Supported Link Speeds Vector field.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

2.2.60. TD_1_60 PASID Extended Capability Structure

The test verifies that if the function under test reports a Process Address Space ID (PASID) Extended Capability structure, it is implemented as defined in the relevant specifications.

The test will only run for Base 3.x or later testing.

Relevant Specifications

- *PCI Express Base Specification*
- *ECN Process Address Space ID (PASID) (to Base 3.0)*
- *ECN Root Complex Integrated Endpoint & IOV Updates (to Base 3.1)*
- *ECN SR-IOV Table Updates (to SR-IOV 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 001Bh (PASID Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. For Base 2.x or earlier testing: if the Extended Capability ID of 001Bh is found in an Extended Capability structure, the test terminates with a failure.
4. For Base 3.x or later testing: if the Extended Capability ID of 001Bh is found in an Extended Capability structure for a VF, the test terminates with a failure.
5. For Base 3.x or later testing: if the Extended Capability ID of 001Bh is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
6. For Base 3.x or later testing: if the Extended Capability ID of 001Bh is found in an Extended Capability structure for a device type that is not an Endpoint, not a Legacy Endpoint, and not a Root Complex Integrated Endpoint, the test terminates with a failure.
7. For Base 3.x or later testing: if the Extended Capability ID of 001Bh is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 001Bh is not found in an Extended Capability structure, the test skips to step 13.
8. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.

9. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
10. A WORD is read from offset 04h (PASID Capability register) and the following checks are performed:
 a. The Max PASID Width field must be 20 or less. All other encodings are reserved and are recorded as a failure, but the test continues.
 b. For Base 3.1 or later testing: the Max PASID Width field should be 20. If not, then a warning message is issued, but this is not treated in itself as a failure.
11. The following register field characteristic checks are performed:

PASID Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

PASID Capability Register (Offset 04h) — WORD

a. RsvdP_0	RO-Zero
b. Execute Permission Supported	RO
c. Privileged Mode Supported	RO
d. RsvdP_7-3	RO-Zero
e. Max PASID Width	RO
f. RsvdP_15-13	RO-Zero

PASID Control Register (Offset 06h) — WORD

a. PASID Enable	RW
b. Execute Permission Enable	
(if Execute Permission Supported is 1)	RW
(if Execute Permission Supported is 0)	RO-Zero
c. Privileged Mode Enable	
(if Privileged Mode Supported is 1)	RW
(if Privileged Mode Supported is 0)	RO-Zero
d. RsvdP_15-3	RO-Zero

12. The following default value checks are performed:

PASID Control Register Default Value (Offset 06h) — WORD

a. PASID Enable	0
b. Execute Permission Enable	0
c. Privileged Mode Enable	0

13. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
14. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- More than one PASID Extended Capability structure is present.
- A VF contains a PASID Extended Capability structure.
- An RCRB contains a PASID Extended Capability structure.
- The PASID Extended Capability structure is present in any function other than the following: Endpoint; Legacy Endpoint; Root Complex Integrated Endpoint.
- The Capability Version field does not report 1h.
- The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- The Max PASID Width field is not one of the defined values (0 to 20).
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

The test *warns* if:

- The Max PASID Width field is not 20.

2.2.61. TD_1_61 LNR Extended Capability Structure

The test verifies that if the function under test reports a LNR Extended Capability structure, it is implemented as defined in the relevant specifications.

The test will only run for Base 3.x or later testing.

Relevant Specifications

- *PCI Express Base Specification*
- *ECN Lightweight Notification (LN) Protocol (to Base 3.0)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 001Ch (LNR Extended Capability) are found. If more than one is found, the test terminates with a failure.

3. For Base 2.x or earlier testing: if the Extended Capability ID of 001Ch is found in an Extended Capability structure, the test terminates with a failure.
4. For Base 3.x or later testing: if the Extended Capability ID of 001Ch is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
5. For Base 3.x or later testing: if the Extended Capability ID of 001Ch is found in an Extended Capability structure for a device type that is not an Endpoint, not a Legacy Endpoint, and not a Root Complex Integrated Endpoint, the test terminates with a failure.
6. For Base 3.x or later testing: if the Extended Capability ID of 001Ch is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 001Ch is not found in an Extended Capability structure, the test skips to step 12.
7. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
8. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
9. A WORD is read from offset 04h (LNR Capability register) and the following checks are performed:
 a. At least one of the LNR-64 Supported field or the LNR-128 Supported field must be 1. If both fields are 0, then this is recorded as a failure, but the test continues.
10. The following register field characteristic checks are performed:

LNR Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

LNR Capability Register (Offset 04h) — WORD

a. LNR-64 Supported	RO
b. LNR-128 Supported	RO
c. RsvdP_7-2	RO-Zero
d. LNR Registration Max	RO
e. RsvdP_15-13	RO-Zero

LNR Control Register (Offset 06h) — WORD

a. LNR Enable	RW
b. LNR CLS	
(if both LNR-64 Supported is 1 and LNR-128 Supported is 1)	RW
(otherwise)	RW or RO
c. RsvdP_7-2	RO-Zero
d. LNR Registration Limit	RW
e. RsvdP_15-13	RO-Zero

11. The following default value checks are performed:

LNR Control Register Default Value (Offset 06h) — WORD

a. LNR Enable	0
b. LNR CLS	

(if LNR CLS is RW) 0
c. LNR Registration Limit 11111b

12. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
13. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one LNR Extended Capability structure is present.
- ❑ An RCRB contains a LNR Extended Capability structure.
- ❑ The LNR Extended Capability structure is present in any function other than the following: Endpoint; Legacy Endpoint; Root Complex Integrated Endpoint.
- ❑ The Capability Version field does not report 1h.
- ❑ The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- ❑ Neither LNR-64 Supported field nor LNR-128 Supported field reports 1.
- ❑ Any of the register field characteristic tests fail.
- ❑ Any of the default value tests fail.

2.2.62. TD_1_62 DPC Extended Capability Structure

The test verifies that if the function under test reports a DPC Extended Capability structure, it is implemented as defined in the relevant specifications.

The test will only run for Base 3.x or later testing.

Relevant Specifications

- ❑ *PCI Express Base Specification*
- ❑ *ECN Downstream Port Containment (DPC) (to Base 3.0)*
- ❑ *ECN Enhanced DPC (eDPC) (to Base 3.0)*
- ❑ *ECN SR-IOV Table Updates (to SR-IOV 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 001Dh (DPC Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. For Base 2.x or earlier testing: if the Extended Capability ID of 001Dh is found in an Extended Capability structure, the test terminates with a failure.
4. For Base 3.x or later testing: if the Extended Capability ID of 001Dh is found in an Extended Capability structure for a VF, the test terminates with a failure.
5. For Base 3.x or later testing: if the Extended Capability ID of 001Dh is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
6. For Base 3.x or later testing: if the Extended Capability ID of 001Dh is found in an Extended Capability structure for a device type that is neither a Root Port nor a Switch Downstream Port, the test terminates with a failure.
7. For Base 3.x or later testing: if the Extended Capability ID of 001Dh is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 001Dh is not found in an Extended Capability structure, the test skips to step 13.
8. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
9. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
10. A WORD is read from offset 04h (DPC Capability register) and the following checks are performed:
 a. If the RP Extensions for DPC field returns 1, then the RP PIO Log Size field must be greater than or equal to 4. If not, this is recorded as a failure, but the test continues.
 b. If the RP Extensions for DPC field returns 1, then the RP PIO Log Size field must be less than or equal to (5 + p), where p is the value returned in the Max End-End TLP Prefixes field (Device Capabilities 2 register). If not, this is recorded as a failure, but the test continues.
11. The following register field characteristic checks are performed:

DPC Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

DPC Capability Register (Offset 04h) — WORD

a. DPC Interrupt Message Number	RO
b. RP Extensions for DPC	
(for Root Ports)	RO
(for Switch Downstream Ports)	RO-Zero
c. Poisoned TLP Egress Blocking Supported	
(for Root Ports with RP Extensions for DPC as 1)	RO-Ones
(for Root Ports with RP Extensions for DPC as 0 and Switch Downstream Ports)	RO
d. DPC Software Triggering Supported	
(for Root Ports with RP Extensions for DPC as 1)	RO-Ones
(for Root Ports with RP Extensions for DPC as 0 and Switch Downstream Ports)	RO
e. RP PIO Log Size	
(for Root Ports with RP Extensions for DPC as 1)	RO
(for Root Ports with RP Extensions for DPC as 0 and Switch Downstream Ports)	RO-Zero
f. DL_Active ERR_COR Signaling Supported	
(for Root Ports with RP Extensions for DPC as 1)	RO-Ones
(for Root Ports with RP Extensions for DPC as 0 and Switch Downstream Ports)	RO
g. RsvdP_15-13	RO-Zero

DPC Control Register (Offset 06h) — WORD

a. DPC Trigger Enable	RW
b. DPC Completion Control	RW
c. DPC Interrupt Enable	RW
d. DPC ERR_COR Enable	RW
e. Poisoned TLP Egress Blocking Enable	
(if Poisoned TLP Egress Blocking Supported is 1)	RW
(if Poisoned TLP Egress Blocking Supported is 0)	RW or RO-Zero
f. DPC Software Trigger	RO-Zero

Note: The DPC Trigger Enable field must be written with 0 before this field is tested, otherwise writing the DPC Software Trigger field will cause the port to transition to DPC state (DL_Down) if supported (the DPC Software Triggering Supported field returns 1). The DPC Software Trigger field always returns 0 when read.

g. DL_Active ERR_COR Enable	
(if DL_Active ERR_COR Signaling Supported is 1)	RW
(if DL_Active ERR_COR Signaling Supported is 0)	RW or RO-Zero
h. RsvdP_15-8	RO-Zero

DPC Status Register (Offset 08h) — WORD

a. DPC Trigger Status	RW1CS
b. DPC Trigger Reason	ROS
c. DPC Interrupt Status	RW1CS
d. DPC RP Busy	
(for Root Ports with RP Extensions for DPC as 1)	RO

(for Root Ports with RP Extensions for DPC as 0 and Switch Downstream Ports)	RO-Zero
e. DPC Trigger Reason Extension	ROS
f. RsvdZ_7	RO-Zero
g. RP PIO First Error Pointer (for Root Ports with RP Extensions for DPC as 1)	ROS
(for Root Ports with RP Extensions for DPC as 0 and Switch Downstream Ports)	RO-Zero
h. RsvdZ_15-13	RO-Zero

DPC Error Source ID Register (Offset 0Ah) — WORD

a. DPC Error Source ID	ROS

RP PIO Status Register (Offset 0Ch) — DWORD

(only for Root Ports with RP Extensions for DPC as 1)

a. Cfg UR Cpl	RW1CS
b. Cfg CA Cpl	RW1CS
c. Cfg CTO	RW1CS
d. RsvdZ_7-3	RO-Zero
e. I/O UR Cpl	RW1CS
f. I/O CA Cpl	RW1CS
g. I/O CTO	RW1CS
h. RsvdZ_15-11	RO-Zero
i. Mem UR Cpl	RW1CS
j. Mem CA Cpl	RW1CS
k. Mem CTO	RW1CS
l. RsvdZ_31-19	RO-Zero

RP PIO Mask Register (Offset 10h) — DWORD

(only for Root Ports with RP Extensions for DPC as 1)

a. Cfg UR Cpl	RWS
b. Cfg CA Cpl	RWS
c. Cfg CTO	RWS
d. RsvdP_7-3	RO-Zero
e. I/O UR Cpl	RWS
f. I/O CA Cpl	RWS
g. I/O CTO	RWS
h. RsvdP_15-11	RO-Zero
i. Mem UR Cpl	RWS
j. Mem CA Cpl	RWS
k. Mem CTO	RWS
l. RsvdP_31-19	RO-Zero

RP PIO Severity Register (Offset 14h) — DWORD

(only for Root Ports with RP Extensions for DPC as 1)

a. Cfg UR Cpl	RWS
b. Cfg CA Cpl	RWS
c. Cfg CTO	RWS
d. RsvdP_7-3	RO-Zero
e. I/O UR Cpl	RWS

f. I/O CA Cpl	RWS
g. I/O CTO	RWS
h. RsvdP_15-11	RO-Zero
i. Mem UR Cpl	RWS
j. Mem CA Cpl	RWS
k. Mem CTO	RWS
l. RsvdP_31-19	RO-Zero

RP PIO SysError Register (Offset 18h) — DWORD

(only for Root Ports with RP Extensions for DPC as 1)

a. Cfg UR Cpl	RWS
b. Cfg CA Cpl	RWS
c. Cfg CTO	RWS
d. RsvdP_7-3	RO-Zero
e. I/O UR Cpl	RWS
f. I/O CA Cpl	RWS
g. I/O CTO	RWS
h. RsvdP_15-11	RO-Zero
i. Mem UR Cpl	RWS
j. Mem CA Cpl	RWS
k. Mem CTO	RWS
l. RsvdP_31-19	RO-Zero

RP PIO Exception Register (Offset 1Ch) — DWORD

(only for Root Ports with RP Extensions for DPC as 1)

a. Cfg UR Cpl	RWS
b. Cfg CA Cpl	RWS
c. Cfg CTO	RWS
d. RsvdP_7-3	RO-Zero
e. I/O UR Cpl	RWS
f. I/O CA Cpl	RWS
g. I/O CTO	RWS
h. RsvdP_15-11	RO-Zero
i. Mem UR Cpl	RWS
j. Mem CA Cpl	RWS
k. Mem CTO	RWS
l. RsvdP_31-19	RO-Zero

RP PIO Header Log Register (Offset 20h) — 4 DWORDS

(only for Root Ports with RP Extensions for DPC as 1 and RP PIO Log Size greater than 3)

a. Header Log register (1st DW)	ROS
b. Header Log register (2nd DW)	ROS
c. Header Log register (3rd DW)	ROS
d. Header Log register (4th DW)	ROS

RP PIO ImpSpec Log Register (Offset 30h) — DWORD

(only for Root Ports with RP Extensions for DPC as 1 and RP PIO Log Size greater than 4)

a. RP PIO ImpSpec Log register	ROS

RP PIO TLP Prefix Log Register (Offset 34h) – DWORD

(only for Root Ports with RP Extensions for DPC as 1 and RP PIO Log Size greater than 5)

a. First TLP Prefix Log register ROS

RP PIO TLP Prefix Log Register (Offset 38h) — DWORD
(only for Root Ports with RP Extensions for DPC as 1 and RP PIO Log Size greater than 6)
a. Second TLP Prefix Log register ROS

RP PIO TLP Prefix Log Register (Offset 3Ch) — DWORD
(only for Root Ports with RP Extensions for DPC as 1 and RP PIO Log Size greater than 7)
a. Third TLP Prefix Log register ROS

RP PIO TLP Prefix Log Register (Offset 40h) — DWORD
(only for Root Ports with RP Extensions for DPC as 1 and RP PIO Log Size greater than 8)
a. Fourth TLP Prefix Log register ROS

12. The following default value checks are performed:

DPC Control Register Default Value (Offset 04h) — WORD
a. DPC Trigger Enable 00b
b. DPC Completion Control 0
c. DPC Interrupt Enable 0
d. DPC ERR_COR Enable 0
e. Poisoned TLP Egress Blocking Enable 0
f. DL_Active ERR_COR Enable 0

DPC Status Register Default Value (Offset 08h) — WORD
a. DPC Trigger Status 0
b. DPC Interrupt Status 0

RP PIO Status Register Default Value (Offset 0Ch) — DWORD
(only for Root Ports with RP Extensions for DPC as 1)
a. Cfg UR Cpl 0
b. Cfg CA Cpl 0
c. Cfg CTO 0
d. I/O UR Cpl 0
e. I/O CA Cpl 0
f. I/O CTO 0
g. Mem UR Cpl 0
h. Mem CA Cpl 0
i. Mem CTO 0

RP PIO Mask Register Default Value (Offset 10h) — DWORD
(only for Root Ports with RP Extensions for DPC as 1)
a. Cfg UR Cpl 1
b. Cfg CA Cpl 1
c. Cfg CTO 1
d. I/O UR Cpl 1
e. I/O CA Cpl 1
f. I/O CTO 1
g. Mem UR Cpl 1
h. Mem CA Cpl 1
i. Mem CTO 1

RP PIO Severity Register Default Value (Offset 14h) — DWORD
(only for Root Ports with RP Extensions for DPC as 1)

a. Cfg UR Cpl	0
b. Cfg CA Cpl	0
c. Cfg CTO	0
d. I/O UR Cpl	0
e. I/O CA Cpl	0
f. I/O CTO	0
g. Mem UR Cpl	0
h. Mem CA Cpl	0
i. Mem CTO	0

RP PIO SysError Register Default Value (Offset 18h) — DWORD
(only for Root Ports with RP Extensions for DPC as 1)

a. Cfg UR Cpl	0
b. Cfg CA Cpl	0
c. Cfg CTO	0
d. I/O UR Cpl	0
e. I/O CA Cpl	0
f. I/O CTO	0
g. Mem UR Cpl	0
h. Mem CA Cpl	0
i. Mem CTO	0

RP PIO Exception Register Default Value (Offset 1Ch) — DWORD
(only for Root Ports with RP Extensions for DPC as 1)

a. Cfg UR Cpl	0
b. Cfg CA Cpl	0
c. Cfg CTO	0
d. I/O UR Cpl	0
e. I/O CA Cpl	0
f. I/O CTO	0
g. Mem UR Cpl	0
h. Mem CA Cpl	0
i. Mem CTO	0

13. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
14. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one DPC Extended Capability structure is present.

- A VF contains a DPC Extended Capability structure.
- An RCRB contains a DPC Extended Capability structure.
- The DPC Extended Capability structure is present in any function other than the following: Root Port; Switch Downstream Port.
- The Capability Version field does not report 1h.
- The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- The RP Extensions for DPC field reports 1, but the RP PIO Log Size field reports less than 4.
- The RP Extensions for DPC field reports 1, but the RP PIO Log Size field reports greater than the value in the Max End-End TLP Prefixes field plus 5.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

2.2.63. TD_1_63 L1 PM Substates Extended Capability Structure

The test verifies that if the function under test reports a L1 PM Substates Extended Capability structure, it is implemented as defined in the relevant specifications.

The test will only run for Base 3.x or later testing.

Relevant Specifications

- *PCI Express Base Specification*
- *ECN L1 PM Substates with CLKREQ (to Base 3.0)*
- *ECN SR-IOV Table Updates (to SR-IOV 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 001Eh (L1 PM Substates Extended Capability) are found. If more than one is found, the test terminates with a failure.

3. For Base 2.x or earlier testing: if the Extended Capability ID of 001Eh is found in an Extended Capability structure, the test terminates with a failure.
4. For Base 3.x or later testing: if the Extended Capability ID of 001Eh is found in an Extended Capability structure for a VF, the test terminates with a failure.
5. For Base 3.x or later testing: if the Extended Capability ID of 001Eh is found in an Extended Capability structure for a device type that is a Root Complex Integrated Endpoint or a Root Complex Event Collector, the test terminates with a failure.
6. For Base 3.x or later testing: if the Extended Capability ID of 001Eh is found in an Extended Capability structure for a function associated with an upstream port and the function is not function 0, the test terminates with a failure.
7. For Base 3.x or later testing: if the Extended Capability ID of 001Eh is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 001Eh is not found in an Extended Capability structure, the test skips to step 13.
8. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
9. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
10. A DWORD is read from offset 04h (L1 PM Substates Capabilities register) and the following checks are performed:
 a. The PCI-PM L1.1 Supported field must return 1. If not, this is recorded as a failure, but the test continues.
 b. The L1 PM Substates Supported field must return 1. If not, this is recorded as a failure, but the test continues.
 c. If the PCI-PM L1.2 Supported field is 1 or the ASPM_L1.2 Supported field is 1, then the Port T_POWER_ON Scale field must be a valid value (00b, 01b, 10b). All other encodings are reserved and are recorded as a failure, but the test continues.
11. The following register field characteristic checks are performed:

L1 PM Substates Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

L1 PM Substates Capabilities Register (Offset 04h) — DWORD

a. PCI-PM L1.2 Supported	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
b. PCI-PM L1.1 Supported	
(for non-FLR testing)	HwInit
(for FLR testing)	RO-Ones
c. ASPM L1.2 Supported	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
d. ASPM L1.1 Supported	

(for non-FLR testing)	HwInit
(for FLR testing)	RO
e. L1 PM Substates Supported	
(for non-FLR testing)	HwInit
(for FLR testing)	RO-Ones
f. RsvdP_7-5	RO-Zero
g. Port Common_Mode_Restore_Time	
(if PCI-PM L1.2 Supported is 0 and ASPM_L1.2 Supported is 0)	RO-Zero
(otherwise)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
h. Port T_POWER_ON Scale	
(if PCI-PM L1.2 Supported is 0 and ASPM_L1.2 Supported is 0)	RO-Zero
(otherwise)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
i. RsvdP_18	RO-Zero
j. Port T_POWER_ON Value	
(if PCI-PM L1.2 Supported is 0 and ASPM_L1.2 Supported is 0)	RO-Zero
(otherwise)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
k. RsvdP_31-24	RO-Zero

L1 PM Substates Control 1 Register (Offset 08h) –– DWORD

a. PCI-PM L1.2 Enable	
(if PCI-PM L1.2 Supported is 1)	RW
(if PCI-PM L1.2 Supported is 0)	RW or RO-Zero
b. PCI-PM L1.1 Enable	RW
c. ASPM L1.2 Enable	
(if ASPM L1.2 Supported is 1)	RW
(if ASPM L1.2 Supported is 0)	RW or RO-Zero
d. ASPM L1.1 Enable	
(if ASPM L1.1 Supported is 1)	RW
(if ASPM L1.1 Supported is 0)	RW or RO-Zero
e. RsvdP_7-4	RO-Zero
f. Common_Mode_Restore_Time	
(if PCI-PM L1.2 Supported is 0 and ASPM_L1.2 Supported is 0)	RO-Zero
(otherwise)	RW
g. LTR_L1.2_THRESHOLD Value	
(if ASPM_L1.2 Supported is 0)	RO-Zero
(otherwise)	RW
h. RsvdP_28-26	RO-Zero
i. LTR_L1.2_THRESHOLD Scale	
(if ASPM_L1.2 Supported is 0)	RO-Zero

(otherwise) RW
Note: This test only writes permitted values of 000b to 101b.

L1 PM Substates Control 2 Register (Offset 0Ch) — DWORD

a. T_POWER_ON Scale
(if PCI-PM L1.2 Supported is 0 and ASPM_L1.2 Supported is 0) RO-Zero
(otherwise) RW
b. RsvdP_2 RO-Zero
c. T_POWER_ON Value
(if PCI-PM L1.2 Supported is 0 and ASPM_L1.2 Supported is 0) RO-Zero
(otherwise) RW
d. RsvdP_31-8 RO-Zero

12. The following default value checks are performed:

L1 PM Substates Control 1 Register Default Value (Offset 08h) — DWORD

a. PCI-PM L1.2 Enable 0
b. PCI-PM L1.1 Enable 0
c. ASPM L1.2 Enable 0
d. ASPM L1.1 Enable 0
e. LTR_L1.2_THRESHOLD Value 0000000000b
f. LTR_L1.2_THRESHOLD Scale 000b

L1 PM Substates Control 2 Register Default Value (Offset 0Ch) — DWORD

a. T_POWER_ON Scale 0
b. T_POWER_ON Value 00101b

13. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
14. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one L1 PM Substates Extended Capability structure is present.
- ❑ A VF contains a L1 PM Substates Extended Capability structure.
- ❑ The L1 PM Substates Extended Capability structure is present in a Root Complex Integrated Endpoint or a Root Complex Event Collector.
- ❑ An upstream port function other than 0, and the L1 PM Substates Extended Capability structure is present.
- ❑ The Capability Version field does not report 1h.
- ❑ The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.

- The PCI-PM L1.1 Supported field does not report 1.
- The L1 PM Substates Supported field does not report 1.
- A reserved value is read from the Port T_POWER_ON Scale field.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

2.2.64. TD_1_64 PTM Extended Capability Structure

The test verifies that if the function under test reports a Precision Time Measurement (PTM) Extended Capability structure, it is implemented as defined in the relevant specifications.

The test will only run for Base 3.x or later testing.

Relevant Specifications

- *PCI Express Base Specification*
- *ECN Precision Time Measurement (PTM), Revision 1.0a (to Base 3.0)*
- *ECN SR-IOV Table Updates (to SR-IOV 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 001Fh (PTM Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. For Base 2.x or earlier testing: if the Extended Capability ID of 001Fh is found in an Extended Capability structure, the test terminates with a failure.
4. For Base 3.x or later testing: if the Extended Capability ID of 001Fh is found in an Extended Capability structure for a VF, the test terminates with a failure.
5. For Base 3.x or later testing: if the Extended Capability ID of 001Fh is found in an Extended Capability structure for a device type that is a Switch Downstream Port, a PCI Express to PCI/PCI-X Bridge, a PCI/PCI-X to PCI Express Bridge, or a Root Complex Event Collector, the test terminates with a failure.

6. For Base 3.x or later testing: if the Extended Capability ID of 001Fh is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 001Fh is not found in an Extended Capability structure, the test skips to step 12.
7. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
8. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
9. A DWORD is read from offset 04h (PTM Capability register) and the following checks are performed:
 a. If the PTM Root Capable field is 1, then the PTM Responder Capable field must return 1. If not, this is recorded as a failure, but the test continues.
 b. If the device type is a Switch Upstream Port, and if either the PTM Requester Capable field is 1 or the PTM Responder Capable field is 1, then both the PTM Requester Capable field and the PTM Responder Capable field must be 1. If not, this is recorded as a failure, but the test continues.
10. The following register field characteristic checks are performed:

PTM Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
b. Capability Version	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
c. Next Capability Offset	
(for non-FLR testing)	HwInit
(for FLR testing)	RO

PTM Capability Register (Offset 04h) — DWORD

a. PTM Requester Capable	
(for Root Ports and RCRBs)	RO-Zero
(otherwise)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
b. PTM Responder Capable	
(for PCI Express Endpoints, Legacy Endpoints, and Root Complex Integrated Endpoints)	RO-Zero
(otherwise)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO-Ones
c. PTM Root Capable	
(for PCI Express Endpoints, Legacy Endpoints, and Root Complex Integrated Endpoint)	RO-Zero
(for non-FLR testing)	HwInit
(for FLR testing)	RO
d. RsvdP_7-3	RO-Zero

e. Local Clock Granularity
 (for PCI Express Endpoints, Legacy Endpoints, or Root Complex Integrated Endpoints) — RO-Zero
 (otherwise)
 (for non-FLR testing) — HwInit
 (for FLR testing) — RO
f. RsvdP_31-16 — RO-Zero

PTM Control Register (Offset 08h) — DWORD

a. PTM Enable — RW
b. Root Select
 (if PTM Root Capable is 1) — RW
 (if PTM Root Capable is 0) — RW or RO-Zero
c. RsvdP_7-2 — RO-Zero
d. Effective Granularity
 (if PTM Requester Capable is 1) — RW
 (if PTM Requester Capable is 0) — RW or RO-Zero
e. RsvdP_31-16 — RO-Zero

11. The following default value checks are performed:

PTM Control Register Default Value (Offset 08h) — DWORD

a. PTM Enable — 0
b. Root Select — 0
c. Effective Granularity — 00h

12. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
13. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one PTM Extended Capability structure is present.
- ❑ A VF contains a PTM Extended Capability structure.
- ❑ The PTM Extended Capability structure is present in a Switch Downstream Port, a PCI Express to PCI/PCI-X Bridge, a PCI/PCI-X to PCI Express Bridge, or a Root Complex Event Collector.
- ❑ The Capability Version field does not report 1h.
- ❑ The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.

- The PTM Root Capable field reports 1, and the PTM Responder field does not report 1.
- In a Switch Upstream Port, only one of the PTM Requester Capable and PTM Responder Capable fields reports 1.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

2.2.65. TD_1_65 M-PCIe Extended Capability Structure

The test verifies that if the function under test reports a M-PCIe Extended Capability structure, it is implemented as defined in the relevant specifications.

Only a brief sub-set of M-PCIe testing will be implemented in the compliance test suite at this time.

Note: A comprehensive test description is provided in Section A.2 in Appendix A, for informational purposes only.

Relevant Specifications

- *PCI Express Base Specification*
- *M-PCIe ECN (to Base 3.0)*
- *ECN SR-IOV Table Updates (to SR-IOV 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0020h (M-PCIe Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. For Base 2.x or earlier testing: if the Extended Capability ID of 0020h is found in an Extended Capability structure, the test terminates with a failure.
4. For Base 4.x or later testing: if the Extended Capability ID of 0020h is found in an Extended Capability structure, the test terminates with a failure.
5. For Base 3.x testing: if the Extended Capability ID of 0020h is found in an Extended Capability structure for a VF, the test terminates with a failure.

6. For Base 3.x testing: if the Extended Capability ID of 0020h is found in an Extended Capability structure for device type that is a Root Complex Integrated Endpoint or a Root Complex Event Collector, the test terminates with a failure.
7. For Base 3.x or later testing: if the Extended Capability ID of 0020h is found in an Extended Capability structure for a function associated with an upstream port and the function is not function 0, the test terminates with a failure.
8. For Base 3.x testing: if the Extended Capability ID of 0020h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0020h is not found in an Extended Capability structure, the test skips to step 11.
9. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
10. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
11. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
12. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- A M-PCIe Extended Capability structure is present (for Base 4.x or later testing only).
- More than one M-PCIe Extended Capability structure is present.
- A VF contains a M-PCIe Extended Capability structure.
- A Root Complex Integrated Endpoint or a Root Complex Event Collector contains a M-PCIe Extended Capability structure.
- For a multi-function device associated with an upstream port, the M-PCIe Extended Capability structure is present in a function other than function 0.
- The Capability Version field does not report 1h.
- The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.

2.2.66. TD_1_66 FRS Queuing Extended Capability Structure

The test verifies that if the function under test reports a FRS Queuing Extended Capability structure, it is implemented as defined in the relevant specifications.

The test will only run for Base 3.x or later testing.

Relevant Specifications

- *PCI Express Base Specification*
- *ECN Readiness Notifications (RN) (to Base 3.0)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0021h (FRS Queuing Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. For Base 2.x or earlier testing: if the Extended Capability ID of 0021h is found in an Extended Capability structure, the test terminates with a failure.
4. For Base 3.x or later testing: if the Extended Capability ID of 0021h is found in an Extended Capability structure for a VF, the test terminates with a failure.
5. For Base 3.x or later testing: if the Extended Capability ID of 0021h is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
6. For Base 3.x or later testing: if the Extended Capability ID of 0021h is found in an Extended Capability structure for a device type that is a neither a Root Port nor a Root Complex Event Collector, the test terminates with a failure.
7. For Base 3.x or later testing: if the Extended Capability ID of 0021h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0021h is not found in an Extended Capability structure, the test skips to step 14.
8. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
9. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
10. A DWORD is read from offset 04h (FRS Queuing Capability register) and the following checks are performed:
 a. The FRS Queue Max Depth field must return a value greater than 0. If not, this is recorded as a failure, but the test continues.

11. A DWORD is read from offset 0Ch (FRS Message Queue register) and the following checks are performed:
 a. The FRS Message Queue Depth field must return a value less than or equal to the value returned in the FRS Queue Max Depth field. If not, this is recorded as a failure, but the test continues.

12. The following register field characteristic checks are performed:

 FRS Queuing Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

 FRS Queuing Capability Register (Offset 04h) — DWORD

a. FRS Queue Max Depth	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
b. RsvdP_15-12	RO-Zero
c. FRS Interrupt Message Number	RO
d. RsvdP_31-21	RO-Zero

 FRS Queuing Status Register (Offset 08h) — WORD

a. FRS Message Received	RW1C
b. FRS Message Overflow	RW1C
c. RsvdZ_15-2	RO-Zero

 FRS Queuing Control Register (Offset 0Ah) — WORD

a. FRS Interrupt Enable	RW
b. RsvdP_15-1	RO-Zero

 FRS Message Queue Register (Offset 0Ch) — DWORD

 Note: The FRS Message Queue register cannot be tested as writing it with any value will remove the oldest FRS Message from the Queue and replace it with the next oldest FRS Message (if one exists).

13. The following default value checks are performed:

 FRS Queuing Control Register Default Value (Offset 0Ah) — WORD

a. FRS Interrupt Enable	0

14. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

15. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one FRS Queuing Extended Capability structure is present.

- A VF contains a FRS Queuing Extended Capability structure.
- An RCRB contains a FRS Queuing Extended Capability structure.
- The FRS Queuing Extended Capability structure is present in any function other than the following: Root Port; Root Complex Event Collector.
- The Capability Version field does not report 1h.
- The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- The FRS Queue Max Depth field reports 0.
- The FRS Message Queue Depth field reports a value greater than the FRS Queue Max Depth field reports.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

2.2.67. TD_1_67 Readiness Time Reporting Extended Capability Structure

The test verifies that if the function under test reports a Readiness Time Reporting Extended Capability structure, it is implemented as defined in the relevant specifications.

The test will only run for Base 3.x or later testing.

Relevant Specifications

- *PCI Express Base Specification*
- *ECN Readiness Notifications (RN) (to Base 3.0)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0022h (Readiness Time Reporting Extended Capability) are found. If more than one is found, the test terminates with a failure.

3. For Base 2.x or earlier testing: if the Extended Capability ID of 0022h is found in an Extended Capability structure, the test terminates with a failure.
4. For Base 3.x or later testing: if the Extended Capability ID of 0022h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0022h is not found in an Extended Capability structure, the test skips to step 10.
5. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
6. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
7. The following tests are performed:
 a. A DWORD is read from offset 04h (Readiness Time Reporting 1 register) and the Valid field is checked to see if it returns 1. If it returns 0, then the read is repeated again, until either it returns 0, or until 1 minute has elapsed.
 b. If the Valid field returned 1, then go to step 8, otherwise skip to step 9. (Note: The Valid field never returning 1 is not a failure.)
8. A DWORD is read from each of offset 04h (Readiness Time Reporting 1 register) and offset 08h (Readiness Time Reporting 2 register) and the following checks are performed:
 a. The Scale sub-field of the Reset Time field must be a valid value (000b, 001b, 010b, 011b, 100b, 101b). All other encodings are reserved and are recorded as a failure, but the test continues.
 b. The Reset Time field must return a value less than or equal to A1Eh. If not, this is recorded as a failure, but the test continues.
 c. The Scale sub-field of the DL_Up Time field must be a valid value (000b, 001b, 010b, 011b, 100b, 101b). All other encodings are reserved and are recorded as a failure, but the test continues.
 d. The DL_Up Time field must return a value less than or equal to A1Eh. If not, this is recorded as a failure, but the test continues.
 e. The Scale sub-field of the FLR Time field must be a valid value (000b, 001b, 010b, 011b, 100b, 101b). All other encodings are reserved and are recorded as a failure, but the test continues.
 f. The FLR Time field must return a value less than or equal to A1Eh. If not, this is recorded as a failure, but the test continues.
 g. The Scale sub-field of the D3hot to D0 Time field must be a valid value (000b, 001b, 010b, 011b, 100b, 101b). All other encodings are reserved and are recorded as a failure, but the test continues.
 h. The D3hot to D0 Time field must return a value less than or equal to 80Ah. If not, this is recorded as a failure, but the test continues.

 Note: For functions where any of these fields are RsvdP, they will return 0, which still meets the requirements of all the expected values, so these tests will pass.
9. The following register field characteristic checks are performed:

Readiness Time Reporting Extended Capability Header (Offset 00h) — DWORD

 a. PCI Express Extended Capability ID RO
 b. Capability Version RO

c. Next Capability Offset — RO

Readiness Time Reporting 1 Register (Offset 04h) — DWORD

a. Reset Time
 (if Immediate Readiness is 1) — RO-Zero
 (otherwise)
 (for non-FLR testing) — HwInit
 (for FLR testing) — RO
b. DL_Up Time
 (for VFs or non-VF functions not associated with Upstream Ports) — RO-Zero
 (otherwise)
 (for non-FLR testing) — HwInit
 (for FLR testing) — RO
c. RsvdP_30-24 — RO-Zero
d. Valid
 (for non-FLR testing) — HwInit
 (for FLR testing) — RO

Readiness Time Reporting 2 Register (Offset 08h) — DWORD

a. FLR Time
 (if Function Level Reset Capability is 0) — RO-Zero
 (otherwise)
 (for non-FLR testing) — HwInit
 (for FLR testing) — RO
b. D3hot to D0 Time
 (if Immediate_Readiness_on_Return_to_D0 is 1) — RO-Zero
 (otherwise)
 (for non-FLR testing) — HwInit
 (for FLR testing) — RO
c. RsvdP_31-24 — RO-Zero

10. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
11. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- More than one Readiness Time Reporting Extended Capability structure is present.
- The Capability Version field does not report 1h.
- The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.

- The Scale sub-field of the Reset Time field reports a reserved value, when the Valid field returns 1.
- The Reset Time field reports a value greater than A1Eh, when the Valid field returns 1.
- The Scale sub-field of the DL_Up Time field reports a reserved value, when the Valid field returns 1.
- The DL_Up Time field reports a value greater than A1Eh, when the Valid field returns 1.
- The Scale sub-field of the FLR Time field reports a reserved value, when the Valid field returns 1.
- The FLR Time field reports a value greater than A1Eh, when the Valid field returns 1.
- The Scale sub-field of the D3hot to D0 Time field reports a reserved value, when the Valid field returns 1.
- The D3hot to D0 Time field reports a value greater than 80Ah, when the Valid field returns 1.
- Any of the register field characteristic tests fail.

2.2.68. TD_1_72 Data Link Feature Extended Capability Structure

The test verifies that if the function under test reports a Data Link Feature Extended Capability structure, it is implemented as defined in the relevant specifications.

The test will only run for Base 4.x or later testing.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0025h (Data Link Feature Extended Capability) are found. If more than one is found, the test terminates with a failure.

3. For Base 3.x or earlier testing: if the Extended Capability ID of 0025h is found in an Extended Capability structure, the test terminates with a failure.
4. For Base 4.x or later testing: if the Extended Capability ID of 0025h is found in an Extended Capability structure for a VF, the test terminates with a failure.
5. For Base 4.x or later testing: if the Extended Capability ID of 0025h is found in an Extended Capability structure for a device type that is a Root Complex Integrated Endpoint or a Root Complex Event Collector, the test terminates with a failure.
6. For Base 4.x or later testing: if the Extended Capability ID of 0025h is found in an Extended Capability structure for a function associated with a downstream port, then the following tests are performed:
 a. If the function under test reports the Max Link Speed field (Link Capabilities register) of 0100b or greater, then if the Extended Capability ID of 0025h is not found in an Extended Capability structure, the test terminates with a failure.
 b. If the function under test reports the Capability Version field (PCI Express Capabilities register) is 2h or greater:
 i. If the function under test reports the Supported Link Speeds Vector field (Link Capabilities 2 register) of 000 1000b or greater, then if the Extended Capability ID of 0025h is not found in an Extended Capability structure, the test terminates with a failure.
7. For Base 4.x or later testing: if the Extended Capability ID of 0025h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0025h is not found in an Extended Capability structure, the test skips to step 12.
8. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
9. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
10. For the DWORD at offset 04h (Data Link Feature Capabilities register) the following checks are performed and if any are not as stated, this is recorded as a failure, but the test continues:
 a. For Base 4.x or later, and the Max Link Speed/Supported Link Speeds field is 0100b or greater: the Local Data Link Feature Supported field must have bit 0 = 1.
11. The following register field characteristic checks are performed:

Data Link Feature Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

Data Link Feature Capabilities Register (Offset 04h) — DWORD

a. Local Data Link Feature Supported	
(for non-FLR testing: bit 0)	HwInit
(for FLR testing: bit 0)	RO
(bits 22-1)	RO-Zero
b. RsvdP_30-23	RO-Zero
c. Data Link Feature Exchange Enable	
(for non-FLR testing)	HwInit

(for FLR testing) RO

Data Link Feature Status Register (Offset 08h) –– DWORD

a. Remote Scaled Flow Control Supported RO
b. RsvdZ_30-23 RO-Zero
c. Remote Data Link Feature Supported Valid RO

12. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
13. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one Data Link Feature Extended Capability structure is present.
- ❑ A VF contains a Data Link Feature Extended Capability structure.
- ❑ A Root Complex Integrated Endpoint or a Root Complex Event Collector, and the Data Link Feature Extended Capability structure is present.
- ❑ A downstream port that supports 16.0 GT/s or greater, and the Data Link Feature Extended Capability structure is not present.
- ❑ The Capability Version field does not report 1h.
- ❑ The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- ❑ In a 16.0 GT/s supporting port, the Local Data Link Feature Supported bit is 0.
- ❑ Any of the register field characteristic tests fail.

2.2.69. TD_1_73 Physical Layer 16.0 GT/s Extended Capability Structure

The test verifies that if the function under test reports a Physical Layer 16.0 GT/s Extended Capability structure, it is implemented as defined in the relevant specifications.

The test will only run for Base 4.x or later testing.

Relevant Specifications

- ❑ *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0026h (Physical Layer 16.0 GT/s Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. For Base 3.x or earlier testing: if the Extended Capability ID of 0026h is found in an Extended Capability structure, the test terminates with a failure.
4. For Base 4.x or later testing: if the Extended Capability ID of 0026h is found in an Extended Capability structure for a VF, the test terminates with a failure.
5. For Base 4.x or later testing: if this is an RCRB, then the following tests are performed:
 a. If the RCRB does not contains a Root Complex Internal Link Control Extended Capability structure (Extended Capability ID of 0006h), then if the Extended Capability ID of 0026h is found in an Extended Capability structure, the test terminates with a failure.
 b. If the RCRB contains a Root Complex Internal Link Control Extended Capability structure (Extended Capability ID of 0006h) then:
 i. If the RCRB under test reports the Max Link Speed field (Root Complex Link Capabilities register) of 0100b or greater or the Supported Link Speeds Vector field (Root Complex Link Capabilities register) of 000 1000b or greater, then if the Extended Capability ID of 0026h is not found in an Extended Capability structure, the test terminates with a failure.
6. For Base 4.x or later testing: if this is not an RCRB, then the following tests are performed:
 a. If the device type is a Root Complex Integrated Endpoint or a Root Complex Event Collector, then if the Extended Capability ID of 0026h is found in an Extended Capability structure, the test terminates with a failure.
 b. If the device type is neither a Root Complex Integrated Endpoint nor a Root Complex Event Collector, and if the function under test is associated with an Upstream Port and is not function 0, then if the Extended Capability ID of 0026h is found in an Extended Capability structure, the test terminates with a failure.
 c. If the device type is neither a Root Complex Integrated Endpoint nor a Root Complex Event Collector, and if the function under test is associated with an Upstream Port and is function 0, or if the function under test is associated with a Downstream Port, then:
 i. If the function under test reports the Max Link Speed field (Link Capabilities register) of 0100b or greater, then if the Extended Capability ID of 0026h is not found in an Extended Capability structure, the test terminates with a failure.
 ii. If the function under test reports the Capability Version field (PCI Express Capabilities register) is 2h or greater:

a. If the function under test reports the Supported Link Speeds Vector field (Link Capabilities 2 register) of 000 1000b or greater, then if the Extended Capability ID of 0026h is not found in an Extended Capability structure, the test terminates with a failure.

7. For Base 4.x or later testing: if the Extended Capability ID of 0026h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0026h is not found in an Extended Capability structure, the test skips to step 13.
8. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
9. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
10. The following register field characteristic checks are performed:

Physical Layer 16.0 GT/s Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID — RO
b. Capability Version — RO
c. Next Capability Offset — RO

16.0 GT/s Capabilities Register (Offset 04h) — DWORD

a. RsvdP_31-0 — RO-Zero

16.0 GT/s Control Register (Offset 08h) — DWORD

a. RsvdP_31-0 — RO-Zero

16.0 GT/s Status Register (Offset 0Ch) — DWORD

a. Equalization 16.0 GT/s Complete
 (for Upstream Ports whose function number is non-zero) — RO-Zero
 (otherwise)
 (for non-FLR testing) — RO
 (for FLR testing) — ROS
 Note: During non-FLR testing, the Equalization 16.0 GT/s Complete field cannot be tested for stickiness even though its specified register field attribute is ROS because this field is reset to zero on link down, and is then again updated during link equalization.
b. Equalization 16.0 GT/s Phase 1 Successful
 (for Upstream Ports whose function number is non-zero) — RO-Zero
 (otherwise)
 (for non-FLR testing) — RO
 (for FLR testing) — ROS
 Note: During non-FLR testing, the Equalization 16.0 GT/s Phase 1 Successful field cannot be tested for stickiness even though its specified register field attribute is ROS because this field is reset to zero on link down, and is then again updated during link equalization.
c. Equalization 16.0 GT/s Phase 2 Successful
 (for Upstream Ports whose function number is non-zero) — RO-Zero
 (otherwise)
 (for non-FLR testing) — RO
 (for FLR testing) — ROS

Note: During non-FLR testing, the Equalization 16.0 GT/s Phase 2 Successful field cannot be tested for stickiness even though its specified register field attribute is ROS because this field is reset to zero on link down, and is then again updated during link equalization.

d. Equalization 16.0 GT/s Phase 3 Successful
 (for Upstream Ports whose function number is non-zero) RO-Zero
 (otherwise)
 (for non-FLR testing) RO
 (for FLR testing) ROS
 Note: During non-FLR testing, the Equalization 16.0 GT/s Phase 3 Successful field cannot be tested for stickiness even though its specified register field attribute is ROS because this field is reset to zero on link down, and is then again updated during link equalization.
e. Link Equalization Request 16.0 GT/s
 (for Upstream Ports whose function number is non-zero) RO-Zero
 (otherwise)
 (for non-FLR testing) RW1C
 (for FLR testing) RW1CS
 Note: During non-FLR testing, the Link Equalization Request 16.0 GT/s field cannot be tested for stickiness even though its specified register field attribute is RW1CS because this field is updated during link equalization.
f. RsvdZ_31-5 RO-Zero

16.0 GT/s Local Data Parity Mismatch Status Register (Offset 10h) — DWORD

a. (bits [Maximum Link Width-1] - 0) RW1CS
b. (if [Maximum Link Width] is less than 32:
 bits 31 - [Maximum Link Width]) RO-Zero

16.0 GT/s First Retimer Data Parity Mismatch Status Register (Offset 14h) — DWORD

a. (bits [Maximum Link Width-1] - 0) RW1CS
b. (if [Maximum Link Width] is less than 32:
 bits 31 - [Maximum Link Width]) RO-Zero

16.0 GT/s Second Retimer Data Parity Mismatch Status Register (Offset 18h) — DWORD

a. (bits [Maximum Link Width-1] - 0) RW1CS
b. (if [Maximum Link Width] is less than 32:
 bits 31 - [Maximum Link Width]) RO-Zero

16.0 GT/s Reserved Register (Offset 1Ch) — DWORD

a. RsvdP_31-0 RO-Zero

11. The following default value checks are performed:

16.0 GT/s Status Register Default Value (Offset 0Ch) — DWORD

a. Link Equalization Request 16.0 GT/s 0
 Note: A function under test that supports 16.0 GT/s will participate in Link Equalization, so the default values of the 16.0 GT/s equalization status fields cannot be tested on a 16.0 GT/s capable device.

16.0 GT/s Local Data Parity Mismatch Status Register Default Value (Offset 10h) — DWORD

a. (bits [Maximum Link Width-1] - 0)
 (if Max Link Speed/Supported Link Speeds = 0011b or less) 0

Note: A function under test that supports 16.0 GT/s may encounter link errors at 16.0 GT/s, so the default values of the 16.0 GT/s parity mismatch status fields cannot be tested on a 16.0 GT/s capable device.

16.0 GT/s First Retimer Data Parity Mismatch Status Register Default Value (Offset 14h) — DWORD

a. (bits [Maximum Link Width-1] - 0)
 (if Max Link Speed/Supported Link Speeds = 0011b or less) 0
 (if Max Link Speed/Supported Link Speeds = 0100b
 and Retimer Presence Detected = 0) 0
 Note: A function under test that supports 16.0 GT/s and has a Retimer connected may encounter link errors at 16.0 GT/s, so the default values of the 16.0 GT/s first retimer parity mismatch status fields cannot be tested on a 16.0 GT/s capable device that has a Retimer connected.

16.0 GT/s Second Retimer Data Parity Mismatch Status Register Default Value (Offset 18h) — DWORD

a. (bits [Maximum Link Width-1] - 0)
 (if Max Link Speed/Supported Link Speeds = 0011b or less) 0
 (if Max Link Speed/Supported Link Speeds = 0100b and
 Two Retimers Presence Detected = 0) 0
 Note: A function under test that supports 16.0 GT/s and has two Retimers connected may encounter link errors at 16.0 GT/s, so the default values of the 16.0 GT/s second retimer parity mismatch status fields cannot be tested on a 16.0 GT/s capable device that has two Retimers connected.

12. For each 16.0 GT/s Lane Equalization Control Entry register set instance Number [n] (from 0 to the value in Maximum Link Width - 1), the following register field characteristic checks are performed:

16.0 GT/s Lane Equalization Control Entry Register (n) (Offset 20h + n * 01h) – BYTE

a. Downstream Port 16.0 GT/s Transmitter Preset
 (for Upstream Ports with Crosslink Supported as 0) RO-Zero
 (for Upstream Ports with Crosslink Supported as 1)
 (for non-FLR testing) HwInit
 (for FLR testing) RO
 (for Downstream Ports) HwInit
b. Upstream Port 16.0 GT/s Transmitter Preset
 (for Upstream Ports with Crosslink Supported as 0) RO
 (for Upstream Ports with Crosslink Supported as 1)
 (for non-FLR testing) HwInit
 (for FLR testing) RO
 (for Downstream Ports) HwInit

13. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

14. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- More than one Physical Layer 16.0 GT/s Extended Capability structure is present.
- A VF contains a Physical Layer 16.0 GT/s Extended Capability structure.
- An RCRB that does not correspond to a Root Complex Internal Link and the Physical Layer 16.0 GT/s Extended Capability structure is present.
- An RCRB that corresponds to a Root Complex Internal Link and that supports 16.0 GT/s or greater, and the Physical Layer 16.0 GT/s Extended Capability structure is not present.
- A Root Complex Integrated Endpoint or a Root Complex Event Collector, and the Physical Layer 16.0 GT/s Extended Capability structure is present.
- An upstream port function other than 0, and the Physical Layer 16.0 GT/s Extended Capability structure is present.
- A device type that supports 16.0 GT/s or greater, and the Physical Layer 16.0 GT/s Extended Capability structure is not present.
- The Capability Version field does not report 1h.
- The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

2.2.70. TD_1_74 Margining Extended Capability Structure

The test verifies that if the function under test reports a Margining Extended Capability structure, it is implemented as defined in the relevant specifications.

The test will only run for Base 4.x or later testing.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0027h (Margining Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. For Base 3.x or earlier testing: if the Extended Capability ID of 0027h is found in an Extended Capability structure, the test terminates with a failure.
4. For Base 4.x or later testing: if the Extended Capability ID of 0027h is found in an Extended Capability structure for a VF, the test terminates with a failure.
5. For Base 4.x or later testing: if this is an RCRB, then the following tests are performed:
 a. If the RCRB does not contains a Root Complex Internal Link Control Extended Capability structure (Extended Capability ID of 0006h), then if the Extended Capability ID of 0027h is found in an Extended Capability structure, the test terminates with a failure.
 b. If the RCRB contains a Root Complex Internal Link Control Extended Capability structure (Extended Capability ID of 0006h) then:
 i. If the RCRB under test reports the Max Link Speed field (Root Complex Link Capabilities register) of 0100b or greater or the Supported Link Speeds Vector field (Root Complex Link Capabilities register) of 000 1000b or greater, then if the Extended Capability ID of 0027h is not found in an Extended Capability structure, the test terminates with a failure.
6. For Base 4.x or later testing: if this is not an RCRB, then the following tests are performed:
 a. If the device type is a Root Complex Integrated Endpoint or a Root Complex Event Collector, then if the Extended Capability ID of 0027h is found in an Extended Capability structure, the test terminates with a failure.
 b. If the device type is neither a Root Complex Integrated Endpoint nor a Root Complex Event Collector, and if the function under test is associated with an Upstream Port and is not function 0, then if the Extended Capability ID of 0027h is found in an Extended Capability structure, the test terminates with a failure.
 c. If the device type is neither a Root Complex Integrated Endpoint nor a Root Complex Event Collector, and if the function under test is associated with an Upstream Port and is function 0, or if the function under test is associated with a Downstream Port, then:
 i. If the function under test reports the Max Link Speed field (Link Capabilities register) of 0100b or greater, then if the Extended Capability ID of 0027h is not found in an Extended Capability structure, the test terminates with a failure.
 ii. If the function under test reports the Capability Version field (PCI Express Capabilities register) is 2h or greater:
 a. If the function under test reports the Supported Link Speeds Vector field (Link Capabilities 2 register) of 000 1000b or greater, then if the Extended Capability ID of 0027h is not found in an Extended Capability structure, the test terminates with a failure.
7. For Base 4.x or later testing: if the Extended Capability ID of 0027h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If

the Extended Capability ID of 0027h is not found in an Extended Capability structure, the test skips to step 13.

8. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
9. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
10. The following register field characteristic checks are performed:

Margining Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

Margining Port Capabilities Register (Offset 04h) — WORD

a. Margining Uses Driver Software	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
b. RsvdP_15-1	RO-Zero

Margining Port Status Register (Offset 06h) — WORD

a. Margining Ready	RO
b. Margining Software Ready	RO
c. RsvdZ_15-2	RO-Zero

11. For each Margining Lane Control Entry and Margining Lane Status Entry register set instance Number [n] (from 0 to the value in Maximum Link Width - 1), the following register field characteristic checks are performed:

Margining Lane Control Entry Register (n) (Offset 08h + n * 02h) – WORD

a. Receiver Number	RW
b. Margin Type	RW
c. Usage Model	RW
d. RsvdP_7	RO-Zero
e. Margin Payload	RW

Margining Lane Status Entry Register (n) (Offset 0Ah + n * 02h) – WORD

a. Receiver Number Status	RO
b. Margin Type Status	RO
c. Usage Model Status	RO
d. RsvdZ_7	RO-Zero
e. Margin Payload Status	RO

12. For each Margining Lane Control Entry and Margining Lane Status Entry register set instance Number [n] (from 0 to the value in Maximum Link Width - 1), the following default value checks are performed:

Margining Lane Control Entry Register (n) Default Value (Offset 08h + n * 02h) – WORD

a. Receiver Number	0
b. Margin Type	111b
c. Usage Model	0

d. Margin Payload 9Ch

Margining Lane Status Entry Register (n) Default Value (Offset 0Ah + n * 02h) – WORD

a. Receiver Number Status
 (for Upstream Ports with Crosslink Supported as 0) 0
 (for Upstream Ports with Crosslink Supported as 1
 and Max Link Speed/Supported Link Speeds = 0011b or less) 0
 (for Downstream Ports
 with Max Link Speed/Supported Link Speeds = 0011b or less) 0
b. Margin Type Status
 (for Upstream Ports with Crosslink Supported as 0) 0
 (for Upstream Ports with Crosslink Supported as 1
 and Max Link Speed/Supported Link Speeds = 0011b or less) 0
 (for Downstream Ports
 with Max Link Speed/Supported Link Speeds = 0011b or less) 0
c. Usage Model Status
 (for Upstream Ports with Crosslink Supported as 0) 0
 (for Upstream Ports with Crosslink Supported as 1
 and Max Link Speed/Supported Link Speeds = 0011b or less) 0
 (for Downstream Ports
 with Max Link Speed/Supported Link Speeds = 0011b or less) 0
d. Margin Payload Status
 (for Upstream Ports with Crosslink Supported as 0) 0
 (for Upstream Ports with Crosslink Supported as 1
 and Max Link Speed/Supported Link Speeds = 0011b or less) 0
 (for Downstream Ports
 with Max Link Speed/Supported Link Speeds = 0011b or less) 0

 Note: A downstream port under test that supports 16.0 GT/s will receive Control SKPs at 16.0 GT/s, so the default values of the margining lane status fields cannot be tested on a 16.0 GT/s capable downstream port.

13. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
14. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one Margining Extended Capability structure is present.
- ❑ A VF contains a Margining Extended Capability structure.

- An RCRB that does not correspond to a Root Complex Internal Link and the Margining Extended Capability structure is present.
- An RCRB that corresponds to a Root Complex Internal Link and that supports 16.0 GT/s or greater, and the Margining Extended Capability structure is not present.
- A Root Complex Integrated Endpoint or a Root Complex Event Collector, and the Margining Extended Capability structure is present.
- An upstream port function other than 0, and the Margining Extended Capability structure is present.
- A device type that supports 16.0 GT/s or greater, and the Margining Extended Capability structure is not present.
- The Capability Version field does not report 1h.
- The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

2.2.71. TD_1_75 Hierarchy ID Extended Capability Structure

The test verifies that if the function under test reports a Hierarchy ID Extended Capability structure, it is implemented as defined in the relevant specifications.

The test will only run for Base 3.1 or later testing.

Relevant Specifications

- *PCI Express Base Specification*
- *ECN Hierarchy ID Message (to Base 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0028h (Hierarchy ID Extended Capability) are found. If more than one is found, the test terminates with a failure.

3. For Base 3.0 or earlier testing: if the Extended Capability ID of 0028h is found in an Extended Capability structure, the test terminates with a failure.
4. For Base 3.1 or later testing: if the Extended Capability ID of 0028h is found in an Extended Capability structure for a device type that is a Root Complex Event Collector, the test terminates with a failure.
5. For Base 3.1 or later testing: if the Extended Capability ID of 0028h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0028h is not found in an Extended Capability structure, the test skips to step 10.
6. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
7. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
8. The following register field characteristic checks are performed:

Hierarchy ID Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

Hierarchy ID Status Register (Offset 04h) — DWORD

a. Message Routing ID	
(for RC Integrated Endpoints excluding VFs)	RO-Zero
(otherwise)	
(for Downstream Ports)	RO-Zero
(for Upstream Ports)	RO
b. RsvdZ_27-16	RO-Zero
c. Hierarchy ID Writeable	
(for VFs)	RW or RO-Zero
(for RC Integrated Endpoints excluding VFs)	RO
(otherwise)	
(for Downstream Ports)	RO-Ones
(for Upstream Ports)	RO-Zero
d. Hierarchy ID VF Configurable	
(for VFs with Hierarchy ID Writeable as RW)	RO-Ones
(otherwise)	RO-Zero
e. Hierarchy ID Pending	
(for Downstream Ports)	RW or RO-Zero

Note: After being written with 1, the Hierarchy ID Pending field returns 0 when read, once the Hierarchy ID message has been sent.

(for Upstream Ports)	RO-Zero
f. Hierarchy ID Valid	
(for Downstream Ports)	RO-Ones
(for Upstream Ports)	
(if Hierarchy ID Writable is 1)	RW

(if Hierarchy ID Writable is 0) RO

Hierarchy ID Data Register (Offset 08h) — DWORD

a. System GUID Authority ID
 (if Hierarchy ID Writable is 1) RW
 (if Hierarchy ID Writable is 0) RO
b. RsvdP_15-8 RO-Zero
c. Hierarchy ID
 (if Hierarchy ID Writable is 1) RW
 (if Hierarchy ID Writable is 0) RO

Hierarchy ID GUID 1 Register (Offset 0Ch) — DWORD

a. System GUID 1
 (if Hierarchy ID Writable is 1) RW
 (if Hierarchy ID Writable is 0) RO
b. RsvdP_31-16 RO-Zero

Hierarchy ID GUID 2 Register (Offset 10h) — DWORD

a. System GUID 2
 (if Hierarchy ID Writable is 1) RW
 (if Hierarchy ID Writable is 0) RO

Hierarchy ID GUID 3 Register (Offset 14h) — DWORD

a. System GUID 3
 (if Hierarchy ID Writable is 1) RW
 (if Hierarchy ID Writable is 0) RO

Hierarchy ID GUID 4 Register (Offset 18h) — DWORD

a. System GUID 4
 (if Hierarchy ID Writable is 1) RW
 (if Hierarchy ID Writable is 0) RO

Hierarchy ID GUID 5 Register (Offset 1Ch) — DWORD

a. System GUID 5
 (if Hierarchy ID Writable is 1) RW
 (if Hierarchy ID Writable is 0) RO

9. The following default value checks are performed:

Hierarchy ID Status Register Default Value (Offset 04h) – DWORD

a. Hierarchy ID Writeable
 (for VFs) 0
b. Hierarchy ID Pending 0
 (for Downstream Ports) 0
c. Hierarchy ID Valid 0
 (if Hierarchy ID Writable is 1) 0

Hierarchy ID Data Register Default Value (Offset 08h) – DWORD

a. System GUID Authority ID
 (if Hierarchy ID Writable is 1) 0
b. Hierarchy ID
 (if Hierarchy ID Writable is 1) 0

Hierarchy ID GUID 1 Register Default Value (Offset 0Ch) – DWORD

a. System GUID 1
(if Hierarchy ID Writable is 1) 0

Hierarchy ID GUID 2 Register Default Value (Offset 10h) – DWORD

a. System GUID 2
(if Hierarchy ID Writable is 1) 0

Hierarchy ID GUID 3 Register Default Value (Offset 14h) – DWORD

a. System GUID 3
(if Hierarchy ID Writable is 1) 0

Hierarchy ID GUID 4 Register Default Value (Offset 18h) – DWORD

a. System GUID 4
(if Hierarchy ID Writable is 1) 0

Hierarchy ID GUID 5 Register Default Value (Offset 1Ch) – DWORD

a. System GUID 5
(if Hierarchy ID Writable is 1) 0

Note: For those functions that capture the Hierarchy ID Message content, those captured fields cannot be tested for default value, as any incoming Hierarchy ID Message will cause those fields to be updated.

10. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
11. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one Hierarchy ID Extended Capability structure is present.
- ❑ A Root Complex Event Collector, and the Hierarchy ID Extended Capability structure is present.
- ❑ The Capability Version field does not report 1h.
- ❑ The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- ❑ Any of the register field characteristic tests fail.
- ❑ Any of the default value tests fail.

2.2.72. TD_1_76 Native PCIe Enclosure Management Extended Capability Structure

The test verifies that if the function under test reports a Native PCIe Enclosure Management Extended Capability structure, it is implemented as defined in the relevant specifications.

The test will only run for Base 3.1 or later testing.

Relevant Specifications

- *PCI Express Base Specification*
- *ECN Native PCIe Enclosure Management (to Base 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0029h (Native PCIe Enclosure Management Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. For Base 3.0 or earlier testing: if the Extended Capability ID of 0029h is found in an Extended Capability structure, the test terminates with a failure.
4. For Base 3.1 or later testing: if the Extended Capability ID of 0029h is found in an Extended Capability structure for a VF, the test terminates with a failure.
5. For Base 3.1 or later testing: if the Extended Capability ID of 0029h is found in an Extended Capability structure for a device type that is a Switch Upstream Port, a PCI/PCI-X to PCI Express Bridge, a PCI Express to PCI/PCI-X Bridge, or a Root Complex Event Collector, the test terminates with a failure.
6. For Base 3.1 or later testing: if the Extended Capability ID of 0029h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0029h is not found in an Extended Capability structure, the test skips to step 12.
7. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.

8. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
9. For the DWORD at offset 04h (NPEM Capability register) the following checks are performed and if any are not as stated, this is recorded as a failure, but the test continues:
 a. If the NPEM Capable field is 1: the NPEM OK Capable field must be 1, the NPEM Locate Capable field must be 1, the NPEM Fail Capable field must be 1, and the NPEM Rebuild Capable field must be 1.
10. The following register field characteristic checks are performed:

NEPM Extended Capability Header (Offset 00h) –– DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

NPEM Capability Register (Offset 04h) –– DWORD

a. NPEM Capable	
(for Upstream Ports)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
(for Downstream Ports)	HwInit
b. NPEM Reset Capable	
(for Upstream Ports)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
(for Downstream Ports)	HwInit
c. NPEM OK Capable	
(for Upstream Ports)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
(for Downstream Ports)	HwInit
d. NPEM Locate Capable	
(for Upstream Ports)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
(for Downstream Ports)	HwInit
e. NPEM Fail Capable	
(for Upstream Ports)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
(for Downstream Ports)	HwInit
f. NPEM Rebuild Capable	
(for Upstream Ports)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
(for Downstream Ports)	HwInit
g. NPEM PFA Capable	
(for Upstream Ports)	
(for non-FLR testing)	HwInit

(for FLR testing)	RO
(for Downstream Ports)	HwInit
h. NPEM Hot Spare Capable	
(for Upstream Ports)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
(for Downstream Ports)	HwInit
i. NPEM In A Critical Array Capable	
(for Upstream Ports)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
(for Downstream Ports)	HwInit
j. NPEM In A Failed Array Capable	
(for Upstream Ports)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
(for Downstream Ports)	HwInit
k. NPEM Invalid Device Type Capable	
(for Upstream Ports)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
(for Downstream Ports)	HwInit
l. NPEM Disabled Capable	
(for Upstream Ports)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
(for Downstream Ports)	HwInit
m. RsvdP_23-12	RO-Zero
n. Enclosure-specific Capabilities	
(for Upstream Ports)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
(for Downstream Ports)	HwInit

NPEM Control Register (Offset 08h) — DWORD

a. NPEM Enable	RW
b. NPEM Initiate Reset	RO-Zero
Note: The NPEM Initiate Reset field always returns 0 when read.	
c. NPEM OK Control	
(if NPEM OK Capable is 1)	RW
(if NPEM OK Capable is 0)	RW or RO-Zero
d. NPEM Locate Control	
(if NPEM Locate Capable is 1)	RW
(if NPEM Locate Capable is 0)	RW or RO-Zero
e. NPEM Fail Control	
(if NPEM Fail Capable is 1)	RW

(if NPEM Fail Capable is 0) — RW or RO-Zero

f. NPEM Rebuild Control
(if NPEM Rebuild Capable is 1) — RW
(if NPEM Rebuild Capable is 0) — RW or RO-Zero

g. NPEM PFA Control
(if NPEM PFA Capable is 1) — RW
(if NPEM PFA Capable is 0) — RW or RO-Zero

h. NPEM Hot Spare Control
(if NPEM Hot Spare Capable is 1) — RW
(if NPEM Hot Spare Capable is 0) — RW or RO-Zero

i. NPEM In A Critical Array Control
(if NPEM In A Critical Array Capable is 1) — RW
(if NPEM In A Critical Array Capable is 0) — RW or RO-Zero

j. NPEM In A Failed Array Control
(if NPEM In A Failed Array Capable is 1) — RW
(if NPEM In A Failed Array Capable is 0) — RW or RO-Zero

k. NPEM Invalid Device Type Control
(if NPEM Invalid Device Type Capable is 1) — RW
(if NPEM Invalid Device Type Capable is 0) — RW or RO-Zero

l. NPEM Disabled Control
(if NPEM Disabled Capable is 1) — RW
(if NPEM Disabled Capable is 0) — RW or RO-Zero

m. RsvdP_23-12 — RO-Zero

n. Enclosure-specific Controls
(if Enclosure-specific Capabilities is not 00h) — RW
(if Enclosure-specific Capabilities is 00h) — RW or RO-Zero

NPEM Status Register (Offset 0Ch) — DWORD

a. NPEM Command Completed — RW1C
b. RsvdZ_23-1 — RO-Zero
c. Enclosure-specific Status
(if Enclosure-specific Capabilities is not 00h) — RW1C
(if Enclosure-specific Capabilities is 00h) — RW1C or RO-Zero

11. The following default value checks are performed:

NPEM Control Register Default Value (Offset 08h) – DWORD

a. NPEM Enable — 0
b. NPEM OK Control — 0

c. NPEM Locate Control 0
d. NPEM Fail Control 0
e. NPEM Rebuild Control 0
f. NPEM PFA Control 0
g. NPEM Hot Spare Control 0
h. NPEM In A Critical Array Control 0
i. NPEM In A Failed Array Control 0
j. NPEM Invalid Device Type Control 0
k. NPEM Disabled Control 0
l. Enclosure-specific Controls 00h

NPEM Status Register Default Value (Offset 0Ch) – DWORD

a. NPEM Command Completed 0

12. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
13. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- More than one Native PCIe Enclosure Management Extended Capability structure is present.
- A VF contains a Native PCIe Enclosure Management Extended Capability structure.
- A Switch Upstream Port, a PCI/PCI-X to PCI Express Bridge, a PCI Express to PCI/PCI-X Bridge, or a Root Complex Event Collector, and the Native PCIe Enclosure Management Extended Capability structure is present.
- The Capability Version field does not report 1h.
- The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- The NPEM Capable bit is 1, but any of the following bits are 0: NPEM OK Capable; NPEM Locate Capable; NPEM Fail Capable; NPEM Rebuild Capable.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

2.2.73. TD_1_998 Aggregated Secondary Bus Reset

The purpose of this test is to ensure a cross section of the DUTs register field attributes behave properly in response to a Secondary Bus Reset (Hot Reset). This test is intended to aggregate several other TD_1_xx tests, but force Secondary Bus Reset as the reset mechanism. The subset of TD_1_xx tests chosen is based on a compromise between test coverage and total test run time.

This test can only be invoked from the main test selection menu under either "Run Compliance Test" or "Run Individual Register and Capability Test Cases".

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Check if the DUT contains a port. If not, the test terminates (this is not a failure and the test result is reported as skipped).
2. Check the port direction of the DUT. Create the list of tests to run as follows:

 Test 1: TD_1_4
 Test 2: TD_1_5
 Test 3: TD_1_7
 Test 4: TD_1_11
 Test 5: TD_1_15
 Test 6: TD_1_40
 Test 7: TD_1_41
 Test 8: TD_1_58
 Test 9: TD_1_73

3. Set the test selection to the first test in the test list.
4. Run the selected test from the test list according to its specific test algorithm, but forcing any reset event to use the Secondary Bus Reset mechanism (see Section 2.1.1.1.2) in place of any other selected reset mechanism.
5. Increment the test selection and repeat step 4, until all tests in the test list have been run.

The test *fails* if:

- Any of the specific test's failure cases occur.

The test *warns* if:

- Any of the specific test's warning cases occur.

2.2.74. TD_1_999 Aggregated Function Level Reset

The purpose of this test is to ensure a cross section of the DUTs register field attributes behave properly in response to a Function Level Reset (FLR). This test is intended to aggregate several

other TD_1_xx tests, but force Function Level Reset as the reset mechanism. The subset of TD_1_xx tests chosen is based on a compromise between test coverage and total test run time. This test can only be invoked from the main test selection menu under either "Run Compliance Test" or "Run Individual Register and Capability Test Cases".

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. If the Function Level Reset Capability field (Device Capabilities register) returns 0, the test terminates (this is not a failure and the test result is reported as skipped).
2. Create the list of tests to run as follows:

 Test 1: TD_1_4
 Test 2: TD_1_5
 Test 3: TD_1_11
 Test 4: TD_1_40
 Test 5: TD_1_41

3. Set the test selection to the first test in the test list.
4. Run the selected test from the test list according to its specific test algorithm, but forcing any reset event to use the Function Level Reset mechanism (see Section 2.1.1.1.3) in place of any other selected reset mechanism.
5. Increment the test selection and repeat step 4, until all tests in the test list have been run.

The test *fails* if:

- Any of the specific test's failure cases occur.

The test *warns* if:

- Any of the specific test's warning cases occur.

2.3. Configuration Register Tests (Devices with Upstream Ports)

This set of tests applies only to upstream ports of Switches, Bridges, or Endpoint devices.

2.3.1. TD_2_1 ASPM Configuration Stress (Upstream Ports)

The test verifies that if the function under test implements ASPM, test software attempts to configure the function under test to a variety of different ASPM settings will not cause the device to operate abnormally, as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on upstream ports of PCI Express Endpoints, Legacy Endpoints, Switch Upstream Ports, and PCI Express to PCI/PCI-X Bridges.

(Note: The downstream port connected to the function under test must be known to operate correctly in each of its supported ASPM modes.)

Starting Configuration

Function under test is completely uninitialized following a reset.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1. If the procedure fails to complete successfully, the test terminates with failure.
2. Read the Active State Power Management (ASPM) Support field from the Link Capabilities register of the function under test (this will also be referred to as the upstream port of the link). Record this value in Upstream ASPM [UASPMS].
3. Read the Active State Power Management (ASPM) Support field from the Link Capabilities register of the immediate upstream device's port (the downstream port of the link connected to the function under test), which will be referred to as the downstream port of the link. Record this value in Downstream ASPM [DASPMS].
4. Read the Retimer Presence Detect Supported field from the Link Capabilities 2 register of the immediate upstream device's port (the downstream port of the link connected to the function under test), and if the field's value is 0, then set [RTPSNT] to 0, but if the field's value is 1 then:
 a. Read the Retimer Presence Detected field from the Link Status 2 register of the immediate upstream device's port (the downstream port of the link connected to the function under test). Record this value in Retimer Present [RTPSNT].
5. If [RTPSNT] is 1, then skip to step 1.
6. Read the Two Retimers Presence Detect Supported field from the Link Capabilities 2 register of the immediate upstream device's port (the downstream port of the link connected to the

function under test), and if the field's value is 0, then set [RTPSNT] to 0, but if the field's value is 1 then:

a. Read the Two Retimers Presence Detected field from the Link Status 2 register of the immediate upstream device's port (the downstream port of the link connected to the function under test). Record this value in [RTPSNT].

7. Use the level of testing to determine the interpretation of the Active State Power Management (ASPM) Support field, and what values to write to the Active State Power Management (ASPM) Control field in the Link Control register of the upstream port of the link and the downstream port of the link. If the function under test is not a VF, but is part of a multi-function device (the Multi-Function Device field of Header Type register is 1), then the same ASPM setting value must be written to all non-VF functions in that multi-function device. If the function under test is a VF, then the ASPM setting value must be written to the PF associated with that VF, as well as any other non-VF functions in the multi-function device. If [RTPSNT] is 1, then all [UASPMS] and [DASPMS] values are modified so that bit 0 of the Active State Power Management (ASPM) Control field is forced to 0b (L0s disabled).
 a. For Base 1.x testing: use Table 1 in Section 2.1.2.21.1, together with [UASPMS] and [DASPMS] to determine which ASPM combinations are supported, perform step 1 for each of the supported ASPM combinations in Table 1 in Section 2.1.2.21.1. If the total number of iterations is less than 100, repeat this entire step again.
 b. For Base 2.x or later testing: read the ASPM Optionality Compliance field from the Link Capabilities register in both the upstream port of the link and the downstream port of the link, and based on their reported values perform the following:
 i. If the ASPM Optionality Compliance field is 0 in both the upstream port of the link and the downstream port of the link, use Table 1 in Section 2.1.2.21.1, together with [UASPMS] and [DASPMS] to determine which ASPM combinations are supported, perform step 1 for each of the supported ASPM combinations in Table 1 in Section 2.1.2.21.1. If the total number of iterations is less than 100, repeat this entire step again.
 ii. If the ASPM Optionality Compliance field is 1 in the upstream port of the link and the ASPM Optionality Compliance field is 0 in the downstream port of the link, use Table 2 in Section 2.1.2.21.2, together with [UASPMS] and [DASPMS] to determine which ASPM combinations are supported, perform step 1 for each of the supported ASPM combinations in Table 2 in Section 2.1.2.21.2. If the total number of iterations is less than 100, repeat this entire step again.
 iii. If the ASPM Optionality Compliance field is 0 in the upstream port of the link and the ASPM Optionality Compliance field is 1 in the downstream port of the link, use Table 3 in Section 2.1.2.21.3, together with [UASPMS] and [DASPMS] to determine which ASPM combinations are supported, perform step 1 for each of the supported ASPM combinations in Table 3 in Section 2.1.2.21.3. If the total number of iterations is less than 100, repeat this entire step again.
 iv. If the ASPM Optionality Compliance field is 1 in both the upstream port of the link and the downstream port of the link, use Table 4 in Section 2.1.2.21.4, together with [UASPMS] and [DASPMS] to determine which ASPM combinations are supported, perform step 1 for each of the supported ASPM combinations in Table 4 in Section 2.1.2.21.4. If the total number of iterations is less than 100, repeat this entire step again.

8. For functions under test that have a link, the test is run at each of the following link speeds:
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.

c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- The function under test fails to respond to any part of the standard configuration sequence.

2.3.2. TD_2_2 Link Retraining Stress (Upstream Ports)

The test verifies that the function under test correctly handles link retraining when it is initiated using the Link Control register of the downstream port connected to the function under test as required in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on upstream ports of PCI Express Endpoints, Legacy Endpoints, Switch Upstream Ports, and PCI Express to PCI/PCI-X Bridges.

Starting Configuration

The device is placed into the desired starting state (D0-Uninitialized) following the standard initialization sequence in Section 2.1.1. Testing in additional Dx states may be optionally supported.

Overview of Test Steps

Test software performs the following steps:

1. Test software configures the function under test following the procedure described in Section 2.1.1. If the procedure fails to complete successfully, the test terminates with failure.
2. Test software modifies at least one non-sticky register field value from its default value. Any of the following fields can be used as long as they are implemented as RW in the target: Memory Space Enable (Command register); I/O Space Enable (Command register); Bus Master Enable (Command register); Interrupt Disable (Command register). If none of these fields are implemented as RW in the target, then other non-sticky RW fields can be used. If test software cannot find any non-sticky RW field in the target, then this step is skipped.
3. Test software reads the Negotiated Link Width field (Link Status register) for both the function under test and the downstream port of the link. Both values must be the same otherwise the test terminates with failure. If the same, the value is recorded in the Link Width Value [LWV].
4. Test software writes 1 to the Retrain Link field (Link Control register) on the downstream port of the link using a WORD access, while preserving all the other fields in this register.
5. Test software reads the Link Training field (Link Status register) on the downstream port of the link, until it returns 0.
6. Test software reads the Negotiated Link Width field (Link Status register) for both the function under test and the downstream port of the link. Both values must be the same otherwise the test terminates with failure. If the same, the value must be the same as [LWV] otherwise the test terminates with failure.

7. Test software reads back the register field programmed to a non-default value in step 2 and confirms it has not changed back to its default value. If it has changed back then the test terminates with failure.
8. Steps 2-7 are repeated for 100 iterations.
9. For functions under test that have a link, the test is run at each of the following link speeds:
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- The reported Negotiated Link Width of the upstream component fails to match the Negotiated Link Width of the downstream component.
- Link retraining causes the Negotiated Link Width to change.
- Link retraining causes the upstream port to reset (restoring default values).

2.3.3. TD_2_3 Tolerance of Hot-Plug Signaling/Ignored Messages

The test verifies that the function under test continues to be configurable and respond normally when Hot-Plug Signaling/Ignored messages are intermixed with the standard configuration sequence as required in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on upstream ports of PCI Express Endpoints, Legacy Endpoints, Switch Upstream Ports, and PCI Express to PCI/PCI-X Bridges.

(Note: The downstream port originating the link hierarchy containing the function under test must be known to generate Hot-Plug Signaling message types. As this support was deleted in any Base 1.1 complaint device, these message types are now defined as Ignored messages and are not to be generated by any Base 1.1 or later compliant port.)

Starting Configuration

The device is placed into the desired starting state (D0-Uninitialized) following the standard initialization sequence in Section 2.1.1. Testing in additional Dx states may be optionally supported.

Overview of Test Steps

Test software performs the following steps:

1. Check that the downstream port originating the link hierarchy containing the function under test is capable of sending Hot-Plug Messages (Attention Indicator, or Power Indicator). If not, the test terminates (this is not a failure and the test result is reported as skipped).

2. Configure the function under test following the procedure described in Section 2.1.1 (D0-Initialized).
3. At the end of the configuration sequence test software writes 01b to the Attention Indictor Control field of the downstream port to which the function under test is attached. This causes an ATTENTION_INDICATOR message to be sent to the function under test.
4. Test software reads standard configuration registers to ensure that the function under test is still responding normally. If not, the test terminates with a failure.
5. The standard configuration sequence described in Section 2.1.1 (D0-Initialized) is run with a random Attention or Power Indicator control message sent between every normal configuration access.
6. Step 5 is repeated for 100 iterations.
7. A flood of Attention/Power Indicator control messages (500) are sent to the function under test.
8. Test software ensures the device configuration registers can still be accessed normally. If not, the test terminates with a failure.
9. Note: If the function under test has Attention and Power Indicators present on the card, test software uses other mechanisms to send unsupported messages to the function under test (if possible).
10. For functions under test that have a link, the test is run at each of the following link speeds:
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- The function under test fails to respond normally to configuration accesses at any time.
- The function under test produces an error in response to an Attention or Power Indicator control message.

2.3.4. TD_2_4 Response To Earliest Allowed Configuration Requests After Reset

The test verifies that the function under test operates normally when test software attempts to configure the function under test such that configuration requests begin as early as allowed after reset as required in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on upstream ports of PCI Express Endpoints, Legacy Endpoints, Switch Upstream Ports, and PCI Express to PCI/PCI-X Bridges.

Starting Configuration

Function under test is completely uninitialized following a reset.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1. In all cases the first configuration request following reset is sent at the earliest allowed time (100 ms). If the procedure fails to complete successfully, the test terminates with failure.
2. Repeat step 1 for 100 iterations.
3. For functions under test that have a link, the test is run at each of the following link speeds:
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- ❑ The function under test fails to respond to any part of the standard configuration sequence.

2.3.5. TD_2_6 Secondary Bus Reset (Upstream Ports)

The test verifies that the function under test implements the Secondary Bus Reset (Bridge Control register) behavior as defined in the relevant specifications.

Relevant Specifications

- ❑ *PCI Express Base Specification*
- ❑ *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on upstream ports of Switch Upstream Ports, and PCI Express to PCI/PCI-X Bridges.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Verify that a device is present on the secondary side of the Bridge or on any downstream port of the Switch. If not, the test terminates (this is not a failure and the test result is reported as skipped).
3. Modify some non-sticky register field in the device on the secondary side of the Bridge or on any downstream port of the Switch. Any of the following fields can be used as long as they are implemented as RW in the target: Memory Space Enable (Command register); I/O Space

Enable (Command register); Bus Master Enable (Command register); Interrupt Disable (Command register). If none of these fields are implemented as RW in the target, then other non-sticky RW fields can be used. If test software cannot find any non-sticky RW field in the target, then this step is skipped.

4. A reset of the secondary interface is initiated by test software through writing a 1 to the Secondary Bus Reset field in the function under test (for a Bridge, the Bridge Control register in the Bridge; for a Switch, the Bridge Control register in the Switch Upstream Port) using a WORD access, while preserving all the other fields in this register, and then writing a 0 using a WORD access, while preserving all the other fields in this register. (See Section 2.1.1.1.2 for details of the reset algorithm.)
5. If a non-sticky RW field was found in step 3, after the necessary delay, verify the same non-sticky field (from step 3) in the device on the secondary side of the Bridge or on any downstream port of the Switch is reset to its default value. If the value has not changed to the default value, the test fails and is terminated.
6. For functions under test that have a link, the test is run at each of the following link speeds:
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- For a Bridge, a non-sticky register field in the device on the secondary side of the Bridge fails to reset to its default settings.
- For a Switch, a non-sticky register field in the device on any downstream port of the Switch fails to reset to its default settings.

2.3.6. TD_2_7 Requested Link Speed (Upstream Ports)

The test verifies that the function under test can function at the correct link speed when test software attempts to configure the function under test with each supported link speed as defined in the relevant specifications. (The test initiates the link speed change from the immediate downstream port connected to the function under test, but only if that downstream port supports selecting that link speed using the Target Link Speed field. In order to pass, the test requires that the downstream port supports all link speeds defined in the relevant specification. In order to pass, the test requires that the function under test be able train to each link speed up to the maximum link speed supported by the function under test.)

The test will run for 100 iterations and if any single iteration fails the test will report a failure and stop. The iteration stages will be different for the different Base levels of testing. However, in all stage, any link speed change will be initiated by the downstream port. (Note: The downstream port is required to attempt a speed change any time the Retrain Link field (Link Control register) is set to 1 and the current link speed is not equal to the Target Link Speed field. However, the actual negotiated link speed will be determined by the lowest Target Link Speed field of both the downstream port and upstream port.)

- For Base 1.x testing, the test will attempt to step the downstream port target link speed through a sequence of one stage, with the sequence repeated until 100 total iterations are performed.

- For a 2.5 GT/s capable DUT connected to a 2.5 GT/s or greater capable port, the sequence is:
 Stage 0: DP2.5+UP2.5=2.5
- For a 5.0 GT/s capable DUT connected to a 2.5 GT/s or greater capable port, the sequence is:
 Stage 0: DP2.5+UP5.0=2.5
- For an 8.0 GT/s capable DUT connected to a 2.5 GT/s or greater capable port, the sequence is:
 Stage 0: DP2.5+UP8.0=2.5
- For a 16.0 GT/s capable DUT connected to a 2.5 GT/s or greater capable port, the sequence is:
 Stage 0: DP2.5+UP16.0=2.5

- For Base 2.x testing, the test will attempt to step the downstream port target link speed through a multi-stage sequence of up to two stages, with the sequence repeated until 100 total iterations are performed.
 - For a 2.5 GT/s capable DUT connected to a 2.5 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP2.5=2.5
 - For a 2.5 GT/s capable DUT connected to a 5.0 GT/s or greater capable port, the sequence is:
 Stage 0: DP2.5+UP2.5=2.5
 Stage 1: DP5.0+UP2.5=2.5
 - For a 5.0 GT/s capable DUT connected to a 2.5 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP5.0=2.5
 - For a 5.0 GT/s capable DUT connected to a 5.0 GT/s or greater capable port, the sequence is:
 Stage 0: DP2.5+UP5.0=2.5
 Stage 1: DP5.0+UP5.0=5.0
 - For an 8.0 GT/s capable DUT connected to a 2.5 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP8.0=2.5
 - For an 8.0 GT/s capable DUT connected to a 5.0 GT/s or greater capable port, the sequence is:
 Stage 0: DP2.5+UP8.0=2.5
 Stage 1: DP5.0+UP8.0=5.0
 - For a 16.0 GT/s capable DUT connected to a 2.5 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP16.0=2.5
 - For a 16.0 GT/s capable DUT connected to a 5.0 GT/s or greater capable port, the sequence is:
 Stage 0: DP2.5+UP16.0=2.5
 Stage 1: DP5.0+UP16.0=5.0

- For Base 3.x testing, the test will attempt to step the downstream port target link speed through a multi-stage sequence of up to six stages, with the sequence repeated until 100 total iterations are performed.
 - For a 2.5 GT/s capable DUT connected to a 2.5 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP2.5=2.5
 - For a 2.5 GT/s capable DUT connected to a 5.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP2.5=2.5
 Stage 1: DP5.0+UP2.5=2.5
 - For a 2.5 GT/s capable DUT connected to an 8.0 GT/s or greater capable port, the sequence is:
 Stage 0: DP2.5+UP2.5=2.5
 Stage 1: DP5.0+UP2.5=2.5
 Stage 2: DP8.0+UP2.5=2.5
 Stage 3: DP5.0+UP2.5=2.5
 Stage 4: DP2.5+UP2.5=2.5
 Stage 5: DP8.0+UP2.5=2.5
 - For a 5.0 GT/s capable DUT connected to a 2.5 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP5.0=2.5
 - For a 5.0 GT/s capable DUT connected to a 5.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP5.0=2.5
 Stage 1: DP5.0+UP5.0=5.0
 - For a 5.0 GT/s capable DUT connected to an 8.0 GT/s or greater capable port, the sequence is:
 Stage 0: DP2.5+UP5.0=2.5
 Stage 1: DP5.0+UP5.0=5.0
 Stage 2: DP8.0+UP5.0=5.0
 Stage 3: DP5.0+UP5.0=5.0
 Stage 4: DP2.5+UP5.0=2.5
 Stage 5: DP8.0+UP5.0=5.0
 - For an 8.0 GT/s capable DUT connected to a 2.5 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP8.0=2.5
 - For an 8.0 GT/s capable DUT connected to a 5.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP8.0=2.5
 Stage 1: DP5.0+UP8.0=5.0
 - For an 8.0 GT/s capable DUT connected to an 8.0 GT/s or greater capable port, the sequence is:

Stage 0: DP2.5+UP8.0=2.5
Stage 1: DP5.0+UP8.0=5.0
Stage 2: DP8.0+UP8.0=8.0
Stage 3: DP5.0+UP8.0=5.0
Stage 4: DP2.5+UP8.0=2.5
Stage 5: DP8.0+UP8.0=8.0

- For a 16.0 GT/s capable DUT connected to a 2.5 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP16.0=2.5
- For a 16.0 GT/s capable DUT connected to a 5.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP16.0=2.5
 Stage 1: DP5.0+UP16.0=5.0
- For a 16.0 GT/s capable DUT connected to an 8.0 GT/s or greater capable port, the sequence is:
 Stage 0: DP2.5+UP16.0=2.5
 Stage 1: DP5.0+UP16.0=5.0
 Stage 2: DP8.0+UP16.0=8.0
 Stage 3: DP5.0+UP16.0=5.0
 Stage 4: DP2.5+UP16.0=2.5
 Stage 5: DP8.0+UP16.0=8.0

(Note: For 8.0 GT/s or greater, this test assumes that hardware initiated Link Equalization has already been performed by the downstream port connected to the function under test. The test does not attempt to perform software initiated Link Equalization.)

- For Base 4.x testing, the test will attempt to step the downstream port target link speed through a multi-stage sequence of up to twelve stages, with the sequence repeated until 100 total iterations are performed.
 - For a 2.5 GT/s capable DUT connected to a 2.5 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP2.5=2.5
 - For a 2.5 GT/s capable DUT connected to a 5.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP2.5=2.5
 Stage 1: DP5.0+UP2.5=2.5
 - For a 2.5 GT/s capable DUT connected to an 8.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP2.5=2.5
 Stage 1: DP5.0+UP2.5=2.5
 Stage 2: DP8.0+UP2.5=2.5
 Stage 3: DP5.0+UP2.5=2.5
 Stage 4: DP2.5+UP2.5=2.5
 Stage 5: DP8.0+UP2.5=2.5
 - For a 2.5 GT/s capable DUT connected to a 16.0 GT/s or greater capable port, the sequence is:

Stage 0: DP2.5+UP2.5=2.5
Stage 1: DP5.0+UP2.5=2.5
Stage 2: DP8.0+UP2.5=2.5
Stage 3: DP5.0+UP2.5=2.5
Stage 4: DP2.5+UP2.5=2.5
Stage 5: DP8.0+UP2.5=2.5
Stage 6: DP16.0+UP2.5=2.5
Stage 7: DP8.0+UP2.5=2.5
Stage 8: DP2.5+UP2.5=2.5
Stage 9: DP16.0+UP2.5=2.5
Stage 10: DP5.0+UP2.5=2.5
Stage 11: DP16.0+UP2.5=2.5

- For a 5.0 GT/s capable DUT connected to a 2.5 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP5.0=2.5
- For a 5.0 GT/s capable DUT connected to a 5.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP5.0=2.5
 Stage 1: DP5.0+UP5.0=5.0
- For a 5.0 GT/s capable DUT connected to an 8.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP5.0=2.5
 Stage 1: DP5.0+UP5.0=5.0
 Stage 2: DP8.0+UP5.0=5.0
 Stage 3: DP5.0+UP5.0=5.0
 Stage 4: DP2.5+UP5.0=2.5
 Stage 5: DP8.0+UP5.0=5.0
- For a 5.0 GT/s capable DUT connected to a 16.0 GT/s or greater capable port, the sequence is:
 Stage 0: DP2.5+UP5.0=2.5
 Stage 1: DP5.0+UP5.0=5.0
 Stage 2: DP8.0+UP5.0=5.0
 Stage 3: DP5.0+UP5.0=5.0
 Stage 4: DP2.5+UP5.0=2.5
 Stage 5: DP8.0+UP5.0=5.0
 Stage 6: DP16.0+UP5.0=5.0
 Stage 7: DP8.0+UP5.0=5.0
 Stage 8: DP2.5+UP5.0=2.5
 Stage 9: DP16.0+UP5.0=5.0
 Stage 10: DP5.0+UP5.0=5.0
 Stage 11: DP16.0+UP5.0=5.0
- For an 8.0 GT/s capable DUT connected to a 2.5 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP8.0=2.5
- For an 8.0 GT/s capable DUT connected to a 5.0 GT/s capable port, the sequence is:

Stage 0: DP2.5+UP8.0=2.5
Stage 1: DP5.0+UP8.0=5.0

- For an 8.0 GT/s capable DUT connected to an 8.0 GT/s capable port, the sequence is:

 Stage 0: DP2.5+UP8.0=2.5
 Stage 1: DP5.0+UP8.0=5.0
 Stage 2: DP8.0+UP8.0=8.0
 Stage 3: DP5.0+UP8.0=5.0
 Stage 4: DP2.5+UP8.0=2.5
 Stage 5: DP8.0+UP8.0=8.0

- For an 8.0 GT/s capable DUT connected to a 16.0 GT/s or greater capable port, the sequence is:

 Stage 0: DP2.5+UP8.0=2.5
 Stage 1: DP5.0+UP8.0=5.0
 Stage 2: DP8.0+UP8.0=8.0
 Stage 3: DP5.0+UP8.0=5.0
 Stage 4: DP2.5+UP8.0=2.5
 Stage 5: DP8.0+UP8.0=8.0
 Stage 6: DP16.0+UP8.0=8.0
 Stage 7: DP8.0+UP8.0=8.0
 Stage 8: DP2.5+UP8.0=2.5
 Stage 9: DP16.0+UP8.0=8.0
 Stage 10: DP5.0+UP8.0=5.0
 Stage 11: DP16.0+UP8.0=8.0

- For a 16.0 GT/s capable DUT connected to a 2.5 GT/s capable port, the sequence is:

 Stage 0: DP2.5+UP16.0=2.5

- For a 16.0 GT/s capable DUT connected to a 5.0 GT/s capable port, the sequence is:

 Stage 0: DP2.5+UP16.0=2.5
 Stage 1: DP5.0+UP16.0=5.0

- For a 16.0 GT/s capable DUT connected to an 8.0 GT/s capable port, the sequence is:

 Stage 0: DP2.5+UP16.0=2.5
 Stage 1: DP5.0+UP16.0=5.0
 Stage 2: DP8.0+UP16.0=8.0
 Stage 3: DP5.0+UP16.0=5.0
 Stage 4: DP2.5+UP16.0=2.5
 Stage 5: DP8.0+UP16.0=8.0

- For a 16.0 GT/s capable DUT connected to a 16.0 GT/s or greater capable port, the sequence is:

Stage 0: DP2.5+UP16.0=2.5
Stage 1: DP5.0+UP16.0=5.0
Stage 2: DP8.0+UP16.0=8.0
Stage 3: DP5.0+UP16.0=5.0
Stage 4: DP2.5+UP16.0=2.5
Stage 5: DP8.0+UP16.0=8.0
Stage 6: DP16.0+UP16.0=16.0
Stage 7: DP8.0+UP16.0=8.0
Stage 8: DP2.5+UP16.0=2.5
Stage 9: DP16.0+UP16.0=16.0
Stage 10: DP5.0+UP16.0=5.0
Stage 11: DP16.0+UP16.0=16.0

(Note: For 8.0 GT/s or greater, this test assumes that hardware initiated Link Equalization has already been performed by the downstream port connected to the function under test. The test does not attempt to perform software initiated Link Equalization.)

The test only runs if both the function under test and the downstream port connected to the function under test, report a PCI Express Capability Version of 2h or greater.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on upstream ports of PCI Express Endpoints, Legacy Endpoints, Switch Upstream Ports, and PCI Express to PCI/PCI-X Bridges; that report a PCI Express Capability Version of 2h or greater.

Starting Configuration

Function under test is completely uninitialized following a reset.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Set Iteration Count [ICNT] to 0 and set Downstream port iteration Stage [DSTAGE] to 0.
3. For this test, the immediate upstream device's port (the downstream port of the link connected to the function under test) will be referred to as the downstream port of the link. Downstream port Link Speed Value [DLSV] is used to control the link speed of the downstream port of the link. Initially set [DLSV] to 0001b.
4. For this test, function 0 of the device containing the function under test will be referred to as the upstream port of the link. Upstream port Link Speed Value [ULSV] is used to control the link speed of the upstream port of the link.
5. Read the Link Capabilities register bits 3-0 value from the upstream port of the link and assign it to Upstream port Supported Speed Value [USSV] and perform the following:
 a. If [USSV] is 0000b, the test terminates with failure.
 b. If [USSV] is 0001b or greater, then set [ULSV] to [USSV].

6. The Target Link Speed field (Link Control 2 register) is set to [ULSV] on the upstream port of the link and then the following tests are performed:
 a. If [USSV] is 0001b: the same Target Link Speed field is read back, and if it does not return [ULSV] or 0000b, the test terminates with failure.
 b. If [USSV] is greater than 0001b: the same Target Link Speed field is read back, and if it does not return [ULSV], the test terminates with failure.
7. Read the immediate upstream device's port (the downstream port of the link connected to the function under test) Link Capabilities register bits 3-0 value and assign it to Downstream port Supported Speed Value [DSSV] and perform the following:
 a. If [DSSV] is 0000b, terminate the test, however this is not considered a failure, but rather the test result is reported as skipped.
 b. If [DLSV] is 0010b or greater and [DSSV] is 0001b, then set [DSTAGE] to 0 and set [DLSV] to 0001b.
 c. If [DLSV] is 0011b or greater and [DSSV] is 0010b, then set [DSTAGE] to 0 and set [DLSV] to 0001b.
 d. If [DLSV] is 0100b and [DSSV] is 0011b, then set [DSTAGE] to 0 and set [DLSV] to 0001b.
8. The Target Link Speed field (Link Control 2 register) is set to [DLSV] on the immediate upstream device's port (the downstream port of the link connected to the function under test). This port will be referred to as the downstream port of the link.
9. The Target Link Speed field (Link Control 2 register) is read back and if it does not return [DLSV] on the downstream port of the link, then the remainder of this test is skipped (this is not a failure, but the test result is reported as skipped).
10. Test software writes 1 to the Link Autonomous Bandwidth Status field (Link Status register) on the downstream port of the link (to clear the status).
11. Test software writes 1 to the Retrain Link field (Link Control register) on the downstream port of the link using a WORD access, while preserving all the other fields in this register.
12. Test software reads the Link Training field (Link Status register) on the downstream port of the link until it reads 0. If it does not return 0 within 1 second, then report this as a link training failure, and terminate the test with a failure.
13. Test software reads the Link Capabilities register bits 3-0 value in the function under test and assigns it to Function under test Supported Speed Value [FSSV] and performs the following:
 a. If [FSSV] is 0000b, then the test terminates with failure.
 b. If [FSSV] is less than [USSV], then the test terminates with failure.
 c. If [FSSV] is less than [ULSV], then the test terminates with failure.
14. Test software reads the Current Link Speed field (Link Status register) in both the downstream port of the link and the function under test. Both values must return a value equal to one of the following two values: if [DLSV] <= [ULSV] then value is [DLSV]; if [DLSV] > [ULSV] then value is either [ULSV] or the lesser of ([DLSV], [USSV]), otherwise the test terminates with failure.
15. Test software reads the Link Bandwidth Notification Capability field (Link Capabilities register) on the downstream port of the link and if it returns 1, the following tests are performed:
 a. Test software reads the Link Autonomous Bandwidth Status field (Link Status register) on the downstream port of the link. If it returns 1, terminate the test with a failure.

16. Based on the value of [DLSV] one of the following is performed:
 a. If [DLSV] is 0001b:
 i. For Base 2.x testing: if [DSSV] is 0010b or greater, then set [DSTAGE] to 1, and set [DLSV] to 0010b.
 ii. For Base 3.x or later testing: if [DSSV] is 0001b, then set [DSTAGE] to 0, and set [DLSV] to 0001b.
 iii. For Base 3.x or later testing: if [DSSV] is 0010b or greater and [DSTAGE] is 0, then increment [DSTAGE] by 1 and set [DLSV] to 0010b.
 iv. For Base 3.x or later testing: if [DSSV] is 0011b or greater and [DSTAGE] is 4, then increment [DSTAGE] by 1 and set [DLSV] to 0011b.
 v. For Base 4.x or later testing: if [DSSV] is 0100b or greater and [DSTAGE] is 8, then increment [DSTAGE] by 1 and set [DLSV] to 0100b.
 b. If [DLSV] is 0010b:
 i. For Base 2.x testing: set [DSTAGE] to 0 and set [DLSV] to 0001b.
 ii. For Base 3.x or later testing: if [DSSV] is 0010b or less and [DSTAGE] is 1, then set [DSTAGE] to 0, and set [DLSV] to 0001b.
 iii. For Base 3.x or later testing: if [DSSV] is 0011b or greater and [DSTAGE] is 1, then increment [DSTAGE] by 1 and set [DLSV] to 0011b.
 iv. For Base 3.x or later testing: if [DSTAGE] is 3, then increment [DSTAGE] by 1 and set [DLSV] to 0001b.
 v. For Base 4.x or later testing: if [DSTAGE] is 10, then increment [DSTAGE] by 1 and set [DLSV] to 0100b.
 c. If [DLSV] is 0011b:
 i. For Base 3.x or later testing: if [DSTAGE] is 2, then increment [DSTAGE] by 1 and set [DLSV] to 0010b.
 ii. For Base 3.x testing: if [DSTAGE] is 5, then set [DSTAGE] to 0 and set [DLSV] to 0001b.
 iii. For Base 4.x or later testing: if [DSSV] is 0011b or less and [DSTAGE] is 5, then set [DSTAGE] to 0, and set [DLSV] to 0001b.
 iv. For Base 4.x or later testing: if DSSV] is 0100b or greater and [DSTAGE] is 5, then increment [DSTAGE] by 1 and set [DLSV] to 0100b.
 v. For Base 4.x or later testing: if [DSTAGE] is 7, then increment [DSTAGE] by 1 and set [DLSV] to 0001b.
 d. If [DLSV] is 0100b:
 i. For Base 4.x or later testing: if [DSTAGE] is 6, then increment [DSTAGE] by 1 and set [DLSV] to 0011b.
 ii. For Base 4.x or later testing: if [DSTAGE] is 9, then increment [DSTAGE] by 1 and set [DLSV] to 0010b.
 iii. For Base 4.x or later testing: if [DSTAGE] is 11, then set [DSTAGE] to 0 and set [DLSV] to 0001b.

17. Increment [ICNT] by 1.

18. Based on the value of [ICNT] the following are performed:
 a. If [ICNT] equals or is greater than 100, terminate the test and report the test results as follows:
 i. If [USSV] is less than or equal to [DSSV], report the test results, without modification.

ii. If [USSV] is greater than [DSSV], report any individual failing test results, otherwise if there are no failures, the overall test result is reported as skipped.

b. If [ICNT] is less than 100, repeat steps 5-18.

The test *fails* if:

- The function under test fails to respond to any part of the standard configuration sequence.
- Link training fails to complete within 1 second of a test software initiated link retrain.
- The function under test is connected to an upstream port, but it reports a Max Link Speed/Supported Link Speeds field of 0000b.
- If the function under test is connected to an upstream port, is not function 0, but function 0 in the same multi-function device reports a Max Link Speed/Supported Link Speeds field of 0000b.
- If the function under test is function 0 and it reports a Max Link Speed/Supported Link Speeds field greater than 0001b and its Target Link Speed field cannot be written with the value reported in the Max Link Speed/Supported Link Speeds field.
- If the function under test is not function 0 and function 0 in the same multi-function device reports a Max Link Speed/Supported Link Speeds field greater than 0001b, and function 0's Target Link Speed field cannot be written with the value reported in the Max Link Speed/Supported Link Speeds field.
- The Current Link Speed in both the upstream port and the downstream port does not match the expected link speed in any case.
- The Link Autonomous Bandwidth Status in the downstream port returns 1 in any case.

2.3.7. TD_2_8 Supported Link Width (Upstream Ports)

The test verifies that the function under test can function at the correct link speed when hardware attempts to configure the function under test with the supported link width as defined in the relevant specifications. The test can be run with or without a mechanical adapter in the system slot to control the achievable link width. The test requires the Achievable Link Width selection to indicate the link width and in order to successfully complete this test, the function under test must be able to pass at that link width.

The test only runs if the downstream port reports a PCI Express Capability Version of 2h or greater.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on upstream ports of PCI Express Endpoints, Legacy Endpoints, Switch Upstream Ports, and PCI Express to PCI/PCI-X Bridges.

Starting Configuration

Function under test is completely uninitialized following a reset.

Overview of Test Steps

Test software performs the following steps:

1. In manual mode, prompt the user for the Achievable Link Width selection.
2. Set the tested Link Width Value [LWV] to 00 0001b (x1).
3. Set the tested Link Speed Value [LSV] to 0001b (2.5 GT/s). In manual mode, if the Achievable Link Width selection has not yet been obtained, prompt the user and ask if the function under test is connected to a x1 link. In automatic mode, check the specified parameter to see the Achieveable Link Width selection for the function under test. (If the slot has a link that contains more than 1 physical lane, it is necessary to restrict the lane width to x1 by placing a x16 to x1 mechanical adaptor in the system slot. All lanes except the configured width for the test are not terminated during the test case.) If the Achieveable Link Width selection is not x1, or the user response to x1 is NO, then skip this part of the test (this is not a failure) and continue the test at step 12.
4. Configure the function under test following procedure described in Section 2.1.1.
5. Set the link speed to [LSV], following the appropriate procedures described in Sections 2.1.2.12 to 2.1.2.15.
6. Test software reads the Current Link Speed field (Link Status register) in both the function under test and the immediate upstream device's port (the downstream port of the link connected to the function under test). This port will be referred to as the downstream port of the link. The values must return [LSV], if both sides support that link speed. If not, this is recorded as a failure and the test terminates.
7. Test software reads the Negotiated Link Width field (Link Status register) in both the downstream port of the link and the function under test. The values must return [LWV]. If not, this is recorded as a failure and the test terminates.
8. Repeat steps 4-7 for 100 iterations.
9. For Base 2.x or later testing: if both the downstream port of the link and the function under test report Max Link Speed/Supported Link Speeds (Link Capabilities register) of 0010b or greater (it is capable of 5.0 GT/s operation) then set the tested Link Speed Value [LSV] to 0010b (5.0 GT/s) and repeat steps 4-8.
10. For Base 3.x or later testing: if both the downstream port of the link and the function under test report Max Link Speed/Supported Link Speeds (Link Capabilities register) of 0011b or greater (it is capable of 8.0 GT/s operation) then set the tested Link Speed Value [LSV] to 0011b (8.0 GT/s) and repeat steps 4-8.
11. For Base 4.x or later testing: if both the downstream port of the link and the function under test report Max Link Speed/Supported Link Speeds (Link Capabilities register) of 0100b or greater (it is capable of 16.0 GT/s operation) then set the tested Link Speed Value [LSV] to 0100b (16.0 GT/s) and repeat steps 4-8.
12. Set the tested Link Width Value [LWV] to 00 0010b (x2).
 a. If the function under test reports Maximum Link Width field (Link Capabilities register) less than [LWV], terminate the test (this is not a failure).
 b. If the downstream port of the link reports Maximum Link Width field (Link Capabilities register) less than [LWV], terminate the test (this is not a failure).

c. Set the tested Link Speed Value [LSV] to 0001b (2.5 GT/s). In manual mode, if the Achievable Link Width selection has not yet been obtained, prompt the user and ask if the function under test is connected to a x2 link. In automatic mode, check the specified parameter to see the Achieveable Link Width selection for the function under test. (If the slot has a link that contains more than 2 physical lanes, it is necessary to restrict the lane width to x2 by placing a x16 to x2 mechanical adaptor in the system slot. All lanes except the configured width for the test are not terminated during the test case.) If the Achieveable Link Width selection is not x2, or the user response to x2 is NO, then skip this part of the test (this is not a failure) and continue the test at step 13.
d. Repeat steps 4-11, with the following exception. For the first iteration only if the test fails to establish a link at the desired [LWV], then skip this part of the test (this is not a failure) and continue the test at step 13. Note: Since x2 support is optional, a port may not support this link width, but if it does support this link width, it must be able to train to it for each iteration attempt, otherwise this is recorded as a failure and the test terminates.

13. Set the tested Link Width Value [LWV] to 00 0100b (x4).
 a. If the function under test reports Maximum Link Width field (Link Capabilities register) less than [LWV], terminate the test (this is not a failure).
 b. If the downstream port of the link reports Maximum Link Width field (Link Capabilities register) less than [LWV], terminate the test (this is not a failure).
 c. Set the tested Link Speed Value [LSV] to 0001b (2.5 GT/s). In manual mode, if the Achievable Link Width selection has not yet been obtained, prompt the user and ask if the function under test is connected to a x4 link. In automatic mode, check the specified parameter to see the Achieveable Link Width selection for the function under test. (If the slot has a link that contains more than 4 physical lanes, it is necessary to restrict the lane width to x4 by placing a x16 to x4 mechanical adaptor in the system slot. All lanes except the configured width for the test are not terminated during the test case.) If the Achieveable Link Width selection is not x4, or the user response to x4 is NO, then skip this part of the test (this is not a failure) and continue the test at step 14.
 d. Repeat steps 4-11.
14. Set the tested Link Width Value [LWV] to 00 1000b (x8).
 a. If the function under test reports Maximum Link Width field (Link Capabilities register) less than [LWV], terminate the test (this is not a failure).
 b. If the downstream port of the link reports Maximum Link Width field (Link Capabilities register) less than [LWV], terminate the test (this is not a failure).
 c. Set the tested Link Speed Value [LSV] to 0001b (2.5 GT/s). In manual mode, if the Achievable Link Width selection has not yet been obtained, prompt the user and ask if the function under test is connected to a x8 link. In automatic mode, check the specified parameter to see the Achieveable Link Width selection for the function under test. (If the slot has a link that contains more than 8 physical lanes, it is necessary to restrict the lane width to x8 by placing a x16 to x8 mechanical adaptor in the system slot. All lanes except the configured width for the test are not terminated during the test case.) If the Achieveable Link Width selection is not x8, or the user response to x8 is NO, then skip this part of the test (this is not a failure) and continue the test at step 15.
 d. Repeat steps 4-11.
15. Set the tested Link Width Value [LWV] to 00 1100b (x12).

a. If the function under test reports Maximum Link Width field (Link Capabilities register) less than [LWV], terminate the test (this is not a failure).
b. If the downstream port of the link reports Maximum Link Width field (Link Capabilities register) less than [LWV], terminate the test (this is not a failure).
c. Set the tested Link Speed Value [LSV] to 0001b (2.5 GT/s). In manual mode, if the Achievable Link Width selection has not yet been obtained, prompt the user and ask if the function under test is connected to a x12 link. In automatic mode, check the specified parameter to see the Achieveable Link Width selection for the function under test. (If the slot has a link that contains more than 12 physical lanes, it is necessary to restrict the lane width to x12 by placing a x16 to x12 mechanical adaptor in the system slot. All lanes except the configured width for the test are not terminated during the test case.) If the Achieveable Link Width selection is not x12, or the user response to x12 is NO, then skip this part of the test (this is not a failure) and continue the test at step 16.
d. Repeat steps 4-11, with the following exception. For the first iteration only if the test fails to establish a link at the desired [LWV], then skip this part of the test (this is not a failure) and continue the test at step 16. Note: Since x12 support is optional, a port may not support this link width, but if it does support this link width, it must be able to train to it for each iteration attempt, otherwise this is recorded as a failure and the test terminates.

16. Set the tested Link Width Value [LWV] to 01 0000b (x16).
 a. If the function under test reports Maximum Link Width field (Link Capabilities register) less than [LWV], terminate the test (this is not a failure).
 b. If the downstream port of the link reports Maximum Link Width field (Link Capabilities register) less than [LWV], terminate the test (this is not a failure).
 c. Set the tested Link Speed Value [LSV] to 0001b (2.5 GT/s). In manual mode, if the Achievable Link Width selection has not yet been obtained, prompt the user and ask if the function under test is connected to a x16 link. In automatic mode, check the specified parameter to see the Achieveable Link Width selection for the function under test. If the Achieveable Link Width selection is not x16, or the user response to x16 is NO, then skip this part of the test (this is not a failure).
 d. Repeat steps 4-11.

The test *fails* if:

- The function under test fails to respond to any part of the standard configuration sequence.
- The Current Link Speed does not match the expected link speed in any case.
- The Negotiated Link Width does not match the expected link width in any case.

2.3.8. TD_2_12 Non-ARI Upstream Ports Support Non-Zero Device Number

The test verifies that if the function under test is part of a non-ARI device, then it will respond to Type 0 configuration accesses to any Device Number as required in the relevant specifications. (This test requires a downstream port that implements ARI Forwarding to be connected to the function under test's upstream port. It utilizes the requirement that a downstream port with ARI Forwarding enabled allows Type 0 configuration cycles to non-zero Device Numbers to be sent downstream.)

Relevant Specifications

- *PCI Express Base Specification*
- *ECN Alternate Routing-ID Interpretation (to Base 2.0 and Base 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on upstream ports of PCI Express Endpoints, Legacy Endpoints, Switch Upstream Ports, and PCI Express to PCI/PCI-X Bridges.

Starting Configuration

Function under test is completely uninitialized following a reset.

Overview of Test Steps

Test software performs the following steps:

1. Test software checks that the immediate upstream device's port (the downstream port of the link connected to the function under test) reports the Capability Version field (PCI Express Capabilities register) is 2h or greater. If not, the test terminates (this is not a failure and the test result is reported as skipped). This port will be referred to as the downstream port of the link.
2. Test software checks that the downstream port of the link reports the ARI Forwarding Supported field (Device Capabilities 2 register) as 1. If not, the test terminates (this is not a failure and the test result is reported as skipped).
3. Test software reads the ARI Forwarding Enable field (Device Control 2 register) on the downstream port of the link, and saves its value for later restoration.
4. Test software programs the ARI Forwarding Enable field (Device Control 2 register) to 0 on the downstream port of the link.
5. Create a 16 bit value of Bus number/Device number/Function number [BDF] as follows: bits 15-8 = downstream port of the link's Secondary Bus Number value; bits 7-3 = 00000b; bits 2-0 = function under test's Function Number.
6. Test software issues a configuration read to the function at [BDF] for the WORD at location 00h (Vendor ID register) and it must return a value other than FFFFh. If it does not, the restoration described in step 11 is performed, and then the test terminates (this is not a failure and the test result is reported as skipped).
7. Test software checks that the function at [BDF] is a non-ARI device (by checking that it does not have an ARI Extended Capability). If it is an ARI device, the restoration described in step 11 is performed, and then the test terminates (this is not a failure and the test result is reported as skipped).
8. Test software programs the ARI Forwarding Enable field (Device Control 2 register) to 1 on the downstream port of the link.
9. Test software increments [BDF] by 8h (increments Device Number). If this causes the upper 8 bits of [BDF] to change (Device Number exceeds 1Fh), then skip to step 11.
10. Test software issues a configuration read to the function at [BDF] for the WORD at location 00h (Vendor ID register) and it must return a value other than FFFFh. If it does then repeat

steps 9-10. If it does not, this is recorded as a failure, the restoration described in step 11 is performed, and then the test terminates.

11. Test software programs the ARI Forwarding Enable field (Device Control 2 register) to the value saved in step 3 on the downstream port of the link. (This ensures that ARI functions will remain visible to other tests, and non-ARI functions will not be duplicated.)
12. For functions under test that have a link, the test is run at each of the following link speeds:
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- For any non-zero Device Number, the function under test returns a value of FFFFh (Unsupported Request response) when an attempt is made to read the Vendor ID of the function under test on the Secondary Bus Number value of the downstream port of the link (reading the Vendor ID of the function under test connected to the downstream port).

2.3.9. TD_2_9 Software Initiated 8.0 GT/s Link Equalization (Upstream Ports)

The test verifies that the function under test can function at the correct link speed when test software attempts to redo the Link Equalization procedure as defined in the relevant specifications. (The test initiates the Link Equalization procedure from the downstream port, but only if that downstream port supports 8.0 GT/s or greater. In order to pass, the test requires that the function under test support 8.0 GT/s or greater.)

The test will only run for Base 3.x or later testing and it will run for 100 iterations and if any single iteration fails the test will report a failure and stop.

(Note: The downstream port is required to attempt a speed change any time the Retrain Link field (Link Control register) is set to 1 and the current link speed is not equal to the Target Link Speed field. However, the actual negotiated link speed will be determined by the lowest Target Link Speed field of both the downstream port and upstream port.)

(Note: In using 8.0 GT/s, this test assumes that hardware initiated Link Equalization has already occurred once at that data rate and completed successfully.)

The test only runs if both the function under test and the downstream port device connected to the function under test, report a PCI Express Capability Version of 2h or greater.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on upstream ports of PCI Express Endpoints, Legacy Endpoints, Switch Upstream Ports, and PCI Express to PCI/PCI-X Bridges; that report support for 8.0 GT/s or greater.

Starting Configuration

Function under test is completely uninitialized following a reset.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Set Iteration Count [ICNT] to 0.
3. For this test, the immediate upstream device's port (the downstream port of the link connected to the function under test) will be referred to as the downstream port of the link. Downstream port Link Speed Value [DLSV] is used to control the link speed of the downstream port of the link.
4. For this test, function 0 of the device containing the function under test will be referred to as the upstream port of the link. Upstream port Link Speed Value [ULSV] is used to control the link speed of the upstream port of the link.
5. Test software reads a WORD from the Link Status 2 register of the upstream port of the link and checks that the Link Equalization Request 8.0 GT/s field returns 0 (i.e., initial link equalization was satisfactorily completed). If this field returns 1, terminate the test, however this is not considered a failure, but rather the test result is reported as skipped.
6. Test software writes a WORD to the Link Status 2 register of the upstream port of the link with the Link Equalization Request 8.0 GT/s field set to 1 (to clear the status).
7. Read the Link Capabilities register bits 3-0 value from the upstream port of the link and assign it to Upstream port Supported Speed Value [USSV] and perform the following:
 a. If [USSV] is 0010b or less, the test terminates with failure.
 b. If [USSV] is 0011b or greater, then set [ULSV] to [USSV].
8. The Target Link Speed field (Link Control 2 register) is set to [ULSV] on the upstream port of the link and then the following tests are performed:
 a. If [USSV] is 0001b: the same Target Link Speed field is read back, and if it does not return [ULSV] or 0000b, the test terminates with failure.
 b. If [USSV] is greater than 0001b: the same Target Link Speed field is read back, and if it does not return [ULSV], the test terminates with failure.
9. Read the Link Capabilities register bits 3-0 value from the downstream port of the link and assign it to Downstream port Supported Speed Value [DSSV] and perform the following:
 a. If [DSSV] is 0010b or less, terminate the test, however this is not considered a failure, but rather the test result is reported as skipped.
 b. If [DSSV] is 0011b or greater, then set [DLSV] to 0011b.
10. Test software writes 1 to the Perform Equalization field (Link Control 3 register) on the downstream port of the link.
11. The Target Link Speed field (Link Control 2 register) is set to [DLSV] on the downstream port of the link.
12. The Target Link Speed field (Link Control 2 register) is read back and if it does not return [DLSV] on the downstream port of the link, then the remainder of this test is skipped (this is not a failure, but the test result is reported as skipped).

13. Test software writes 1 to the Link Autonomous Bandwidth Status field (Link Status register) on the downstream port of the link (to clear the status).
14. Test software writes 1 to the Retrain Link field (Link Control register) on the downstream port of the link using a WORD access, while preserving all the other fields in this register.
15. Test software reads the Link Training field (Link Status register) on the downstream port of the link until it reads 0. If it does not return 0 within 1 second, then report this as a link training failure, and terminate the test with a failure.
16. Test software reads the Link Capabilities register bits 3-0 value in the function under test and assigns it to Function under test Supported Speed Value [FSSV] and performs the following:
 a. If [FSSV] is 0000b, then the test terminates with failure.
 b. If [FSSV] is less than [USSV], then the test terminates with failure.
 c. If [FSSV] is less than [ULSV], then the test terminates with failure.
17. Test software reads the Current Link Speed field (Link Status register) in both the downstream port of the link and the function under test. Both values must return a value equal to one of the following two values: if [DLSV] <= [ULSV] then value is [DLSV]; if [DLSV] > [ULSV] then value is either [ULSV] or the lesser of ([DLSV], [USSV]), otherwise the test result is as follows. If both the returned values are correct, the common returned value is assigned to the Current Link Speed Value [CLSV].
 a. If the test result was incorrect because both values of the current link speed are not as expected and the test was run starting at a link speed of 8.0 GT/s or greater, then the test terminates with failure.
 b. If the test result was incorrect because both values of the current link speed are not as expected and the test was run starting at a link speed of less than 8.0 GT/s, then the test terminates and a warning message is issued, but this is not treated in itself as a failure.
18. Test software reads the Link Bandwidth Notification Capability field (Link Capabilities register) on the downstream port of the link and if it returns 1, the following checks are performed:
 a. Test software reads the Link Autonomous Bandwidth Status field (Link Status register) on the downstream port of the link. If it returns 1, terminate the test with a failure.
19. Test software reads the Link Status 2 register in the upstream port of the link and performs the following checks and if any are not as stated, this is recorded as a failure and the test terminates:
 a. If [CLSV] is 0011b:
 i. The Equalization 8.0 GT/s Complete field must be 1.
 ii. The Equalization 8.0 GT/s Phase 1 Successful field must be 1.
 iii. If the Equalization 8.0 GT/s Phase 2 Successful field returns 0, then the Equalization 8.0 GT/s Phase 3 Successful field must be 0.
 iv. If the Equalization 8.0 GT/s Phase 3 Successful field returns 1, then the Equalization 8.0 GT/s Phase 2 Successful field must be 1.
 v. The Link Equalization Request 8.0 GT/s field must be 0.
 b. If [CLSV] is 0010b or less and [USSV] is 0010b or less:
 i. The Equalization 8.0 GT/s Complete field must be 0.
 ii. The Equalization 8.0 GT/s Phase 1 Successful field must be 0.
 iii. The Equalization 8.0 GT/s Phase 2 Successful field must be 0.
 iv. The Equalization 8.0 GT/s Phase 3 Successful field must be 0.
 v. The Link Equalization Request 8.0 GT/s field must be 0.

20. Increment [ICNT] by 1.
21. Based on the value of [ICNT] the following are performed:
 a. If [ICNT] equals or is greater than 100, terminate the test and report the test results.
 b. If [ICNT] is less than 100, repeat steps 6-21.
22. For functions under test that have a link, the test is run at each of the following link speeds:
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- ❑ The function under test fails to respond to any part of the standard configuration sequence.
- ❑ Link training fails to complete within 1 second of a test software initiated link retrain.
- ❑ The function under test initially reports a Max Link Speed/Supported Link Speeds field of 0011b or greater, but later reports a Max Link Speed/Supported Link Speeds field less than 0011b, or its Target Link Speed field cannot be written with a value of 0011b.
- ❑ If the function under test is connected to an upstream port, is not function 0, but function 0 in the same multi-function device reports a Max Link Speed/Supported Link Speeds field of 0000b.
- ❑ If the function under test is function 0 and it reports a Max Link Speed/Supported Link Speeds field greater than 0001b and its Target Link Speed field cannot be written with the value reported in the Max Link Speed/Supported Link Speeds field.
- ❑ If the function under test is not function 0 and function 0 in the same multi-function device reports a Max Link Speed/Supported Link Speeds field greater than 0001b, and function 0's Target Link Speed field cannot be written with the value reported in the Max Link Speed/Supported Link Speeds field.
- ❑ The Current Link Speed field in both the upstream port and the downstream port does not match the expected link speed in any case.
- ❑ The Link Autonomous Bandwidth Status field in the downstream port returns 1 in any case.
- ❑ The link speed following retrain is 8.0 GT/s and all of the following fields do not return 1 in function 0 of the device under test: Equalization 8.0 GT/s Complete; Equalization 8.0 GT/s Phase 1 Successful.
- ❑ The link speed following retrain is 8.0 GT/s and Equalization 8.0 GT/s Phase 3 Successful field returns 1 in function 0 of the device under test: but the Equalization 8.0 GT/s Phase 2 Successful field does not return 1 in function 0 of the device under test. (Since the downstream port may skip both Phase 2 and Phase 3 during any equalization, the Equalization 8.0 GT/s Phase 2 Successful field and the Equalization 8.0 GT/s Phase 3 Successful field must either both be set or both be clear for a successful equalization.)
- ❑ The link speed following retrain is not 8.0 GT/s and all of the following fields do not return 0 in function 0 of the device under test: Equalization 8.0 GT/s Complete; Equalization 8.0 GT/s Phase 1 Successful; Equalization 8.0 GT/s Phase 2 Successful; Equalization 8.0 GT/s Phase 3 Successful.

- The Link Equalization Request 8.0 GT/s field returns 1 in function 0 of the device under test following a link retrain.

The test *warns* if:

- When starting at an initial link speed less than 8.0 GT/s, the function under test fails to participate in a request to perform link equalization.

2.3.10. TD_2_10 Software Initiated 16.0 GT/s Link Equalization (Upstream Ports)

The test verifies that the function under test can function at the correct link speed when test software attempts to redo the Link Equalization procedure as defined in the relevant specifications. (The test initiates the Link Equalization procedure from the downstream port, but only if that downstream port supports 16.0 GT/s or greater. In order to pass, the test requires that the function under test support 16.0 GT/s or greater.)

The test will only run for Base 4.x or later testing and it will run for 100 iterations and if any single iteration fails the test will report a failure and stop.

(Note: The downstream port is required to attempt a speed change any time the Retrain Link field (Link Control register) is set to 1 and the current link speed is not equal to the Target Link Speed field. However, the actual negotiated link speed will be determined by the lowest Target Link Speed field of both the downstream port and upstream port.)

(Note: In using 16.0 GT/s, this test assumes that hardware initiated Link Equalization has already occurred once at that data rate and completed successfully.)

The test only runs if both the function under test and the downstream port device connected to the function under test, report a PCI Express Capability Version of 2h or greater.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on upstream ports of PCI Express Endpoints, Legacy Endpoints, Switch Upstream Ports, and PCI Express to PCI/PCI-X Bridges; that report support for 16.0 GT/s or greater.

Starting Configuration

Function under test is completely uninitialized following a reset.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Set Iteration Count [ICNT] to 0.
3. For this test, the immediate upstream device's port (the downstream port of the link connected to the function under test) will be referred to as the downstream port of the link. Downstream port Link Speed Value [DLSV] is used to control the link speed of the downstream port of the link.

4. For this test, function 0 of the device containing the function under test will be referred to as the upstream port of the link. Upstream port Link Speed Value [ULSV] is used to control the link speed of the upstream port of the link.
5. Test software reads a DWORD from the 16.0 GT/s Status register of the upstream port of the link and checks that the Link Equalization Request 16.0 GT/s field returns 0 (i.e., initial link equalization was satisfactorily completed). If this field returns 1, terminate the test, however this is not considered a failure, but rather the test result is reported as skipped.
6. Test software writes a DWORD to the 16.0 GT/s Status register of the upstream port of the link with the Link Equalization Request 16.0 GT/s field set to 1 (to clear the status).
7. Read the Link Capabilities register bits 3-0 value from the upstream port of the link and assign it to Upstream port Supported Speed Value [USSV] and perform the following:
 a. If [USSV] is 0011b or less, the test terminates with failure.
 b. If [USSV] is 0100b or greater, then set [ULSV] to [USSV].
8. The Target Link Speed field (Link Control 2 register) is set to [ULSV] on the upstream port of the link and then the following tests are performed:
 a. If [USSV] is 0001b: the same Target Link Speed field is read back, and if it does not return [ULSV] or 0000b, the test terminates with failure.
 b. If [USSV] is greater than 0001b: the same Target Link Speed field is read back, and if it does not return [ULSV], the test terminates with failure.
9. Read the Link Capabilities register bits 3-0 value from the downstream port of the link and assign it to Downstream port Supported Speed Value [DSSV] and perform the following:
 a. If [DSSV] is 0011b or less, terminate the test, however this is not considered a failure, but rather the test result is reported as skipped.
 b. If [DSSV] is 0100b or greater, then set [DLSV] to 0100b.
10. Test software writes 1 to the Perform Equalization field (Link Control 3 register) on the downstream port of the link.
11. The Target Link Speed field (Link Control 2 register) is set to [DLSV] on the downstream port of the link.
12. The Target Link Speed field (Link Control 2 register) is read back and if it does not return [DLSV] on the downstream port of the link, then the remainder of this test is skipped (this is not a failure, but the test result is reported as skipped).
13. Test software writes 1 to the Link Autonomous Bandwidth Status field (Link Status register) on the downstream port of the link (to clear the status).
14. Test software writes 1 to the Retrain Link field (Link Control register) on the downstream port of the link using a WORD access, while preserving all the other fields in this register.
15. Test software reads the Link Training field (Link Status register) on the downstream port of the link until it reads 0. If it does not return 0 within 1 second, then report this as a link training failure, and terminate the test with a failure.
16. Test software reads the Link Capabilities register bits 3-0 value in the function under test and assigns it to Function under test Supported Speed Value [FSSV] and performs the following:
 a. If [FSSV] is 0000b, then the test terminates with failure.
 b. If [FSSV] is less than [USSV], then the test terminates with failure.

c. If [FSSV] is less than [ULSV], then the test terminates with failure.

17. Test software reads the Current Link Speed field (Link Status register) in both the downstream port of the link and the function under test. Both values must return a value equal to one of the following two values: if [DLSV] <= [ULSV] then value is [DLSV]; if [DLSV] > [ULSV] then value is either [ULSV] or the lesser of ([DLSV], [USSV]), otherwise the test result is as follows. If both the returned values are correct, the common returned value is assigned to the Current Link Speed Value [CLSV].
 a. If the test result was incorrect because both values of the current link speed are not as expected and the test was run starting at a link speed of 16.0 GT/s or greater, then the test terminates with failure.
 b. If the test result was incorrect because both values of the current link speed are not as expected and the test was run starting at a link speed of less than 16.0 GT/s, then the test terminates and a warning message is issued, but this is not treated in itself as a failure.
18. Test software reads the Link Bandwidth Notification Capability field (Link Capabilities register) on the downstream port of the link and if it returns 1, the following checks are performed:
 a. Test software reads the Link Autonomous Bandwidth Status field (Link Status register) on the downstream port of the link. If it returns 1, terminate the test with a failure.
19. Test software reads the 16.0 GT/s Status register in the upstream port of the link and performs the following checks and if any are not as stated, this is recorded as a failure and the test terminates:
 a. If [CLSV] is 0100b:
 i. The Equalization 16.0 GT/s Complete field must be 1.
 ii. The Equalization 16.0 GT/s Phase 1 Successful field must be 1.
 iii. If the Equalization 16.0 GT/s Phase 2 Successful field returns 0, then the Equalization 16.0 GT/s Phase 3 Successful field must be 0.
 iv. If the Equalization 16.0 GT/s Phase 3 Successful field returns 1, then the Equalization 16.0 GT/s Phase 2 Successful field must be 1.
 v. The Link Equalization Request 16.0 GT/s field must be 0.
 b. If [CLSV] is 0011b or less and [USSV] is 0011b or less:
 i. The Equalization 16.0 GT/s Complete field must be 0.
 ii. The Equalization 16.0 GT/s Phase 1 Successful field must be 0.
 iii. The Equalization 16.0 GT/s Phase 2 Successful field must be 0.
 iv. The Equalization 16.0 GT/s Phase 3 Successful field must be 0.
 v. The Link Equalization Request 16.0 GT/s field must be 0.
20. Increment [ICNT] by 1.
21. Based on the value of [ICNT] the following are performed:
 a. If [ICNT] equals or is greater than 100, terminate the test and report the test results.
 b. If [ICNT] is less than 100, repeat steps 6-21.
22. For functions under test that have a link, the test is run at each of the following link speeds:
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- The function under test fails to respond to any part of the standard configuration sequence.
- Link training fails to complete within 1 second of a test software initiated link retrain.
- The function under test initially reports a Max Link Speed/Supported Link Speeds field of 0100b or greater, but later reports a Max Link Speed/Supported Link Speeds field less than 0100b, or its Target Link Speed field cannot be written with a value of 0100b.
- If the function under test is connected to an upstream port, is not function 0, but function 0 in the same multi-function device reports a Max Link Speed/Supported Link Speeds field of 0000b.
- If the function under test is function 0 and it reports a Max Link Speed/Supported Link Speeds field greater than 0001b and its Target Link Speed field cannot be written with the value reported in the Max Link Speed/Supported Link Speeds field.
- If the function under test is not function 0 and function 0 in the same multi-function device reports a Max Link Speed/Supported Link Speeds field greater than 0001b, and function 0's Target Link Speed field cannot be written with the value reported in the Max Link Speed/Supported Link Speeds field.
- The Current Link Speed field in both the upstream port and the downstream port does not match the expected link speed in any case.
- The Link Autonomous Bandwidth Status field in the downstream port returns 1 in any case.
- The link speed following retrain is 16.0 GT/s and all of the following fields do not return 1 in function 0 of the device under test: Equalization 16.0 GT/s Complete; Equalization 16.0 GT/s Phase 1 Successful.
- The link speed following retrain is 16.0 GT/s and Equalization 16.0 GT/s Phase 3 Successful field returns 1 in function 0 of the device under test: but the Equalization 16.0 GT/s Phase 2 Successful field does not return 1 in function 0 of the device under test. (Since the downstream port may skip both Phase 2 and Phase 3 during any equalization, the Equalization 16.0 GT/s Phase 2 Successful field and the Equalization 16.0 GT/s Phase 3 Successful field must either both be set or both be clear for a successful equalization.)
- The link speed following retrain is not 16.0 GT/s and all of the following fields do not return 0 in function 0 of the device under test: Equalization 16.0 GT/s Complete; Equalization 16.0 GT/s Phase 1 Successful; Equalization 16.0 GT/s Phase 2 Successful; Equalization 16.0 GT/s Phase 3 Successful.
- The Link Equalization Request 16.0 GT/s field returns 1 in function 0 of the device under test following a link retrain.

The test *warns* if:

- When starting at an initial link speed less than 16.0 GT/s, the function under test fails to participate in a request to perform link equalization.

Configuration Register Tests (Devices with Downstream Ports)

This set of tests applies only to downstream ports of Root Ports, Switches, and Bridges.

2.3.11. TD_3_1 Slot Capabilities, Slot Control, and Slot Status Registers (PCIe Cap Ver = 1)

The test verifies that if the function under test reports support for a Slot Connector, it implements the Slot Capabilities, Slot Control, and Slot Status registers as defined in the relevant specifications.

The test only runs on a downstream port or a Root Complex Event Collector, that reports a PCI Express Capability Version of 1h. For a downstream port if the Slot Implemented field is 0 the Slot Capabilities, Slot Control, and Slot Status registers must be hardwired to 0 except for the Presence Detect State field in the Slot Status register which must be hardwired to 1.

Relevant Specifications

- *PCI Express Base Specification, Revision 1.1 only*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on downstream ports of Root Ports, Switch Downstream Ports, PCI/PCI-X to PCI Express Bridges, and Root Complex Event Collectors.

Starting Configuration

For a non-Root Port function under test, it is completely uninitialized following a reset, except that the bus number fields are initialized with valid numbers.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Capability ID field for each of the function's Capability structures. Determine how many instances of the Capability ID of 10h (PCI Express Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Capability ID of 10h is not found in a Capability structure, the test terminates with a failure.
4. If the Capability ID of 10h is found in a Capability structure, read a WORD located at offset 02h in the PCI Express Capability structure and if the Capability Version field is equal or greater than 2h, the test terminates (this is not a failure and the test result is reported as skipped).
5. For Base 2.x or later testing: if the Capability ID of 10h is found in a Capability structure and if the Capability Version field is equal or less than 1h, then the test terminates and reports a failure.
6. For Base 1.x testing: if the Capability ID of 10h is found in a Capability structure and if the Capability Version field is equal or less than 1h, the following tests are performed on that Capability structure:
7. If the Slot Implemented field is 0, then skip to step 12.

8. Read the DWORD located at offset 14h (Slot Capabilities register) in the PCI Express Capability structure.
9. If the Attention Indicator Present field returns 1, then the following tests are performed:
 a. Test software writes the Attention Indicator Control field with 01b.
 b. If the No Command Completed Support field (Slot Capabilities register) is 0:
 i. Test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then steps a-b are repeated. If this still does not occur after 10 repeats, this part of the test terminates with a test failure and the test continues at step 10. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status).
 c. Test software reads the Attention Indicator Control field and checks that it returns the value previously written. If not, this part of the test terminates with a test failure and the test continues at step 10.
 d. Repeat steps a-c using the Attention Indicator Control field data values as follows: 10b; 11b.
 e. Perform a default value check on the Attention Indicator Control field and confirm that it returns one of the allowed default values (01b, 10b, or 11b). If not, this is recorded as a failure, but the test continues.
10. If the Power Indicator Present field returns 1, then the following tests are performed:
 a. Test software writes the Power Indicator Control field with 01b.
 b. If the No Command Completed Support field (Slot Capabilities register) is 0:
 i. Test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then steps a-b are repeated. If this still does not occur after 10 repeats, this part of the test terminates with a test failure and the test continues at step 11. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status).
 c. Test software reads the Power Indicator Control field and checks that it returns the value previously written. If not, this part of the test terminates with a test failure and the test continues at step 11.
 d. Repeat steps a-c using the Power Indicator Control field data values as follows: 10b; 11b.
 e. Perform a default value check on the Power Indicator Control field and confirm that it returns one of the allowed default values (01b, 10b, or 11b). If not, this is recorded as a failure, but the test continues.
11. If the Power Controller Implemented field returns 1, then the following tests are performed:
 a. Test software writes the Power Controller Control field with 0.
 b. If the No Command Completed Support field (Slot Capabilities register) is 0:
 i. Test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then steps a-b are repeated. If this still does not occur after 10 repeats, this part of the test terminates with a test failure and the test continues at step 12. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status).
 c. Test software reads the Power Controller Control field and checks that it returns the value previously written. If not, this part of the test terminates with a test failure and the test continues at step 12.

d. Test software reads the Power Fault Detected field (Slot Status register) and checks that it returns 0. If not, this part of the test terminates with a test failure and the test continues at step 12.
(Note: Power Controller Control field data value 1 is not tested, as this would power down the hot-plug slot. There is no intention in this test to remove power from any card in any slot.)

12. The following register field characteristic checks are performed:

Slot Capabilities Register (Offset 14h) – DWORD

(for Downstream Ports with Slot Implemented as 1)

a. Attention Button Present	HwInit
b. Power Controller Present	HwInit
c. MRL Sensor Present	HwInit
d. Attention Indicator Present	HwInit
e. Power Indicator Present	HwInit
f. Hot-Plug Surprise	HwInit
g. Hot-Plug Capable	HwInit
h. Slot Power Limit Value	HwInit
i. Slot Power Limit Scale	HwInit
j. Electromechanical Interlock Present	HwInit
k. No Command Completed Support	HwInit
l. Physical Slot Number	HwInit

Slot Capabilities Register (Offset 14h) — DWORD

(for Root Ports with Slot Implemented as 0 or RC Event Collectors)

a. RsvdP_31-0	RO-Zero

Slot Control Register (Offset 18h) — WORD

(for Downstream Ports with Slot Implemented as 1)

a. Attention Button Pressed Enable	
(if Attention Button Present is 1)	RW
(if Attention Button Present is 0)	RW or RO-Zero
b. Power Fault Detected Enable	RW or RO-Zero
c. MRL Sensor Changed Enable	
(if MRL Sensor Present is 1)	RW
(if MRL Sensor Present is 0)	RW or RO-Zero
d. Presence Detect Changed Enable	
(if Hot-Plug Capable is 1)	RW
(if Hot-Plug Capable is 0)	RW or RO-Zero
e. Command Completed Interrupt Enable	
(if No Command Completed Support is 0)	RW
(if No Command Completed Support is 1)	RO-Zero
f. Hot-Plug Interrupt Enable	
(if Hot-Plug Capable is 1)	RW

(if Hot-Plug Capable is 0) RW or RO-Zero

g. Attention Indicator Control
(if Attention Indicator Present is 1 and No Command Completed Support is 1) RW
(if Attention Indicator Present is 0) RW or RO-Zero

h. Power Indicator Control
(if Power Indicator Present is 1 and No Command Completed Support is 1) RW
(if Power Indicator Present is 0) RW or RO-Zero

i. Power Controller Control
(if Power Controller Present is 1 and No Command Completed Support is 1) RW
Note: Writing Power Controller Control with 1 in a Downstream Port with a slot causes the slot to power off. The test should restore this field to 0 when completing testing of this register.

j. Electromechanical Interlock Control RO-Zero
Note: The Electromechanical Interlock Control field always returns 0 when read.

k. Data Link Layer State Changed Enable
(if Data Link Layer Link Active Reporting Capable is 1) RW
(if Data Link Layer Link Active Reporting Capable is 0) RW or RO-Zero

l. RsvdP_15-13 RO-Zero

Slot Control Register (Offset 18h) — WORD

(for Root Ports with Slot Implemented as 0 or RC Event Collectors)

a. RsvdP_15-0 RO-Zero

Slot Status Register (Offset 1Ah) — WORD

(for Downstream Ports with Slot Implemented as 1)

a. Attention Button Pressed
(if Attention Button Present is 1) RW1C
(if Attention Button Present is 0) RO-Zero

b. Power Fault Detected
(if Power Controller Present is 1) RW1C
(if Power Controller Present is 0) RO-Zero

c. MRL Sensor Changed
(if MRL Sensor Present is 1) RW1C
(if MRL Sensor Present is 0) RO-Zero

d. Presence Detect Changed RW1C
Note: The Presence Detect Changed field cannot be tested for default value on form factors that don't provide an out-of-band presence signal, as in-band presence will be cleared upon entry to Detect state, and will be updated with a fresh value upon exit from Detect state, which can result in a presence change.

e. Command Completed
(if No Command Completed Support is 0) RW1C
(if No Command Completed Support is 1) RO-Zero

f. MRL Sensor State RO
g. Presence Detect State RO
h. Electromechanical Interlock Status RO
i. Data Link Layer State Changed RW1C
j. RsvdZ_15-9 RO-Zero

Slot Status Register (Offset 1Ah) — WORD
(for Root Ports with Slot Implemented as 0)
a. RsvdZ_5-0 RO-Zero
b. Presence Detect State RO-Ones
c. RsvdZ_15-7 RO-Zero

Slot Status Register (Offset 1Ah) — WORD
(for RC Event Collectors)
a. RsvdP_15-0 RO-Zero

13. The following default value checks are performed:

Slot Control Register Default Value (Offset 18h) – WORD
(for Downstream Ports with Slot Implemented as 1)
a. Attention Button Pressed Enable 0
b. Power Fault Detected Enable 0
c. MRL Sensor Changed Enable 0
d. Presence Detect Changed Enable 0
e. Command Completed Interrupt Enable 0
f. Hot-Plug Interrupt Enable 0
g. Data Link Layer State Changed Enable 0

Slot Status Register Default Value (Offset 1Ah) – WORD
(for Downstream Ports with Slot Implemented as 1)
a. Attention Button Pressed 0
b. Power Fault Detected 0
c. MRL Sensor Changed 0
d. Command Completed 0

The test *fails* if:

- A PCI Express Capability structure is not present.
- More than one PCI Express Capability structure is present.
- Any of the slot related enable fields are set by default for a non-embedded slot (for Base 1.x testing only).
- Any of the slot status change/detect fields are set by default for a slot that has just been reset (for Base 1.x testing only).
- The No Command Completed Support field is 0, but the Command Completed field status does not return 1 within the time allowance after initiating a command.
- The Attention Indicator Present field is 1, but the Power Indicator Control field cannot be written with one of the valid values (for Base 1.x testing only).
- The Power Indicator Present field is 1, but the Power Indicator Control field cannot be written with one of the valid values (for Base 1.x testing only).

- The Power Controller Implemented field is 1, but the Power Controller Control field cannot be written with the ON value (0), or the Power Fault Detected field status returns 1 (for Base 1.x testing only).
- Any of the register field characteristic tests fail (for Base 1.x testing only).
- Any of the default value tests fail (for Base 1.x testing only).

2.3.12. TD_3_2 Root Capabilities, Root Control, and Root Status Registers (PCIe Cap Ver = 1)

The test verifies that if the function under test is a Root Port or a Root Complex Event Collector, it implements the Root Capabilities, Root Control, and Root Status registers as defined in the relevant specifications.

The test only runs on a downstream port or a Root Complex Event Collector, that reports a PCI Express Capability Version of 1h.

Relevant Specifications

- *PCI Express Base Specification, Revision 1.1 only*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on Root Ports and Root Complex Event Collectors.

Starting Configuration

For a non-Root Port function under test, it is completely uninitialized following a reset, except that the bus number fields are initialized with valid numbers.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Capability ID field for each of the function's Capability structures. Determine how many instances of the Capability ID of 10h (PCI Express Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Capability ID of 10h is not found in a Capability structure, the test terminates with a failure.
4. If the Capability ID of 10h is found in a Capability structure, read a WORD located at offset 02h in the PCI Express Capability structure and if the Capability Version field is equal or greater than 2h, the test terminates (this is not a failure and the test result is reported as skipped).
5. For Base 2.x or later testing: if the Capability ID of 10h is found in a Capability structure and if the Capability Version field is equal or less than 1h, then the test terminates and reports a failure.
6. For Base 1.x testing: if the Capability ID of 10h is found in a Capability structure and if the Capability Version field is equal or less than 1h, the following register field characteristic checks are performed on that Capability structure:

 Root Control Register (Offset 1Ch) — WORD
 (for Root Port or RC Event Collector)

a. System Error on Correctable Error Enable — RW
b. System Error on Non-Fatal Error Enable — RW
c. System Error on Fatal Error Enable — RW
d. PME Interrupt Enable — RW
e. CRS Software Visibility Enable
 (for Root Ports with CRS Software Visibility as 1) — RW
 (for Root Ports with CRS Software Visibility as 0) — RO-Zero
 (for RC Event Collectors) — RO-Zero
f. RsvdP_15-5 — RO-Zero

Root Capabilities Register (Offset 1Eh) — WORD
(for Root Port or RC Event Collector)
a. CRS Software Visibility
 (for Root Ports) — RO
 (for RC Event Collectors) — RO-Zero
b. RsvdP_15-1 — RO-Zero

Root Status Register (Offset 20h) — DWORD
(for Root Port or RC Event Collector)
a. PME Requester ID — RO
b. PME Status — RW1C
c. PME Pending — RO
d. RsvdZ_31-18 — RO-Zero

7. For Base 1.x testing: if the Capability ID of 10h is found in a Capability structure and if the Capability Version field is equal or less than 1h, the following default value checks are performed on that Capability structure:

Root Control Register (Offset 1Ch) — WORD
(for Root Port or RC Event Collector)
a. System Error on Correctable Error Enable — 0
b. System Error on Non-Fatal Error Enable — 0
c. System Error on Fatal Error Enable — 0
d. PME Interrupt Enable — 0
e. CRS Software Visibility Enable
 (for Root Ports) — 0

Root Status Register (Offset 20h) — DWORD
(for Root Port or RC Event Collector)
a. PME Status — 0

The test *fails* if:

- ❑ A PCI Express Capability structure is not present.
- ❑ More than one PCI Express Capability structure is present.
- ❑ Any of the register field characteristic tests fail (for Base 1.x testing only).
- ❑ Any of the default value tests fail (for Base 1.x testing only).

2.3.13. TD_3_15 ASPM Configuration Stress (Downstream Ports)

The test verifies that if the function under test implements ASPM, test software attempts to configure the function under test to a variety of different ASPM settings will not cause the device to operate abnormally, as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on downstream ports of Root Ports, Switch Downstream Ports, and PCI/PCI-X to PCI Express Bridges.

(Note: The immediate downstream device (the upstream port of the link connected to the function under test) must be known to operate correctly in each of its supported ASPM modes.)

Starting Configuration

For a non-Root Port function under test, it is completely uninitialized following a reset, except that the bus number fields are initialized with valid numbers.

The immediate downstream device (the upstream port of the link connected to the function under test) is completely uninitialized following a reset.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test and the immediate downstream device (the upstream port of the link connected to the function under test) following the procedure described in Section 2.1.1. If the procedure fails to complete successfully, the test terminates with failure.
2. Read the Active State Power Management (ASPM) Support field from the Link Capabilities register of the immediate downstream device (the upstream port of the link connected to the function under test) (this will also be referred to as the upstream port of the link). Record this value as Upstream ASPM [UASPMS].
3. Read the Active State Power Management (ASPM) Support field from the Link Capabilities register of the function under test, which will be referred to as the downstream port of the link. Record this value as Downstream ASPM [DASPMS].
4. Read the Retimer Presence Detect Supported field from the Link Capabilities 2 register of the function under test, and if the field's value is 0, then set [RTPSNT] to 0, but if the field's value is 1 then:
 a. Read the Retimer Presence Detected field from the Link Status 2 register of the function under test. Record this value in Retimer Present [RTPSNT].
5. If [RTPSNT] is 1, skip to step 1.
6. Read the Two Retimers Presence Detect Supported field from the Link Capabilities 2 register of the function under test, and if the field's value is 0, then set [RTPSNT] to 0, but if the field's value is 1 then:

a. Read the Two Retimers Presence Detected field from the Link Status 2 register of the function under test. Record this value in [RTPSNT].

7. Use the level of testing to determine the interpretation of the Active State Power Management (ASPM) Support field, and what values to write to the Active State Power Management (ASPM) Control field in the Link Control register of the upstream port of the link and the downstream port of the link. If the upstream port device is part of a multi-function device (the Multi-Function Device field of Header Type register is 1), then the same ASPM setting value must be written to all non-VF functions in that multi-function device. If [RTPSNT] is 1, then all [UASPMS] and [DASPMS] values are modified so that bit 0 of the Active State Power Management (ASPM) Control field is forced to 0b (L0s disabled).
 a. For Base 1.x testing: use Table 1 in Section 2.1.2.21.1, together with [UASPMS] and [DASPMS] to determine which ASPM combinations are supported, perform step 1 for each of the supported ASPM combinations in Table 1 in Section 2.1.2.21.1. If the total number of iterations is less than 100, repeat this entire step again.
 b. For Base 2.x or later testing: read the ASPM Optionality Compliance field from the Link Capabilities register in both the upstream port of the link and the downstream port of the link, and based on their reported values perform the following:
 i. If the ASPM Optionality Compliance field is 0 in both the upstream port of the link and the downstream port of the link, use Table 1 in Section 2.1.2.21.1, together with [UASPMS] and [DASPMS] to determine which ASPM combinations are supported, perform step 1 for each of the supported ASPM combinations in Table 1 in Section 2.1.2.21.1. If the total number of iterations is less than 100, repeat this entire step again.
 ii. If the ASPM Optionality Compliance field is 1 in the upstream port of the link and the ASPM Optionality Compliance field is 0 in the downstream port of the link, use Table 2 in Section 2.1.2.21.2, together with [UASPMS] and [DASPMS] to determine which ASPM combinations are supported, perform step 1 for each of the supported ASPM combinations in Table 2 in Section 2.1.2.21.2. If the total number of iterations is less than 100, repeat this entire step again.
 iii. If the ASPM Optionality Compliance field is 0 in the upstream port of the link and the ASPM Optionality Compliance field is 1 in the downstream port of the link, use Table 3 in Section 2.1.2.21.3, together with [UASPMS] and [DASPMS] to determine which ASPM combinations are supported, perform step 1 for each of the supported ASPM combinations in Table 3 in Section 2.1.2.21.3. If the total number of iterations is less than 100, repeat this entire step again.
 iv. If the ASPM Optionality Compliance field is 1 in both the upstream port of the link and the downstream port of the link, use Table 4 in Section 2.1.2.21.4, together with [UASPMS] and [DASPMS] to determine which ASPM combinations are supported, perform step 1 for each of the supported ASPM combinations in Table 4 in Section 2.1.2.21.4. If the total number of iterations is less than 100, repeat this entire step again.

8. For functions under test that have a link, the test is run at each of the following link speeds:
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- The immediate downstream device (the upstream port of the link connected to the function under test) fails to respond to any part of the standard configuration sequence.

2.3.14. TD_3_8 Link Retraining Stress (Downstream Ports)

The test verifies that the function under test implements the Retrain Link (Link Control register) behavior as defined in the relevant specifications and can properly perform link retraining when the Retrain Link field is set. The test prompts the user to populate the slot under test.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on downstream ports of Root Ports, Switch Downstream Ports, and PCI/PCI-X to PCI Express Bridges.

Starting Configuration

For a non-Root Port function under test, it is completely uninitialized following a reset, except that the bus number fields are initialized with valid numbers.

The immediate downstream device (the upstream port of the link connected to the function under test) is completely uninitialized following a reset.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test and the immediate downstream device (the upstream port of the link connected to the function under test) following the procedure described in Section 2.1.1. If the procedure fails to complete successfully, the test terminates with failure.
2. Modify some non-sticky register field in the immediate downstream device to a non-default value. Any of the following fields can be used as long as they are implemented as RW in the target: Memory Space Enable (Command register); I/O Space Enable (Command register); Bus Master Enable (Command register); Interrupt Disable (Command register). If none of these fields are implemented as RW in the target, then other non-sticky RW fields can be used. If test software cannot find any non-sticky RW field in the target, then this step is skipped.
3. Test software reads the Negotiated Link Width field (Link Status register) for both the function under test and the immediate downstream device and records the values. If the two values do not agree, then the test fails and is terminated.
4. Test software writes a 1 to the Retrain Link field (Link Control register) of the function under test using a WORD access, while preserving all the other fields in this register.
5. The function under test is checked to see if it has completed training. Test software continuously reads the Link Training field in the Link Status register, and when it returns 0, go to the next step. If the Link Training field does not return 0 within 1 second, then the test fails, and the remaining steps are skipped.

6. Test software reads the Negotiated Link Width field (Link Status register) for both the function under test and the immediate downstream device and records the values. If the two values do not agree, then the test fails and is terminated. If the value does not match the previously read value, then the test fails and is terminated.
7. If a non-sticky RW register field was found in step 2, test software verifies the same non-sticky field (from step 2) in the immediate downstream device is not reset to its default value. If the value has changed to the default value, the test fails and is terminated.
8. Steps 2-7 are repeated for 100 iterations.

The test *fails* if:

- The reported Negotiated Link Width of the upstream component fails to match the Negotiated Link Width of the downstream component.
- Link retraining causes the Negotiated Link Width to change.
- Link retraining causes the upstream port to reset (restoring default values).

2.3.15. TD_3_13 Secondary Bus Reset (Downstream Ports)

The test verifies that the function under test implements the Secondary Bus Reset (Bridge Control register) behavior as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *PCI Express to PCI/PCI-X Bridge Specification, Revision 1.0*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on downstream ports of Root Ports, Switch Downstream Ports, and PCI/PCI-X to PCI Express Bridges.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test and the immediate downstream device (the upstream port of the link connected to the function under test) following the procedure described in Section 2.1.1.
2. Verify that a device is present on the secondary side of the Bridge, or on the downstream port of the Switch, or on the downstream port of the Root Port. If not, the test terminates (this is not a failure and the test result is reported as skipped).
3. Modify some non-sticky register field in the device on the secondary side of the Bridge, or on the downstream port of the Switch, or on the downstream port of the Root Port. Any of the following fields can be used as long as they are implemented as RW in the target: Memory Space Enable (Command register); I/O Space Enable (Command register); Bus Master Enable

(Command register); Interrupt Disable (Command register). If none of these fields are implemented as RW in the target, then other non-sticky RW fields can be used. If test software cannot find any non-sticky RW field in the target, then this step is skipped.

4. A reset of the secondary interface is initiated by test software through writing a 1 to the Secondary Bus Reset field in the function under test (for a Bridge, the Bridge Control register in the Bridge; for a Switch, the Bridge Control register in the Switch Downstream Port; for a Root Port, the Bridge Control register in the Root Port) using a WORD access, while preserving all the other fields in this register, and then writing a 0 using a WORD access, while preserving all the other fields in this register. (See Section 2.1.1.1.2 for details of the reset algorithm.)
5. If a non-sticky RW field was found in step 3, after the necessary delay, verify the same non-sticky field (from step 3) in the device on the secondary side of the Bridge, or on the downstream port of the Switch, or on the downstream port of the Root Port is reset to its default value. If the value has not changed to the default value, the test fails and is terminated.
6. For functions under test that have a link, the test is run at each of the following link speeds:
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- For a Bridge, a non-sticky register field in the device on the secondary side of the Bridge fails to reset to its default settings.
- For a Switch, a non-sticky register field in the device on the downstream port of the Switch fails to reset to its default settings.
- For a Root Port, a non-sticky register field in the device on the downstream port of the Root Port fails to reset to its default settings.

2.3.16. TD_3_10 Initiated Link Speed (Downstream Ports)

The test verifies that the function under test can function at the correct link speed when test software attempts to configure the function under test with each supported link speed as defined in the relevant specifications. (The test initiates the link speed change from the downstream port which is the function under test, but only if that downstream port supports selecting that link speed using the Target Link Speed field. In order to pass, the test requires that the upstream port device connected to the function under test supports all link speeds defined in the relevant specification. In order to pass, the test requires that the function under test be able train to each link speed up to the maximum link speed supported by the function under test.)

The test will run for 100 iterations and if any single iteration fails the test will report a failure and stop. The iteration stages will be different for the different Base levels of testing. However, in all stages, any link speed change will be initiated by the downstream port. (Note: The downstream port is required to attempt a speed change any time the Retrain Link field (Link Control register) is set to 1 and the current link speed is not equal to the Target Link Speed field. However, the actual negotiated link speed will be determined by the lowest Target Link Speed field of both the downstream port and upstream port.)

- For Base 1.x testing, the test will attempt to step the downstream port target link speed through a sequence of one stage, with the sequence repeated until 100 total iterations are performed.
 - For a 2.5 GT/s capable DUT connected to a 2.5 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP2.5=2.5
 - For a 2.5 GT/s capable DUT connected to a 5.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP5.0=2.5
 - For a 2.5 GT/s capable DUT connected to an 8.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP8.0=2.5
 - For a 2.5 GT/s capable DUT connected to a 16.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP16.0=2.5
- For Base 2.x testing, the test will attempt to step the downstream port target link speed through a multi-stage sequence of up to two stages, with the sequence repeated until 100 total iterations are performed.
 - For a 2.5 GT/s capable DUT connected to a 2.5 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP2.5=2.5
 - For a 2.5 GT/s capable DUT connected to a 5.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP5.0=2.5
 - For a 2.5 GT/s capable DUT connected to an 8.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP8.0=2.5
 - For a 2.5 GT/s capable DUT connected to a 16.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP16.0=2.5
 - For a 5.0 GT/s or greater capable DUT connected to a 2.5 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP2.5=2.5
 Stage 1: DP5.0+UP2.5=2.5
 - For a 5.0 GT/s or greater capable DUT connected to a 5.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP5.0=2.5
 Stage 1: DP5.0+UP5.0=5.0
 - For a 5.0 GT/s or greater capable DUT connected to an 8.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP8.0=2.5
 Stage 1: DP5.0+UP8.0=5.0
 - For a 5.0 GT/s or greater capable DUT connected to a 16.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP16.0=2.5
 Stage 1: DP5.0+UP16.0=5.0

- For Base 3.x testing, the test will attempt to step the downstream port target link speed through a multi-stage sequence of up to six stages, with the sequence repeated until 100 total iterations are performed.
 - For a 2.5 GT/s capable DUT connected to a 2.5 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP2.5=2.5
 - For a 2.5 GT/s capable DUT connected to a 5.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP5.0=2.5
 - For a 2.5 GT/s capable DUT connected to an 8.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP8.0=2.5
 - For a 2.5 GT/s capable DUT connected to a 16.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP16.0=2.5
 - For a 5.0 GT/s capable DUT connected to a 2.5 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP2.5=2.5
 Stage 1: DP5.0+UP2.5=5.0
 - For a 5.0 GT/s capable DUT connected to a 5.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP5.0=2.5
 Stage 1: DP5.0+UP5.0=5.0
 - For a 5.0 GT/s capable DUT connected to an 8.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP8.0=2.5
 Stage 1: DP5.0+UP8.0=5.0
 - For a 5.0 GT/s capable DUT connected to a 16.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP16.0=2.5
 Stage 1: DP5.0+UP16.0=5.0
 - For an 8.0 GT/s capable DUT connected to a 2.5 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP2.5=2.5
 Stage 1: DP5.0+UP2.5=2.5
 Stage 2: DP8.0+UP2.5=2.5
 Stage 3: DP5.0+UP2.5=2.5
 Stage 4: DP2.5+UP2.5=2.5
 Stage 5: DP8.0+UP2.5=2.5
 - For an 8.0 GT/s capable DUT connected to a 5.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP5.0=2.5
 Stage 1: DP5.0+UP5.0=5.0
 Stage 2: DP8.0+UP5.0=5.0
 Stage 3: DP5.0+UP5.0=5.0
 Stage 4: DP2.5+UP5.0=2.5
 Stage 5: DP8.0+UP5.0=5.0

- For an 8.0 GT/s capable DUT connected to an 8.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP8.0=2.5
 Stage 1: DP5.0+UP8.0=5.0
 Stage 2: DP8.0+UP8.0=8.0
 Stage 3: DP5.0+UP8.0=5.0
 Stage 4: DP2.5+UP8.0=2.5
 Stage 5: DP8.0+UP8.0=8.0
- For an 8.0 GT/s capable DUT connected to a 16.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP16.0=2.5
 Stage 1: DP5.0+UP16.0=5.0
 Stage 2: DP8.0+UP16.0=8.0
 Stage 3: DP5.0+UP16.0=5.0
 Stage 4: DP2.5+UP16.0=2.5
 Stage 5: DP8.0+UP16.0=8.0

(Note: For 8.0 GT/s or greater, this test assumes that hardware initiated Link Equalization has already been performed by the function under test. The test does not attempt to perform software initiated Link Equalization.)

- For Base 4.x testing, the test will attempt to step the downstream port target link speed through a multi-stage sequence of up to twelve stages, with the sequence repeated until 100 total iterations are performed.
 - For a 2.5 GT/s capable DUT connected to a 2.5 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP2.5=2.5
 - For a 2.5 GT/s capable DUT connected to a 5.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP5.0=2.5
 - For a 2.5 GT/s capable DUT connected to an 8.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP8.0=2.5
 - For a 2.5 GT/s capable DUT connected to a 16.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP16.0=2.5
 - For a 5.0 GT/s capable DUT connected to a 2.5 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP2.5=2.5
 Stage 1: DP5.0+UP2.5=5.0
 - For a 5.0 GT/s capable DUT connected to a 5.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP5.0=2.5
 Stage 1: DP5.0+UP5.0=5.0
 - For a 5.0 GT/s capable DUT connected to an 8.0 GT/s capable port, the sequence is:
 Stage 0: DP2.5+UP8.0=2.5
 Stage 1: DP5.0+UP8.0=5.0

- For a 5.0 GT/s capable DUT connected to a 16.0 GT/s capable port, the sequence is:
 - Stage 0: DP2.5+UP16.0=2.5
 - Stage 1: DP5.0+UP16.0=5.0
- For an 8.0 GT/s capable DUT connected to a 2.5 GT/s capable port, the sequence is:
 - Stage 0: DP2.5+UP2.5=2.5
 - Stage 1: DP5.0+UP2.5=2.5
 - Stage 2: DP8.0+UP2.5=2.5
 - Stage 3: DP5.0+UP2.5=2.5
 - Stage 4: DP2.5+UP2.5=2.5
 - Stage 5: DP8.0+UP2.5=2.5
- For an 8.0 GT/s capable DUT connected to a 5.0 GT/s capable port, the sequence is:
 - Stage 0: DP2.5+UP5.0=2.5
 - Stage 1: DP5.0+UP5.0=5.0
 - Stage 2: DP8.0+UP5.0=5.0
 - Stage 3: DP5.0+UP5.0=5.0
 - Stage 4: DP2.5+UP5.0=2.5
 - Stage 5: DP8.0+UP5.0=5.0
- For an 8.0 GT/s capable DUT connected to an 8.0 GT/s capable port, the sequence is:
 - Stage 0: DP2.5+UP8.0=2.5
 - Stage 1: DP5.0+UP8.0=5.0
 - Stage 2: DP8.0+UP8.0=8.0
 - Stage 3: DP5.0+UP8.0=5.0
 - Stage 4: DP2.5+UP8.0=2.5
 - Stage 5: DP8.0+UP8.0=8.0
- For an 8.0 GT/s capable DUT connected to a 16.0 GT/s capable port, the sequence is:
 - Stage 0: DP2.5+UP16.0=2.5
 - Stage 1: DP5.0+UP16.0=5.0
 - Stage 2: DP8.0+UP16.0=8.0
 - Stage 3: DP5.0+UP16.0=5.0
 - Stage 4: DP2.5+UP16.0=2.5
 - Stage 5: DP8.0+UP16.0=8.0
- For a 16.0 GT/s capable DUT connected to a 2.5 GT/s capable port, the sequence is:

Stage 0: DP2.5+UP2.5=2.5
Stage 1: DP5.0+UP2.5=2.5
Stage 2: DP8.0+UP2.5=2.5
Stage 3: DP5.0+UP2.5=2.5
Stage 4: DP2.5+UP2.5=2.5
Stage 5: DP8.0+UP2.5=2.5
Stage 6: DP16.0+UP2.5=2.5
Stage 7: DP8.0+UP2.5=2.5
Stage 8: DP2.5+UP2.5=2.5
Stage 9: DP16.0+UP2.5=2.5
Stage 10: DP5.0+UP2.5=2.5
Stage 11: DP16.0+UP2.5=2.5

- For a 16.0 GT/s capable DUT connected to a 5.0 GT/s capable port, the sequence is:

 Stage 0: DP2.5+UP5.0=2.5
 Stage 1: DP5.0+UP5.0=5.0
 Stage 2: DP8.0+UP5.0=5.0
 Stage 3: DP5.0+UP5.0=5.0
 Stage 4: DP2.5+UP5.0=2.5
 Stage 5: DP8.0+UP5.0=5.0
 Stage 6: DP16.0+UP5.0=5.0
 Stage 7: DP8.0+UP5.0=5.0
 Stage 8: DP2.5+UP5.0=2.5
 Stage 9: DP16.0+UP5.0=5.0
 Stage 10: DP5.0+UP5.0=5.0
 Stage 11: DP16.0+UP5.0=5.0

- For a 16.0 GT/s capable DUT connected to an 8.0 GT/s capable port, the sequence is:

 Stage 0: DP2.5+UP8.0=2.5
 Stage 1: DP5.0+UP8.0=5.0
 Stage 2: DP8.0+UP8.0=8.0
 Stage 3: DP5.0+UP8.0=5.0
 Stage 4: DP2.5+UP8.0=2.5
 Stage 5: DP8.0+UP8.0=8.0
 Stage 6: DP16.0+UP8.0=8.0
 Stage 7: DP8.0+UP8.0=8.0
 Stage 8: DP2.5+UP8.0=2.5
 Stage 9: DP16.0+UP8.0=8.0
 Stage 10: DP5.0+UP8.0=5.0
 Stage 11: DP16.0+UP8.0=8.0

- For a 16.0 GT/s capable DUT connected to a 16.0 GT/s capable port, the sequence is:

Stage 0: DP2.5+UP16.0=2.5
Stage 1: DP5.0+UP16.0=5.0
Stage 2: DP8.0+UP16.0=8.0
Stage 3: DP5.0+UP16.0=5.0
Stage 4: DP2.5+UP16.0=2.5
Stage 5: DP8.0+UP16.0=8.0
Stage 6: DP16.0+UP16.0=16.0
Stage 7: DP8.0+UP16.0=8.0
Stage 8: DP2.5+UP16.0=2.5
Stage 9: DP16.0+UP16.0=16.0
Stage 10: DP5.0+UP16.0=5.0
Stage 11: DP16.0+UP16.0=16.0

(Note: For 8.0 GT/s or greater, this test assumes that hardware initiated Link Equalization has already been performed by the function under test. The test does not attempt to perform software initiated Link Equalization.)

The test only runs if both the function under test and the upstream port device connected to the function under test, report a PCI Express Capability Version of 2h or greater.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on downstream ports of Root Ports, Switch Downstream Ports, and PCI/PCI-X to PCI Express Bridges; that report a PCI Express Capability Version of 2h or greater.

Starting Configuration

For a non-Root Port function under test, it is completely uninitialized following a reset, except that the bus number fields are initialized with valid numbers.

The immediate downstream device (the upstream port of the link connected to the function under test) is completely uninitialized following a reset.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test and the immediate downstream device (the upstream port of the link connected to the function under test) following the procedure described in Section 2.1.1.
2. Set Iteration Count [ICNT] to 0 and set Downstream port iteration Stage [DSTAGE] to 0.
3. For this test, the function under test will be referred to as the downstream port of the link. Downstream port Link Speed Value [DLSV] is used to control the link speed of the downstream port of the link. Initially set [DLSV] to 0001b.
4. For this test, function 0 of the immediate downstream device (the upstream port of the link connected to the function under test) will be referred to as the upstream port of the link. Upstream port Link Speed Value [ULSV] is used to control the link speed of the upstream port of the link.

5. Read the Link Capabilities register bits 3-0 value from the upstream port of the link and assign it to Upstream port Supported Speed Value [USSV] and perform the following:
 a. If [USSV] is 0000b, terminate the test, however this is not considered a failure, but rather the test result is reported as skipped.
 b. If [USSV] is 0001b or greater, then set [ULSV] to [USSV].
6. The Target Link Speed field (Link Control 2 register) is set to [ULSV] on the upstream port of the link and then the following tests are performed:
 a. If [USSV] is 0001b: the same Target Link Speed field is read back, and if it does not return [ULSV] or 0000b, terminate the test, however this is not considered a failure, but rather the test result is reported as skipped.
 b. If [USSV] is greater than 0001b: the same Target Link Speed field is read back, and if it does not return [ULSV], terminate the test, however this is not considered a failure, but rather the test result is reported as skipped.
7. Read the function under test's Link Capabilities register bits 3-0 value and assign it to Downstream port Supported Speed Value [DSSV] and perform the following:
 a. If [DSSV] is 0000b, then the test terminates with failure.
 b. If [DLSV] is 0010b or greater and [DSSV] is 0001b, then set [DSTAGE] to 0 and set [DLSV] to 0001b.
 c. If [DLSV] is 0011b or greater and [DSSV] is 0010b, then set [DSTAGE] to 0 and set [DLSV] to 0001b.
 d. If [DLSV] is 0100b and [DSSV] is 0011b, then set [DSTAGE] to 0 and set [DLSV] to 0001b.
8. The Target Link Speed field (Link Control 2 register) is set to [DLSV] on the function under test. This port will be referred to as the downstream port of the link.
9. The Target Link Speed field (Link Control 2 register) is read back and if it does not return [DLSV] on the downstream port of the link, then the test terminates with failure.
10. Test software writes a WORD to the Link Status register with both the Link Bandwidth Management Status field and the Link Autonomous Bandwidth Status field set to 1 (to clear the status).
11. Test software writes 1 to the Retrain Link field (Link Control register) on the downstream port of the link using a WORD access, while preserving all the other fields in this register.
12. Test software reads the Link Training field (Link Status register) on the downstream port of the link until it reads 0. If it does not return 0 within 1 second, then report this as a link training failure, and terminate the test with a failure.
13. Test software reads the Current Link Speed field (Link Status register) in both the function under test and the upstream port of the link. Both values must return a value equal to one of the following two values: if [DLSV] <= [ULSV] then value is [DLSV]; if [DLSV] > [ULSV] then value is either [ULSV] or the lesser of ([DLSV], [USSV]), otherwise the test terminates with failure.
14. Test software reads the Link Bandwidth Notification Capability field (Link Capabilities register) on the downstream port of the link and if it returns 1, the following tests are performed:
 a. Test software reads the Link Autonomous Bandwidth Status field (Link Status register) on the downstream port of the link. If it returns 1, terminate the test with a failure.

b. Test software reads the Link Bandwidth Management Status field (Link Status register) on the downstream port of the link and performs the following:
 i. If it returns 0, terminate the test with a failure.
 ii. If it returns 1, test software writes a WORD to the Link Status register with both the Link Bandwidth Management Status field and the Link Autonomous Bandwidth Status field set to 1 (to clear the status).

15. Based on the value of [DLSV] one of the following is performed:
 a. If [DLSV] is 0001b:
 i. For Base 2.x testing: if [DSSV] is 0010b or greater, then set [DSTAGE] to 1, and set [DLSV] to 0010b.
 ii. For Base 3.x or later testing: if [DSSV] is 0001b, then set [DSTAGE] to 0, and set [DLSV] to 0001b.
 iii. For Base 3.x or later testing: if [DSSV] is 0010b or greater and [DSTAGE] is 0, then increment [DSTAGE] by 1 and set [DLSV] to 0010b.
 iv. For Base 3.x or later testing: if [DSSV] is 0011b or greater and [DSTAGE] is 4, then increment [DSTAGE] by 1 and set [DLSV] to 0011b.
 v. For Base 4.x or later testing: if [DSSV] is 0100b or greater and [DSTAGE] is 8, then increment [DSTAGE] by 1 and set [DLSV] to 0100b.
 b. If [DLSV] is 0010b:
 i. For Base 2.x testing: set [DSTAGE] to 0 and set [DLSV] to 0001b.
 ii. For Base 3.x or later testing: if [DSSV] is 0010b or less and [DSTAGE] is 1, then set [DSTAGE] to 0, and set [DLSV] to 0001b.
 iii. For Base 3.x or later testing: if [DSSV] is 0011b or greater and [DSTAGE] is 1, then increment [DSTAGE] by 1 and set [DLSV] to 0011b.
 iv. For Base 3.x or later testing: if [DSTAGE] is 3, then increment [DSTAGE] by 1 and set [DLSV] to 0001b.
 v. For Base 4.x or later testing: if [DSTAGE] is 10, then increment [DSTAGE] by 1 and set [DLSV] to 0100b.
 c. If [DLSV] is 0011b:
 i. For Base 3.x or later testing: if [DSTAGE] is 2, then increment [DSTAGE] by 1 and set [DLSV] to 0010b.
 ii. For Base 3.x testing: if [DSTAGE] is 5, then set [DSTAGE] to 0 and set [DLSV] to 0001b.
 iii. For Base 4.x or later testing: if [DSSV] is 0011b or less and [DSTAGE] is 5, then set [DSTAGE] to 0, and set [DLSV] to 0001b.
 iv. For Base 4.x or later testing: if DSSV] is 0100b or greater and [DSTAGE] is 5, then increment [DSTAGE] by 1 and set [DLSV] to 0100b.
 v. For Base 4.x or later testing: if [DSTAGE] is 7, then increment [DSTAGE] by 1 and set [DLSV] to 0001b.
 d. If [DLSV] is 0100b:
 i. For Base 4.x or later testing: if [DSTAGE] is 6, then increment [DSTAGE] by 1 and set [DLSV] to 0011b.
 ii. For Base 4.x or later testing: if [DSTAGE] is 9, then increment [DSTAGE] by 1 and set [DLSV] to 0010b.
 iii. For Base 4.x or later testing: if [DSTAGE] is 11, then set [DSTAGE] to 0 and set [DLSV] to 0001b.

16. Increment [ICNT] by 1.

17. Based on the value of [ICNT] the following are performed:
 a. If [ICNT] equals or is greater than 100, terminate the test and report the test results as follows:
 i. If [DSSV] is less than or equal to [USSV], report the test results, without modification.
 ii. If [DSSV] is greater than [USSV], report any individual failing test results, otherwise if there are no failures, the overall test result is reported as skipped.
 b. If [ICNT] is less than 100, repeat steps 5-17.

The test *fails* if:

- The function under test fails to respond to any part of the standard configuration sequence.
- The function under test is connected to a downstream port, but it reports a Max Link Speed/Supported Link Speeds field of 0000b.
- The function under test reports a Max Link Speed/Supported Link Speeds field greater than 0001b and its Target Link Speed field cannot be written with a value between 0001b and the value reported in the Max Link Speed/Supported Link Speeds field.
- Link training fails to complete within 1 second of a test software initiated link retrain.
- The Current Link Speed in both the upstream port and the downstream port does not match the expected link speed in any case.
- In the function under test, the Link Bandwidth Notification Capability returns 1 and the Link Autonomous Bandwidth Status returns 1 following a link retrain.
- In the function under test, the Link Bandwidth Notification Capability returns 1 and the Link Bandwidth Management Status returns 0 following a link retrain.

2.3.17. TD_3_11 Supported Link Width (Downstream Ports)

The test verifies that the function under test can function at the correct link speed when hardware attempts to configure the function under test with the supported link width as defined in the relevant specifications. The test can be run with or without a mechanical adapter in the system slot to control the achievable link width. The test requires the Achievable Link Width selection to indicate the link width and in order to successfully complete this test, the function under test must be able to pass at that link width.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on downstream ports of Root Ports, Switch Downstream Ports, and PCI/PCI-X to PCI Express Bridges.

Starting Configuration

For a non-Root Port function under test, it is completely uninitialized following a reset, except that the bus number fields are initialized with valid numbers.

The immediate downstream device (the upstream port of the link connected to the function under test) is completely uninitialized following a reset.

Overview of Test Steps

Test software performs the following steps:

1. In manual mode, prompt the user for the Achievable Link Width selecton.
2. Set the tested Link Width Value [LWV] to 00 0001b (x1).
3. Set the tested Link Speed Value [LSV] to 0001b (2.5 GT/s). In manual mode, if the Achievable Link Width selection has not yet been obtained, prompt the user and ask if the function under test is connected to a x1 link. In automatic mode, check the specified parameter to see the Achieveable Link Width selection for the function under test. (If the slot has a link that contains more than 1 physical lane, it is necessary to restrict the lane width to x1 by placing a x16 to x1 mechanical adaptor in the system slot, or by using an add-in card that is only x1. All lanes except the configured width for the test are not terminated during the test case.) If the Achieveable Link Width selection is not x1, or the user response to x1 is NO, then skip this part of the test (this is not a failure) and continue the test at step 12.
4. Configure the function under and the immediate downstream device (the upstream port of the link connected to the function under test) following the procedure described in Section 2.1.1.
5. Set the link speed to [LSV], following the appropriate procedures described in Sections 2.1.2.12 to 2.1.2.142.1.2.15.
6. Test software reads the Current Link Speed field (Link Status register) in both the downstream port of the function under test and the immediate downstream device (the upstream port of the link connected to the function under test). The function under test port will be referred to as the downstream port of the link. The immediate downstream device will be referred to as the upstream port of the link. The values must return [LSV], if both sides support that link speed. If not, this is recorded as a failure and the test terminates.
7. Test software reads the Negotiated Link Width field (Link Status register) in both the downstream port of the link and the upstream port of the link. The values must return [LWV]. If not, this is recorded as a failure and the test terminates.
8. Repeat steps 4-7 for 100 iterations.
9. For Base 2.x or later testing: if the function under test reports Max Link Speed/Supported Link Speeds (Link Capabilities register) of 0010b or greater (it is capable of 5.0 GT/s operation) then set the tested Link Speed Value [LSV] to 0010b (5.0 GT/s) and repeat steps 4-8.
10. For Base 3.x or later testing: if the function under test reports Max Link Speed/Supported Link Speeds (Link Capabilities register) of 0011b or greater (it is capable of 8.0 GT/s operation) then set the tested Link Speed Value [LSV] to 0011b (8.0 GT/s) and repeat steps 4-8.
11. For Base 4.x or later testing: if the function under test report Max Link Speed/Supported Link Speeds (Link Capabilities register) of 0100b or greater (it is capable of 16.0 GT/s operation) then set the tested Link Speed Value [LSV] to 0100b (16.0 GT/s) and repeat steps 4-8.
12. Set the tested Link Width Value [LWV] to 00 0010b (x2).
 a. If the function under test reports Maximum Link Width field (Link Capabilities register) less than [LWV], terminate the test (this is not a failure).

b. If the upstream port of the link reports Maximum Link Width field (Link Capabilities register) less than [LWV], terminate the test (this is not a failure).
c. Set the tested Link Speed Value [LSV] to 0001b (2.5 GT/s). In manual mode, if the Achievable Link Width selection has not yet been obtained, prompt the user and ask if the function under test is connected to a x2 link. In automatic mode, check the specified parameter to see the Achieveable Link Width selection for the function under test. (If the slot has a link that contains more than 2 physical lanes, it is necessary to restrict the lane width to x2 by placing a x16 to x2 mechanical adaptor in the system slot, or by using a x2 add-in card. All lanes except the configured width for the test are not terminated during the test case.) If the Achieveable Link Width selection is not x2, or the user response to x2 is NO, then skip this part of the test (this is not a failure) and continue the test at step 13.
d. Repeat steps 4-11, with the following exception. For the first iteration only if the test fails to establish a link at the desired [LWV], then skip this part of the test (this is not a failure) and continue the test at step 13. Note: Since x2 support is optional, a port may not support this link width, but if it does support this link width, it must be able to train to it for each iteration attempt, otherwise this is recorded as a failure and the test terminates.

13. Set the tested Link Width Value [LWV] to 00 0100b (x4).
 a. If the function under test reports Maximum Link Width field (Link Capabilities register) less than [LWV], terminate the test (this is not a failure).
 b. If the upstream port of the link reports Maximum Link Width field (Link Capabilities register) less than [LWV], terminate the test (this is not a failure).
 c. Set the tested Link Speed Value [LSV] to 0001b (2.5 GT/s). In manual mode, if the Achievable Link Width selection has not yet been obtained, prompt the user and ask if the function under test is connected to a x4 link. In automatic mode, check the specified parameter to see the Achieveable Link Width selection for the function under test. (If the slot has a link that contains more than 4 physical lanes, it is necessary to restrict the lane width to x4 by placing a x16 to x4 mechanical adaptor in the system slot, or by using a x4 add-in card. All lanes except the configured width for the test are not terminated during the test case.) If the Achieveable Link Width selection is not x4, or the user response to x4 is NO, then skip this part of the test (this is not a failure) and continue the test at step 14.
 d. Repeat steps 4-11.
14. Set the tested Link Width Value [LWV] to 00 1000b (x8).
 a. If the function under test reports Maximum Link Width field (Link Capabilities register) less than [LWV], terminate the test (this is not a failure).
 b. If the downstream port of the link reports Maximum Link Width field (Link Capabilities register) less than [LWV], terminate the test (this is not a failure).
 c. Set the tested Link Speed Value [LSV] to 0001b (2.5 GT/s). In manual mode, if the Achievable Link Width selection has not yet been obtained, prompt the user and ask if the function under test is connected to a x8 link. In automatic mode, check the specified parameter to see the Achieveable Link Width selection for the function under test. (If the slot has a link that contains more than 8 physical lanes, it is necessary to restrict the lane width to x8 by placing a x16 to x8 mechanical adaptor in the system slot, or by using a x8 add-in card. All lanes except the configured width for the test are not terminated during the test case.) If the Achieveable Link Width selection is not x8, or the user response to x8 is NO, then skip this part of the test (this is not a failure) and continue the test at step 15.
 d. Repeat steps 4-11.

15. Set the tested Link Width Value [LWV] to 00 1100b (x12).
 a. If the function under test reports Maximum Link Width field (Link Capabilities register) less than [LWV], terminate the test (this is not a failure).
 b. If the upstream port of the link reports Maximum Link Width field (Link Capabilities register) less than [LWV], terminate the test (this is not a failure).
 c. Set the tested Link Speed Value [LSV] to 0001b (2.5 GT/s). In manual mode, if the Achievable Link Width selection has not yet been obtained, prompt the user and ask if the function under test is connected to a x12 link. In automatic mode, check the specified parameter to see the Achieveable Link Width selection for the function under test. (If the slot has a link that contains more than 12 physical lanes, it is necessary to restrict the lane width to x12 by placing a x16 to x12 mechanical adaptor in the system slot, or by using a x12 add-in card. All lanes except the configured width for the test are not terminated during the test case.) If the Achieveable Link Width selection is not x12, or the user response to x12 is NO, then skip this part of the test (this is not a failure) and continue the test at step 16.
 d. Repeat steps 4-11, with the following exception. For the first iteration only if the test fails to establish a link at the desired [LWV], then skip this part of the test (this is not a failure) and continue the test at step 16. Note: Since x12 support is optional, a port may not support this link width, but if it does support this link width, it must be able to train to it for each iteration attempt, otherwise this is recorded as a failure and the test terminates.
16. Set the tested Link Width Value [LWV] to 01 0000b (x16).
 a. If the function under test reports Maximum Link Width field (Link Capabilities register) less than [LWV], terminate the test (this is not a failure).
 b. If the downstream port of the link reports Maximum Link Width field (Link Capabilities register) less than [LWV], terminate the test (this is not a failure).
 c. Set the tested Link Speed Value [LSV] to 0001b (2.5 GT/s). In manual mode, if the Achievable Link Width selection has not yet been obtained, prompt the user and ask if the function under test is connected to a x16 link. In automatic mode, check the specified parameter to see the Achieveable Link Width selection for the function under test. If the Achieveable Link Width selection is not x16, or the user response to x16 is NO, then skip this part of the test (this is not a failure).
 d. Repeat steps 4-11.

The test *fails* if:

- The slot fails to respond to any part of the standard configuration sequence.
- The Current Link Speed does not match the expected link speed in any case.
- The Negotiated Link Width does not match the expected link width in any case.

2.3.18. TD_3_12 ARI Downstream Ports Support Non-Zero Device Number

The test verifies that if the function under test implements ARI Forwarding the test verifies that the downstream port with ARI Forwarding enabled allows Type 0 configuration access to non-zero Device Numbers as required in the relevant specifications. (This test requires a non-ARI device to be connected to the function under test's downstream port. It utilizes the requirement that a non-ARI device's upstream port must respond to a Configuration Read for Function Number 0, regardless of the Device Number value.)

Relevant Specifications

- *PCI Express Base Specification*
- *ECN Alternate Routing-ID Interpretation (to Base 2.0 and Base 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on downstream ports of Root Ports and Switch Downstream Ports.

Starting Configuration

For a non-Root Port function under test, it is completely uninitialized following a reset, except that the bus number fields are initialized with valid numbers.

The immediate downstream device (the upstream port of the link connected to the function under test) is completely uninitialized following a reset.

Overview of Test Steps

Test software performs the following steps:

1. Test software checks that the function under test reports the Capability Version field (PCI Express Capabilities register) is 2h or greater. If not, the test terminates (this is not a failure and the test result is reported as skipped).
2. Test software checks that the function under test reports the ARI Forwarding Supported field (Device Capabilities 2 register) as 1. If not, the test terminates (this is not a failure and the test result is reported as skipped).
3. Test software reads the ARI Forwarding Enable field (Device Control 2 register) on the function under test's downstream port, and saves its value for later restoration.
4. Test software programs the ARI Forwarding Enable field (Device Control 2 register) to 0 on the function under test.
5. Create a 16 bit value of Bus number/Device number/Function number [BDF] as follows: bits 15-8 = DUT's Secondary Bus Number value; bits 7-0 = 00h.
6. Test software issues a configuration read to the function at [BDF] for the WORD at location 00h (Vendor ID register) and it must return a value other than FFFFh. If it does not, the restoration described in step 11 is performed, and then the test terminates (this is not a failure and the test result is reported as skipped).
7. Test software checks that the function at [BDF] is a non-ARI device (by checking that it does not have an ARI Extended Capability). If it is an ARI device, the restoration described in step 11 is performed, and then the test terminates (this is not a failure and the test result is reported as skipped).
8. Test software programs the ARI Forwarding Enable field (Device Control 2 register) to 1 on the function under test.
9. Test software increments [BDF] by 8h (increments Device Number). If this causes the upper 8 bits of [BDF] to change (Device Number exceeds 1Fh), then skip to step 11.
10. Test software issues a configuration read to the function at [BDF] for the WORD at location 00h (Vendor ID register) and it must return a value other than FFFFh. If it does then repeat

steps 9-10. If it does not, this is recorded as a failure, the restoration described in step 11 is performed, and then the test terminates.

11. Test software programs the ARI Forwarding Enable field (Device Control 2 register) to the value saved in step 3 on the function under test. (This ensures that ARI functions will remain visible to other tests, and non-ARI functions will not be duplicated.)
12. For functions under test that have a link, the test is run at each of the following link speeds:
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- For any non-zero Device Number, the downstream port returns a value of FFFFh (Unsupported Request response) when an attempt is made to read the Vendor ID of Function Number = 000b on the Secondary Bus Number value of the downstream port (reading the Vendor ID of the function connected to the downstream port).

2.3.19. TD_3_14 Software Initiated 8.0 GT/s Link Equalization (Downstream Ports)

The test verifies that the function under test can function at the correct link speed when test software attempts to redo the Link Equalization procedure as defined in the relevant specifications. (The test initiates the Link Equalization procedure from the downstream port, but only if that downstream port supports 8.0 GT/s or greater. In order to pass, the test requires that the upstream port device connected to the function under test support 8.0 GT/s or greater.)

The test will only run for Base 3.x or later testing and it will run for 100 iterations and if any single iteration fails the test will report a failure and stop.

(Note: In using 8.0 GT/s, this test assumes that hardware initiated Link Equalization has already occurred once at that data rate and completed successfully.)

The test only runs if both the function under test and the upstream port device connected to the function under test, report a PCI Express Capability Version of 2h or greater.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on downstream ports of Root Ports, Switch Downstream Ports, and PCI/PCI-X to PCI Express Bridges; that report support for 8.0 GT/s or greater.

Starting Configuration

For a non-Root Port function under test, it is completely uninitialized following a reset, except that the bus number fields are initialized with valid numbers.

The immediate downstream device (the upstream port of the link connected to the function under test) is completely uninitialized following a reset.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test and the immediate downstream device (the upstream port of the link connected to the function under test) following the procedure described in Section 2.1.1.
2. Set Iteration Count [ICNT] to 0.
3. For this test, the function under test will be referred to as the downstream port of the link. Downstream port Link Speed Value [DLSV] is used to control the link speed of the downstream port of the link.
4. For this test, function 0 of the immediate downstream device (the upstream port of the link connected to the function under test) will be referred to as the upstream port of the link. Upstream port Link Speed Value [ULSV] is used to control the link speed of the upstream port of the link.
5. Test software reads a WORD from the Link Status 2 register of the function under test and checks that the Link Equalization Request 8.0 GT/s field returns 0 (i.e., initial link equalization was satisfactorily completed). If this field returns 1, terminate the test, however this is not considered a failure, but rather the test result is reported as skipped.
6. Test software writes a WORD to the Link Status 2 register of the function under test with the Link Equalization Request 8.0 GT/s field set to 1 (to clear the status).
7. Read the Link Capabilities register bits 3-0 value from the upstream port of the link and assign it to Upstream port Supported Speed Value [USSV] and perform the following:
 a. If [USSV] is 0010b or less, terminate the test, however this is not considered a failure, but rather the test result is reported as skipped.
 b. If [USSV] is 0011b or greater, then set [ULSV] to [USSV].
8. The Target Link Speed field (Link Control 2 register) is set to [ULSV] on the upstream port of the link and then the following tests are performed:
 a. If [USSV] is 0001b: the same Target Link Speed field is read back, and if it does not return [ULSV] or 0000b, terminate the test, however this is not considered a failure, but rather the test result is reported as skipped.
 b. If [USSV] is greater than 0001b: the same Target Link Speed field is read back, and if it does not return [ULSV], terminate the test, however this is not considered a failure, but rather the test result is reported as skipped.
9. Read the function under test's Link Capabilities register bits 3-0 value and assign it to Downstream port Supported Speed Value [DSSV] and perform the following:
 a. If [DSSV] is 0010b or less, then the test terminates with failure.
 b. If [DSSV] is 0011b or greater, then set [DLSV] to 0011b.
10. Test software writes 1 to the Perform Equalization field (Link Control 3 register) on the downstream port of the link.
11. The Target Link Speed field (Link Control 2 register) is set to [DLSV] on the function under test. This port will be referred to as the downstream port of the link.
12. The Target Link Speed field (Link Control 2 register) is read back and if it does not return [DLSV] on the downstream port of the link, then the test terminates with failure.

13. Test software writes a WORD to the Link Status register with both the Link Bandwidth Management Status field and the Link Autonomous Bandwidth Status field set to 1 (to clear the status).
14. Test software writes 1 to the Retrain Link field (Link Control register) on the downstream port of the link using a WORD access, while preserving all the other fields in this register.
15. Test software reads the Link Training field (Link Status register) on the downstream port of the link until it reads 0. If it does not return 0 within 1 second, then report this as a link training failure, and terminate the test with a failure.
16. Test software reads the Current Link Speed field (Link Status register) in both the function under test and the upstream port of the link. Both values must return a value equal to one of the following two values: if [DLSV] <= [ULSV] then value is [DLSV]; if [DLSV] > [ULSV] then value is either [ULSV] or the lesser of ([DLSV], [USSV]), otherwise the test result is as follows. If both the returned values are correct, the common returned value is assigned to the Current Link Speed Value [CLSV].
 a. If the test result was incorrect because both values of the current link speed are not as expected and the test was run starting at a link speed of 8.0 GT/s or greater, then the test terminates with failure.
 b. If the test result was incorrect because both values of the current link speed are not as expected and the test was run starting at a link speed of less than 8.0 GT/s, then the test terminates and a warning message is issued, but this is not treated in itself as a failure.
17. Test software reads the Link Bandwidth Notification Capability field (Link Capabilities register) on the downstream port of the link and if it returns 1, the following checks are performed:
 a. Test software reads the Link Autonomous Bandwidth Status field (Link Status register) on the downstream port of the link. If it returns 1, terminate the test with a failure.
 b. Test software reads the Link Bandwidth Management Status field (Link Status register) on the downstream port of the link and performs the following:
 i. If it returns 0, terminate the test with a failure.
 ii. If it returns 1, test software writes a WORD to the Link Status register with both the Link Bandwidth Management Status field and the Link Autonomous Bandwidth Status field set to 1 (to clear the status).
18. Test software reads the Link Status 2 register on the downstream port of the link and performs the following checks and if any are not as stated, this is recorded as a failure and the test terminates:
 a. If [CLSV] is 0011b:
 i. The Equalization 8.0 GT/s Complete field must be 1.
 ii. The Equalization 8.0 GT/s Phase 1 Successful field must be 1.
 iii. The Equalization 8.0 GT/s Phase 2 Successful field must be 1.
 iv. The Equalization 8.0 GT/s Phase 3 Successful field must be 1.
 v. The Link Equalization Request 8.0 GT/s field must be 0.
 b. If [CLSV] is 0010b or less and [USSV] is 0010b or less:
 i. The Equalization 8.0 GT/s Complete field must be 0.
 ii. The Equalization 8.0 GT/s Phase 1 Successful field must be 0.
 iii. The Equalization 8.0 GT/s Phase 2 Successful field must be 0.
 iv. The Equalization 8.0 GT/s Phase 3 Successful field must be 0.
 v. The Link Equalization Request 8.0 GT/s field must be 0.

19. Increment [ICNT] by 1.
20. Based on the value of [ICNT] the following are performed:
 a. If [ICNT] equals or is greater than 100, terminate the test and report the test results.
 b. If [ICNT] is less than 100, repeat steps 6-20.
21. For functions under test that have a link, the test is run at each of the following link speeds:
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- ❑ The function under test fails to respond to any part of the standard configuration sequence.
- ❑ The function under test reports a Max Link Speed/Supported Link Speeds field less than 0011b or its Target Link Speed field cannot be written with a value of 0011b.
- ❑ Link training fails to complete within 1 second of a test software initiated link retrain.
- ❑ The Current Link Speed field in both the upstream port and the downstream port does not match the expected link speed in any case.
- ❑ In the function under test, the Link Bandwidth Notification Capability field returns 1 and the Link Autonomous Bandwidth Status field returns 1 following a link retrain.
- ❑ In the function under test, the Link Bandwidth Notification Capability field returns 1 and the Link Bandwidth Management Status field returns 0 following a link retrain.
- ❑ In the function under test, the link speed following retrain is 8.0 GT/s and all of the following fields do not return 1: Equalization 8.0 GT/s Complete; Equalization 8.0 GT/s Phase 1 Successful; Equalization 8.0 GT/s Phase 2 Successful; Equalization 8.0 GT/s Phase 3 Successful.
- ❑ In the function under test, the link speed following retrain is not 8.0 GT/s and all of the following fields do not return 0: Equalization 8.0 GT/s Complete; Equalization 8.0 GT/s Phase 1 Successful; Equalization 8.0 GT/s Phase 2 Successful; Equalization 8.0 GT/s Phase 3 Successful.
- ❑ In the function under test, Link Equalization Request 8.0 GT/s field returns 1 following a link retrain.

The test *warns* if:

- ❑ When starting at an initial link speed less than 8.0 GT/s, the function under test fails to participate in a request to perform link equalization.

2.3.20. TD_3_16 Software Initiated 16.0 GT/s Link Equalization (Downstream Ports)

The test verifies that the function under test can function at the correct link speed when test software attempts to redo the Link Equalization procedure as defined in the relevant specifications. (The test initiates the Link Equalization procedure from the downstream port, but only if that

downstream port supports 16.0 GT/s or greater. In order to pass, the test requires that the upstream port device connected to the function under test support 16.0 GT/s or greater.)

The test will only run for Base 4.x or later testing and it will run for 100 iterations and if any single iteration fails the test will report a failure and stop.

(Note: In using 16.0 GT/s, this test assumes that hardware initiated Link Equalization has already occurred once at that data rate and completed successfully.)

The test only runs if both the function under test and the upstream port device connected to the function under test, report a PCI Express Capability Version of 2h or greater.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on downstream ports of Root Ports, Switch Downstream Ports, and PCI/PCI-X to PCI Express Bridges; that report support for 16.0 GT/s or greater.

Starting Configuration

For a non-Root Port function under test, it is completely uninitialized following a reset, except that the bus number fields are initialized with valid numbers.

The immediate downstream device (the upstream port of the link connected to the function under test) is completely uninitialized following a reset.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test and the immediate downstream device (the upstream port of the link connected to the function under test) following the procedure described in Section 2.1.1.
2. Set Iteration Count [ICNT] to 0.
3. For this test, the function under test will be referred to as the downstream port of the link. Downstream port Link Speed Value [DLSV] is used to control the link speed of the downstream port of the link.
4. For this test, function 0 of the immediate downstream device (the upstream port of the link connected to the function under test) will be referred to as the upstream port of the link. Upstream port Link Speed Value [ULSV] is used to control the link speed of the upstream port of the link.
5. Test software reads a DWORD from the 16.0 GT/s Status register of the function under test and checks that the Link Equalization Request 16.0 GT/s field returns 0 (i.e., initial link equalization was satisfactorily completed). If this field returns 1, terminate the test, however this is not considered a failure, but rather the test result is reported as skipped.
6. Test software writes a DWORD to the 16.0 GT/s Status register of the function under test with the Link Equalization Request 16.0 GT/s field set to 1 (to clear the status).
7. Read the Link Capabilities register bits 3-0 value from the upstream port of the link and assign it to Upstream port Supported Speed Value [USSV] and perform the following:

 a. If [USSV] is 0011b or less, terminate the test, however this is not considered a failure, but rather the test result is reported as skipped.
 b. If [USSV] is 0100b or greater, then set [ULSV] to [USSV].

8. The Target Link Speed field (Link Control 2 register) is set to [ULSV] on the upstream port of the link and then the following tests are performed:
 a. If [USSV] is 0001b: the same Target Link Speed field is read back, and if it does not return [ULSV] or 0000b, terminate the test, however this is not considered a failure, but rather the test result is reported as skipped.
 b. If [USSV] is greater than 0001b: the same Target Link Speed field is read back, and if it does not return [ULSV], terminate the test, however this is not considered a failure, but rather the test result is reported as skipped.
9. Read the function under test's Link Capabilities register bits 3-0 value and assign it to Downstream port Supported Speed Value [DSSV] and perform the following:
 a. If [DSSV] is 0011b or less, then the test terminates with failure.
 b. If [DSSV] is 0100b or greater, then set [DLSV] to 0100b.
10. Test software writes 1 to the Perform Equalization field (Link Control 3 register) on the downstream port of the link.
11. The Target Link Speed field (Link Control 2 register) is set to [DLSV] on the function under test. This port will be referred to as the downstream port of the link.
12. The Target Link Speed field (Link Control 2 register) is read back and if it does not return [DLSV] on the downstream port of the link, then the test terminates with failure.
13. Test software writes a WORD to the Link Status register with both the Link Bandwidth Management Status field and the Link Autonomous Bandwidth Status field set to 1 (to clear the status).
14. Test software writes 1 to the Retrain Link field (Link Control register) on the downstream port of the link using a WORD access, while preserving all the other fields in this register.
15. Test software reads the Link Training field (Link Status register) on the downstream port of the link until it reads 0. If it does not return 0 within 1 second, then report this as a link training failure, and terminate the test with a failure.
16. Test software reads the Current Link Speed field (Link Status register) in both the function under test and the upstream port of the link. Both values must return a value equal to one of the following two values: if [DLSV] <= [ULSV] then value is [DLSV]; if [DLSV] > [ULSV] then value is either [ULSV] or the lesser of ([DLSV], [USSV]), otherwise the test result is as follows. If both the returned values are correct, the common returned value is assigned to the Current Link Speed Value [CLSV].
 a. If the test result was incorrect because both values of the current link speed are not as expected and the test was run starting at a link speed of 16.0 GT/s or greater, then the test terminates with failure.
 b. If the test result was incorrect because both values of the current link speed are not as expected and the test was run starting at a link speed of less than 16.0 GT/s, then the test terminates and a warning message is issued, but this is not treated in itself as a failure.
17. Test software reads the Link Bandwidth Notification Capability field (Link Capabilities register) on the downstream port of the link and if it returns 1, the following checks are performed:

a. Test software reads the Link Autonomous Bandwidth Status field (Link Status register) on the downstream port of the link. If it returns 1, terminate the test with a failure.
b. Test software reads the Link Bandwidth Management Status field (Link Status register) on the downstream port of the link and performs the following:
 i. If it returns 0, terminate the test with a failure.
 ii. If it returns 1, test software writes a WORD to the Link Status register with both the Link Bandwidth Management Status field and the Link Autonomous Bandwidth Status field set to 1 (to clear the status).

18. Test software reads the 16.0 GT/s Status register on the downstream port of the link and performs the following checks and if any are not as stated, this is recorded as a failure and the test terminates:
 a. If [CLSV] is 0100b:
 i. The Equalization 16.0 GT/s Complete field must be 1.
 ii. The Equalization 16.0 GT/s Phase 1 Successful field must be 1.
 iii. The Equalization 16.0 GT/s Phase 2 Successful field must be 1.
 iv. The Equalization 16.0 GT/s Phase 3 Successful field must be 1.
 v. The Link Equalization Request 16.0 GT/s field must be 0.
 b. If [CLSV] is 0011b or less and [USSV] is 0011b or less:
 i. The Equalization 16.0 GT/s Complete field must be 0.
 ii. The Equalization 16.0 GT/s Phase 1 Successful field must be 0.
 iii. The Equalization 16.0 GT/s Phase 2 Successful field must be 0.
 iv. The Equalization 16.0 GT/s Phase 3 Successful field must be 0.
 v. The Link Equalization Request 16.0 GT/s field must be 0.
19. Increment [ICNT] by 1.
20. Based on the value of [ICNT] the following are performed:
 a. If [ICNT] equals or is greater than 100, terminate the test and report the test results.
 b. If [ICNT] is less than 100, repeat steps 6-20.
21. For functions under test that have a link, the test is run at each of the following link speeds:
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- ❑ The function under test fails to respond to any part of the standard configuration sequence.
- ❑ The function under test reports a Max Link Speed/Supported Link Speeds field less than 0100b or its Target Link Speed field cannot be written with a value of 0100b.
- ❑ Link training fails to complete within 1 second of a test software initiated link retrain.
- ❑ The Current Link Speed field in both the upstream port and the downstream port does not match the expected link speed in any case.
- ❑ In the function under test, the Link Bandwidth Notification Capability field returns 1 and the Link Autonomous Bandwidth Status field returns 1 following a link retrain.
- ❑ In the function under test, the Link Bandwidth Notification Capability field returns 1 and the Link Bandwidth Management Status field returns 0 following a link retrain.

- In the function under test, the link speed following retrain is 16.0 GT/s and all of the following fields do not return 1: Equalization 16.0 GT/s Complete; Equalization 16.0 GT/s Phase 1 Successful; Equalization 16.0 GT/s Phase 2 Successful; Equalization 16.0 GT/s Phase 3 Successful.
- In the function under test, the link speed following retrain is not 16.0 GT/s and all of the following fields do not return 0: Equalization 16.0 GT/s Complete; Equalization 16.0 GT/s Phase 1 Successful; Equalization 16.0 GT/s Phase 2 Successful; Equalization 16.0 GT/s Phase 3 Successful.
- In the function under test, Link Equalization Request 16.0 GT/s field returns 1 following a link retrain.

The test *warns* if:

- When starting at an initial link speed less than 16.0 GT/s, the function under test fails to participate in a request to perform link equalization.

APPENDIX A. Informational Test Details

A.1 TD_1_57x MR-IOV Extended Capability Structure

The test verifies that if the function under test reports a MR-IOV Extended Capability structure, it is implemented as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *ECN PCI Express Capability Structure Expansion (to Base 1.1)*
- *ECN Function Level Reset (to Base 1.1)*
- *ECN Link Bandwidth Notification (to Base 1.1)*
- *ECN Optimized Buffer Flush/Fill (to Base 2.0 and Base 2.1)*
- *ECN ASPM Optionality (to Base 2.1)*
- *Multi-Root I/O Virtualization and Sharing Specification Revision 1.0*
- *ECN Downstream Port Containment (DPC) (to Base 3.0)*
- *ECN Separate Refclk Independent SSC Architecture (SRIS) (to Base 3.0)*
- *M-PCIe ECN (to Base 3.0)*
- *ECN Readiness Notifications (RN) (to Base 3.0)*
- *ECN Extension Devices (to Base 3.0)*
- *ECN Emergency Power Reduction mechanism with PWRBRK signal (to Base 3.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0011h (MR-IOV Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Extended Capability ID of 0011h is found in an Extended Capability structure for a VF, the test terminates with a failure.
4. If the Extended Capability ID of 0011h is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
5. If the Extended Capability ID of 0011h is found in an Extended Capability structure, the device type must be PCI Express Endpoint, Legacy Endpoint, Root Complex Integrated Endpoint, Switch Upstream Port, or Switch Downstream Port. If not, the test terminates with a failure.
6. If the Extended Capability ID of 0011h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0011h is not found in an Extended Capability structure, the test skips to step 13.
7. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
8. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
9. If the device type is PCI Express Endpoint, Legacy Endpoint, or Root Complex Integrated Endpoint the following checks are performed:
 a. Test software reads a DWORD from offset 04h (MR-IOV Capabilities register) and if the Is Main BF field is 1, then the following checks are performed:
 i Test software reads a DWORD from offset 20h (VL Arbitration Capability and Status register) and determines the MaxVL field value which is saved as [MaxVL].
 ii Test software writes a 1 to the MR Enable field in MR-IOV Control (offset 08h).
 iii Test software writes FFh to the VL Enable field in MR-IOV Control (offset 08h).
 iv Test software reads MR-IOV Control register (offset 08h) and checks that the VL Enable field bits [MaxVL] to 0 each are 1 and the VL Enable field bits 7 to [MaxVL] each are 0. If any are not this is recorded as a failure, but the test continues.
 v Test software writes a 0 to the MR Enable field in MR-IOV Control (offset 08h).
 vi Test software writes FFh to the VL Enable field in MR-IOV Control (offset 08h).
 vii Test software reads MR-IOV Control register (offset 08h) and checks that the VL Enable field bits 0 to 7 are 01h. If not, this is recorded as a failure, but the test continues.
 viii Test software reads a DWORD from offset 10h (MR-IOV VH Counts register) and determines the MaxVH field value which is saved as [MaxVH].
 ix Test software writes a 0 to the MR Enable field in MR-IOV Control (offset 08h).
 x Test software writes [MaxVH] to the NumVH field in MR-IOV VH Counts (offset 10h).
 xi Test software reads MR-IOV VH Counts register (offset 10h) and checks that the NumVH field is [MaxVH]. If not, this is recorded as a failure, but the test continues.
 xii Test software writes a 1 to the MR Enable field in MR-IOV Control (offset 08h).
 xiii Test software writes 00h to the NumVH field in MR-IOV VH Counts (offset 10h).
 xiv Test software reads MR-IOV VH Counts register (offset 10h) and checks that the NumVH field is [MaxVH]. If not, this is recorded as a failure, but the test continues.

xv Test software writes a 0 to the MR Enable field in MR-IOV Control (offset 08h).
xvi Test software writes 00h to the NumVH field in MR-IOV VH Counts (offset 10h).
xvii Test software reads MR-IOV VH Counts register (offset 10h) and checks that the NumVH field is 00h. If not, this is recorded as a failure, but the test continues.

b. Test software reads a DWORD from offset 10h (MR-IOV VH Counts register), and checks that the Function Table Entry Size field is 16 or larger. If not, this is recorded as a failure, but the test continues.
c. Test software reads a DWORD from offset 14h (Function Table Offset register) and performs the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 i The Function Table BIR field must return one of the following values: 000b to 101b.
 ii The BAR pointed to by the Function Table BIR field value is read and bit 0 of that BAR must be 0 (Memory BAR).
 iii The Function Table Offset must be 4 or larger.
d. Test software reads a DWORD from offset 1Ch (LVF Table Offset register) and performs the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 i The LVF Table BIR field must return one of the following values: 000b to 101b.
 ii The BAR pointed to by the LVF Table BIR field value is read and bit 0 of that BAR must be 0 (Memory BAR).
e. Test software reads a DWORD from offset 04h (MR-IOV Capabilities register) and if the VL Arbitration Table Present field is 1, then the following checks are performed:
 i Test software reads VL Arbitration Capability and Status register (offset 20h) and performs the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The VL Arbitration Capability field bits 6 to 10 are each 0.
 b. If the VL Arbitration Capability field bit 5 is 1, then the Reference Clock field must be 00b.
 ii Test software reads a DWORD from offset 28h (VL Arbitration Table Offset register) and performs the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The VL Arbitration Table BIR field must return one of the following values: 000b to 101b.
 b. The BAR pointed to by the VL Arbitration Table BIR field value is read and bit 0 of that BAR must be 0 (Memory BAR).
f. Test software reads a DWORD from offset 54h (Statistics Capability register), and if the Number of Statistics Blocks field is non-zero, the following checks are performed and if any are not as stated, this is recorded as a failure, but the test continues:
 i The Number of Statistics Blocks field is less than or equal to 32 (including 0).
 ii If the Number of Statistics Block field is greater than 0 and less or equal to 32, the value is stored in [NSTBK].
 iii Test software reads a DWORD from offset 58h (Statistics Block Start/Busy register) and if [NSTBK] is less than 32, it checks that bits [NSTBK] to 31 are all 0.
 iv If [NSTBK] is less than 32, test software writes a DWORD of FFFF FFFFh to offset 58h (Statistics Block Start/Busy register).
 v Test software reads a DWORD from offset 58h (Statistics Block Start/Busy register) and if [NSTBK] is less than 32, it checks that bits [NSTBK] to 31 are all 0.

vi Test software reads a DWORD from offset 5Ch (Statistics Block Stop/Busy register) and if [NSTBK] is less than 32, it checks that bits [NSTBK] to 31 are all 0.
vii If [NSTBK] is less than 32, test software writes a DWORD of FFFF FFFFh to offset 5Ch (Statistics Block Stop/Busy register).
viii Test software reads a DWORD from offset 5Ch (Statistics Block Stop/Busy register) and if [NSTBK] is less than 32, it checks that bits [NSTBK] to 31 are all 0.

g. Test software reads a DWORD from offset 54h (Statistics Capability register), and if the Number of Statistics Descriptors field is non-zero, the following checks are performed:
 i. Test software reads a DWORD from offset 60h (Statistics Descriptor Table Offset register) and performs the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The Statistics Descriptor Table BIR field must return one of the following values: 000b to 101b.
 b. The BAR pointed to by the Statistics Descriptor Table BIR field value is read and bit 0 of that BAR must be 0 (Memory BAR).
 ii. Test software reads a DWORD from offset 54h (Statistics Capability register), and if the Number of Statistics Blocks field is non-zero, the following checks are performed:
 iii. Test software reads a DWORD from offset 64h (Statistics Block Table Offset register) and performs the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The Statistics Block Table BIR field must return one of the following values: 000b to 101b.
 b. The BAR pointed to by the Statistics Block Table BIR field value is read and bit 0 of that BAR must be 0 (Memory BAR).

10. If the device type is PCI Switch Upstream Port, or Switch Downstream Port the following checks are performed:
 a. Test software reads a DWORD from offset 18h (MR-IOV Authorization register), and checks that the VS Authorization Bitmap Offset field is greater than 0FFh. If not, this is recorded as a failure, but the test continues.
 b. Test software reads a DWORD from offset 1Ch (MR-IOV Port Table Sizes register), and checks that the Port Table Entry Size field is 31 or larger. If not, this is recorded as a failure, but the test continues.
 c. Test software reads a DWORD from offset 20h (Port Table Offset register) and performs the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 i The Port Table BIR field must return one of the following values: 000b to 001b.
 ii The BAR pointed to by the Port Table BIR field value is read and bit 0 of that BAR must be 0 (Memory BAR).
 iii The Port Table Offset field must be 4 or larger.
 d. Test software reads a DWORD from offset 24h (MR-IOV VS Table Sizes register), and checks that the VS Table Entry Size field is 3 or larger. If not, this is recorded as a failure, but the test continues.
 e. Test software reads a DWORD from offset 28h (VS Table Offset register) and performs the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 i The VS Table BIR field must return one of the following values: 000b to 001b.
 ii The BAR pointed to by the VS Table BIR field value is read and bit 0 of that BAR must be 0 (Memory BAR).

iii The VS Table Offset field must be 4 or larger.

f. Test software reads a DWORD from offset 2Ch (MR-IOV VS Bridge Table Sizes register), and checks that the VS Bridge Table Entry Size field is 12 or larger. If not, this is recorded as a failure, but the test continues.

g. Test software reads a DWORD from offset 30h (VS Bridge Table Offset register) and performs the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 i The VS Bridge Table BIR field must return one of the following values: 000b to 001b.
 ii The BAR pointed to by the VS Bridge Table BIR field value is read and bit 0 of that BAR must be 0 (Memory BAR).

h. Test software reads a DWORD from offset 34h (Statistics Capability register), and the Number of Statistics Blocks field should return a non-zero value. If it does not, a warning message is issued, but this is not treated in itself as a failure.

i. Test software reads a DWORD from offset 34h (Statistics Capability register), and if the Number of Statistics Blocks field is non-zero, the following checks are performed and if any are not as stated, this is recorded as a failure, but the test continues:
 i The Number of Statistics Blocks field is less than or equal to 32 (including 0).
 ii If the Number of Statistics Block field is greater than 0 and less or equal to 32, the value is stored in [NSTBK].
 iii Test software reads a DWORD from offset 38h (Statistics Block Start/Busy register) and if [NSTBK] is less than 32, it checks that bits [NSTBK] to 31 are all 0.
 iv If [NSTBK] is less than 32, test software writes a DWORD of FFFF FFFFh to offset 38h (Statistics Block Start/Busy register).
 v Test software reads a DWORD from offset 38h (Statistics Block Start/Busy register) and if [NSTBK] is less than 32, it checks that bits [NSTBK] to 31 are all 0.
 vi Test software reads a DWORD from offset 3Ch (Statistics Block Stop/Busy register) and if [NSTBK] is less than 32, it checks that bits [NSTBK] to 31 are all 0.
 vii If [NSTBK] is less than 32, test software writes a DWORD of FFFF FFFFh to offset 3Ch (Statistics Block Stop/Busy register).
 viii Test software reads a DWORD from offset 3Ch (Statistics Block Stop/Busy register) and if [NSTBK] is less than 32, it checks that bits [NSTBK] to 31 are all 0.

j. Test software reads a DWORD from offset 34h (Statistics Capability register), and if the Number of Statistics Descriptors field should return a non-zero value. If it does not, a warning message is issued, but this is not treated in itself as a failure.

k. Test software reads a DWORD from offset 34h (Statistics Capability register), and if the Number of Statistics Descriptors field is non-zero, the following checks are performed and if any are not as stated, this is recorded as a failure, but the test continues:
 i Test software reads a DWORD from offset 40h (Statistics Descriptor Table Offset register) and performs the following checks:
 a. The Statistics Descriptor Table BIR field must return one of the following values: 000b to 001b.
 b. The BAR pointed to by the Statistics Descriptor Table BIR field value is read and bit 0 of that BAR must be 0 (Memory BAR).

l. Test software reads a DWORD from offset 34h (Statistics Capability register), and if the Number of Statistics Blocks field is non-zero, the following checks are performed:

i Test software reads a DWORD from offset 44h (Statistics Block Table Offset register) and performs the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The Statistics Block Table BIR field must return one of the following values: 000b to 001b.
 b. The BAR pointed to by the Statistics Block Table BIR field value is read and bit 0 of that BAR must be 0 (Memory BAR).

11. The following register field characteristic checks are performed:

MR-IOV Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

MR-IOV Capabilities Register (Offset 04h) — DWORD

(for Endpoints)

a. VF Mapping Supported	
(if VL Migration Supported is 1)	RO-Ones
(if VL Migration Supported is 0)	RO
b. VF Migration Supported	RO
c. VL Arbitration Table Present	
(if Is Main BF is 1 and MaxVL is non-zero)	RO
(if Is Main BF is 1 and MaxVL is zero)	RO-Zero
(if Is Main BF is 0)	RO-Zero
d. Is Main BF	RO
e. RsvdZ_7-4	RO-Zero
f. Function Dependency Link	RO
g. RsvdZ_19-16	RO-Zero
h. MSI Supported	RO
i. MSI Vector Number	
(if MSI Supported is 1)	RO
(if MSI Supported is 0)	RO-Zero

MR-IOV Capabilities Register (Offset 04h) — DWORD

(for Switch Ports)

a. RsvdZ_20-0	RO-Zero
b. MSI Vector Number	RO

MR-IOV Control Register (Offset 08h) — DWORD

(for Endpoints)

a. Function Table Interrupt Enable	RW
b. Statistics Interrupt Enable	
(if Number of Statistic Blocks is non-zero)	RW
(if Number of Statistics Blocks is 0)	RO-Zero
c. RsvdP_2	RO-Zero
d. MR Uncorrectable Fatal TLP Error Interrupt Enable	
(if Is Main BF is 1)	RW
(if Is Main BF is 0)	RO-Zero
e. RsvdP_4	RO-Zero
f. MR Uncorrectable Global Key Error Interrupt Enable	

(if Is Main BF is 1)	RW
(if Is Main BF is 0)	RO-Zero
g. RsvdP_6	RO-Zero
h. MR Enable	
(if Is Main BF is 1)	RW
(if Is Main BF is 0)	RO-Zero
i. RsvdP_15-8	RO-Zero
j. VL Enable	
(if Is Main BF is 1: bit 0)	RO-Ones
(if Is Main BF is 1 and MR Enable is written with 1: bits [MaxVF] to 1)	RW
(if Is Main BF is 1 and MR Enable is written with 0: bits [MaxVF] to 1)	RO-Zero
(if Is Main BF is 1: bits 7 to [MaxVF])	RO-Zero
(if Is Main BF is 0)	RO-Zero
(The MR Enable field must be written with the appropriate value before this field is tested. Only values up to the value returned in the MaxVF register can be written.)	
k. RsvdP_31-24	RO-Zero

MR-IOV Control Register (Offset 08h) — DWORD

(for Switch Ports)

a. Port Interrupt Enable	
(if VS is Authorized)	RW
(if VS is not Authorized)	RO-Zero
b. VS Interrupt Enable	
(if VS is Authorized)	RW
(if VS is not Authorized)	RO-Zero
c. RsvdP_2	RO-Zero
d. Statistics Interrupt Enable	
(if VS is Authorized and Number of Statistic Blocks is non-zero)	RW
(if VS is Authorized and Number of Statistic Blocks is 0)	RO-Zero
(if VS is not Authorized)	RO-Zero
e. RsvdP_15-4	RO-Zero
f. MR Switch Number	
(if VS is Authorized)	RW
(if VS is not Authorized)	RO-Zero

MR-IOV Status Register (Offset 0Ch) — DWORD

(for Endpoints)

a. Function Table Interrupt Status	RO
b. Statistics Interrupt Status	
(if Number of Statistic Blocks is non-zero)	RW1C
(if Number of Statistic Blocks is 0)	RO-Zero
c. RsvdZ_14-2	RO-Zero
d. MSI Scheduled	
(if MSI Supported is 1)	RW1C
(if MSI Supported is 0)	RO-Zero
e. VL Negotiation Pending	
(if Is Main BF is 1)	RO
(if Is Main BF is 0)	RO-Zero
f. RsvdZ_31-24	RO-Zero

MR-IOV Status Register (Offset 0Ch) — DWORD

(for Switch Ports)

a. Port Interrupt Status	
(if VS is Authorized)	RO
(if VS is not Authorized)	RO-Zero
b. VS Interrupt Status	
(if VS is Authorized)	RO
(if VS is not Authorized)	RO-Zero
c. RsvdZ_2	RO-Zero
d. Statistics Interrupt Status	
(if Number of Statistic Blocks is non-zero)	RW1C
(if Number of Statistic Blocks is 0)	RO-Zero
e. RsvdZ_14-4	RO-Zero
f. MSI Scheduled	RW1C
g. RsvdZ_31-16	RO-Zero

MR-IOV VH Counts Register (Offset 10h) — DWORD

(for Endpoints)

a. MaxVH	
(if Is Main BF is 1)	RO
(if Is Main BF is 0)	RO-Zero
b. Function Table Entry Size	RO
c. NumVH	
(if Is Main BF is 1 and MR Enable is written with 0)	RW
(if Is Main BF is 1 and MR Enable is written with 1)	RO
(if Is Main BF is 0)	RO-Zero
(The MR Enable field must be written with the appropriate value before this field is tested.)	
d. RsvdZ_31-24	RO-Zero

MR-IOV This Bridge Map Register (Offset 10h) — DWORD

(for Switch Ports)

a. VS is Authorized	RO
b. RsvdZ_15-1	RO-Zero
c. VS Bridge Number	RO
d. VS Number	RO

MR-IOV Function Table Offset Register (Offset 14h) — DWORD

(for Endpoints)

a. Function Table BIR	RO
b. Function Table Offset	RO

MR-IOV Watchdog Timer Control Register (Offset 14h) — DWORD

(for Switch Ports)

a. Rearm Watchdog	RO
b. RsvdP_15-1	RO-Zero
c. Watchdog Timer Interval	
(if VS is Authorized)	RW
(if VS is not Authorized)	RO-Zero
d. RsvdP_31-24	RO-Zero

Note: If the Watchdog Timer Interval field is written with a non-zero value, then the Rearm Watchdog field must be written with a 1 every second until the Watchdog Timer Interval field is written to 0. Failure to do this may cause the Switch Port to get reset to its default state if the Watchdog timer expires.

MR-IOV VF MVF Region Register (Offset 18h) — DWORD

(for Endpoints)

a. Max LVF	RO
b. Max MVF	
(if VF Mapping Supported is 1)	RO
(if VF Mapping Supported is 0)	RO-Zero

MR-IOV Authorization Register (Offset 18h) — DWORD

(for Switch Ports)

a. Management VS	
(if VS is Authorized)	RW
(if VS is not Authorized)	RO-Zero
b. RsvdZ_19-8	RO-Zero
c. VS Authorization Bitmap Offset	RO

MR-IOV LVF Table Offset Register (Offset 1Ch) — DWORD

(for Endpoints)

a. LVF Table BIR	RO
b. LVF Table Offset	RO

MR-IOV Port Table Sizes Register (Offset 1Ch) — DWORD

(for Switch Ports)

a. Num Port Table Entries	RO
b. Port Table Entry Size	RO
c. RsvdZ_31-16	RO-Zero

MR-IOV VL Arbitration Capability and Status Register (Offset 20h) — DWORD

(for Endpoints)

a. VL Arbitration Capability	
(if VL Arbitration Table Present is 1)	RO
(if VL Arbitration Table Present is 0)	RO-Zero
b. VL Arbitration Status	
(if VL Arbitration Table Present is 1)	RO
(if VL Arbitration Table Present is 0)	RO-Zero
c. RsvdZ_13	RO-Zero
d. Reference Clock	
(if VL Arbitration Table Present is 1)	RO
(if VL Arbitration Table Present is 0)	RO-Zero
e. MaxVL	
(if Is Main BF is 1)	RO
(if Is Main BF is 0)	RO-Zero
f. RsvdZ_23-19	RO-Zero
g. Maximum Time Slots	
(if VL Arbitration Table Present is 1)	RO
(if VL Arbitration Table Present is 0)	RO-Zero
h. RsvdZ_31	RO-Zero

MR-IOV Port Table Offset Register (Offset 20h) — DWORD

(for Switch Ports)

a. Port Table BIR	RO
b. Port Table Offset	RO

MR-IOV VL Arbitration Control Register (Offset 24h) — DWORD

(for Endpoints)

a. Load VL Arbitration Table	RO-Zero
b. RsvdP_7-1	RO-Zero
c. VL Arbitration Select	
(if VL Arbitration Table Present is 1)	RW
(only those values in VL Arbitration Capability are written)	
(if VL Arbitration Table Present is 0)	RO-Zero
d. RsvdP_15-12	RO-Zero
e. VL Strict Priority Arbitration	
(if VL Arbitration Table Present is 1)	RW
(if VL Arbitration Table Present is 0)	RO-Zero
f. RsvdP_31-24	RO-Zero

MR-IOV VS Table Sizes Register (Offset 24h) — DWORD

(for Switch Ports)

a. Num VS Table Entries	RO
b. VS Table Entry Size	RO
c. RsvdZ_31-16	RO-Zero

MR-IOV VL Arbitration Table Offset Register (Offset 28h) — DWORD

(for Endpoints)

a. VL Arbitration Table BIR	
(if VL Arbitration Table Present is 1)	RO
(if VL Arbitration Table Present is 0)	RO-Zero
b. VL Arbitration Table Offset	
(if VL Arbitration Table Present is 1)	RO
(if VL Arbitration Table Present is 0)	RO-Zero

MR-IOV VS Table Offset Register (Offset 28h) — DWORD

(for Switch Ports)

a. VS Table BIR	RO
b. VS Table Offset	RO

MR-IOV MR Error Status Register (Offset 2Ch) — WORD

(for Endpoints)

a. MR First Error Pointer	
(if Is Main BF is 1)	ROS
(if Is Main BF is 0)	RO-Zero
b. MR Uncorrectable Fatal TLP Error Status	
(if Is Main BF is 1)	RW1CS
(if Is Main BF is 0)	RO-Zero
c. RsvdZ_5	RO-Zero
d. MR Uncorrectable Global Key Error Status	
(if Is Main BF is 1)	RW1CS
(if Is Main BF is 0)	RO-Zero

e. RsvdZ_14-7 RO-Zero
f. MR Multiple Uncorrectable Error
(if Is Main BF is 1) RW1CS
(if Is Main BF is 0) RO-Zero

MR-IOV MR Error Control Register (Offset 2Eh) — WORD

(for Endpoints)
a. RsvdP_3-0 RO-Zero
b. MR Uncorrectable Fatal TLP Error Mask
(if Is Main BF is 1) RWS
(if Is Main BF is 0) RO-Zero
c. RsvdP_5 RO-Zero
d. MR Uncorrectable Global Key Error Mask
(if Is Main BF is 1) RWS
(if Is Main BF is 0) RO-Zero
e. RsvdP_15-7 RO-Zero

MR-IOV VS Bridge Table Sizes Register (Offset 2Ch) — DWORD

(for Switch Ports)
a. Num VS Bridge Table Entries RO
b. VS Bridge Table Entry Size RO
c. RsvdZ_31-16 RO-Zero

MR-IOV Header Log Register (Offset 30h) — 9 DWORDS

(for Endpoints)
a. Header Log register (1st DW)
(if Is Main BF is 1) ROS
(if Is Main BF is 0) RO-Zero
b. Header Log register (2nd DW)
(if Is Main BF is 1) ROS
(if Is Main BF is 0) RO-Zero
c. Header Log register (3rd DW)
(if Is Main BF is 1) ROS
(if Is Main BF is 0) RO-Zero
d. Header Log register (4th DW)
(if Is Main BF is 1) ROS
(if Is Main BF is 0) RO-Zero
e. Header Log register (5th DW)
(if Is Main BF is 1) ROS
(if Is Main BF is 0) RO-Zero
f. Header Log register (6th DW)
(if Is Main BF is 1) ROS
(if Is Main BF is 0) RO-Zero
g. Header Log register (7th DW)
(if Is Main BF is 1) ROS
(if Is Main BF is 0) RO-Zero
h. Header Log register (8th DW)
(if Is Main BF is 1) ROS
(if Is Main BF is 0) RO-Zero

i. Header Log register (9th DW)
(if Is Main BF is 1) ROS
(if Is Main BF is 0) RO-Zero

MR-IOV VS Bridge Table Offset Register (Offset 30h) — DWORD

(for Switch Ports)
a. VS Bridge Table BIR RO
b. VS Bridge Table Offset RO

MR-IOV Statistics Capability Register (Offset 34h) — DWORD

(for Switch Ports)
a. Number of Statistics Descriptors
(if VS is Authorized) RO
(if VS is not Authorized) RO-Zero
b. Number of Statistics Blocks
(if VS is Authorized) RO
(if VS is not Authorized) RO-Zero
c. RsvdZ_31-16 RO-Zero

MR-IOV Statistics Block Start/Busy Register (Offset 38h) — DWORD

(for Switch Ports)
(if VS is not Authorized then all bits) RO-Zero
(if Number of Statistics Blocks is 00h then all bits) RO-Zero
(if Number of Statistics Blocks is non-zero and less than 32:
bits 31-[Number of Statistics Blocks]) RO-Zero

(For the bits that are implemented the value written cannot be read back, so only the unimplemented bits in this register can be checked.)

MR-IOV Statistics Block Stop/Busy Register (Offset 3Ch) — DWORD

(for Switch Ports)
(if VS is not Authorized then all bits) RO-Zero
(if Number of Statistics Blocks is 00h then all bits) RO-Zero
(if Number of Statistics Blocks is non-zero and less than 32:
bits 31-[Number of Statistics Blocks]) RO-Zero

(For the bits that are implemented the value written cannot be read back, so only the unimplemented bits in this register can be checked.)

MR-IOV Statistics Descriptor Table Offset Register (Offset 40h) — DWORD

(for Switch Ports)
a. Statistics Descriptor Table BIR
(if Number of Statistics Descriptors is non-zero) RO
(if Number of Statistics Descriptors is 00h) RO-Zero
b. Statistics Descriptor Table Offset
(if Number of Statistics Descriptors is non-zero) RO
(if Number of Statistics Descriptors is 00h) RO-Zero

MR-IOV Statistics Block Table Offset Register (Offset 44h) — DWORD

(for Switch Ports)
a. Statistics Block Table BIR
(if Number of Statistics Blocks is non-zero) RO

(if Number of Statistics Blocks is 00h) RO-Zero

b. Statistics Block Table Offset
(if Number of Statistics Blocks is non-zero) RO
(if Number of Statistics Blocks is 00h) RO-Zero

MR-IOV Statistics Capability Register (Offset 54h) — DWORD

(for Endpoints)

a. Number of Statistics Descriptors RO
b. Number of Statistics Blocks RO
c. RsvdZ_31-16 RO-Zero

MR-IOV Statistics Block Start/Busy Register (Offset 58h) — DWORD

(for Endpoints)
(if Number of Statistics Blocks is 00h then all bits) RO-Zero
(if Number of Statistics Blocks is non-zero and less than 32:
bits 31-[Number of Statistics Blocks]) RO-Zero

(For the bits that are implemented the value written cannot be read back, so only the unimplemented bits in this register can be checked.)

MR-IOV Statistics Block Stop/Busy Register (Offset 5Ch) — DWORD

(for Endpoints)
(if Number of Statistics Blocks is 00h then all bits) RO-Zero
(if Number of Statistics Blocks is non-zero and less than 32:
bits 31-[Number of Statistics Blocks]) RO-Zero

(For the bits that are implemented the value written cannot be read back, so only the unimplemented bits in this register can be checked.)

MR-IOV Statistics Descriptor Table Offset Register (Offset 60h) — DWORD

(for Endpoints)

a. Statistics Descriptor Table BIR
(if Number of Statistics Descriptors is non-zero) RO
(if Number of Statistics Descriptors is 00h) RO-Zero
b. Statistics Descriptor Table Offset
(if Number of Statistics Descriptors is non-zero) RO
(if Number of Statistics Descriptors is 00h) RO-Zero

MR-IOV Statistics Block Table Offset Register (Offset 64h) — DWORD

(for Endpoints)

a. Statistics Block Table BIR
(if Number of Statistics Blocks is non-zero) RO
(if Number of Statistics Blocks is 00h) RO-Zero
b. Statistics Block Table Offset
(if Number of Statistics Blocks is non-zero) RO
(if Number of Statistics Blocks is 00h) RO-Zero

VS Authorization Bitmap ([offset]) – [r] DWORDS

(for Switch Ports)

a. ([Num VS Table Entries]-1 to 0)
(for bit [n] if VS Table Entry [n] VS Present is 1 and VS is Authorized) RW
Note: All values of [n] from 0 to [Num VS Table Entries]-1 are tested.

(for bit [n] if VS Table Entry [n] VS Present is 0) RO-Zero
Note: All values of [n] from 0 to [Num VS Table Entries]-1 are tested.
(if VS is not Authorized) RO-Zero
b. (bits ([r] * 32) – 1 to [Num VS Table Entries]) RO-Zero

(This group of registers only exists if the Num VS Table Entries field is greater than 0, and therefore this group of registers is not tested if this condition is not true.)
Note: The value of [offset] is the value returned by the VS Authorization Bitmap Offset field. The value of [r] is ([Num VS Table Entries] divided by 32) rounded up to the next integer number.

LVF Table LVF Table Entry (n) ([table] + ([n] * 4)) — DWORD

(for Endpoints)
a. MVF # for this LVF
(bits [high bit] to 0) RW
(bits 15 to [high bit] + 1) RO-Zero
(The value of [high bit] is the smallest value that satisfies the requirement that 2 ** [high bit] is able to denote the range 0 to [Max MVF].)
b. VF State
(if VF Migration Supported is 1) RW
(if VF Migration Supported is 0) RO-Zero
c. RsvdP_31-18 RO-Zero

(This group of registers only exists if the VF Mapping Supported field is a 1, and therefore this group of registers is not tested if this condition is not true. The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the LVF Table BIR field value) plus the offset (value in the LVF Table Offset field multiplied by 8). All values of [n] between 0 and the value in the Max LVF field inclusive must be tested.

Function Interrupt Status Bitmap ([table] - 8) — 8 DWORDS

(for Endpoints)
(if MSI Supported is 1 then for all bits) RO
(if MSI Supported is 0 then for all bits) RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Function Table BIR field value) plus the offset (value in the Function Table Offset field multiplied by 8).

Function Table Entry (n) Function Capabilities 1 ([table] + ([n] * [size])) + 00h — DWORD

(for Endpoints)
a. Num VC Resources Hardware Present
(if VC Capability Supported is 1) RO
(if VC Capability Supported is 0) RO-Zero
b. RsvdZ_3 RO-Zero

c. VC Capability Supported — RO
d. RsvdZ_7-5 — RO-Zero
e. Num MFVC Resources Hardware Present
 (if MFVC Capability Supported is 1) — RO
 (if MFVC Capability Supported is 0) — RO-Zero
f. RsvdZ_11 — RO-Zero
g. MFVC Capability Supported — RO
h. RsvdZ_15-13 — RO-Zero
i. Function Present
 (if (n) is 0) — RO
 (if (n) is non-zero) — RO-Zero
j. RsvdZ_23-17 — RO-Zero
k. Function Offset — RO

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Function Table BIR field value) plus the offset (value in the Function Table Offset field multiplied by 8). The value of [size] is the value in the Function Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the MaxVH field inclusive must be tested.

Function Table Entry (n) Function Capabilities 2 ([table] + ([n] * [size])) + 04h — DWORD

(for Endpoints)
a. First VF Offset
 (for PFs) — RO
 (for non-PFs) — RO-Zero
b. VF Stride
 (for PFs) — RO
 (for non-PFs) — RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Function Table BIR field value) plus the offset (value in the Function Table Offset field multiplied by 8). The value of [size] is the value in the Function Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the MaxVH field inclusive must be tested.

Function Table Entry (n) Function Control 1 ([table] + ([n] * [size])) + 08h — DWORD

(for Endpoints)
a. VC Extended VC Count
 (if VC Capability Supported is 1) — RW
 (if VC Capability Supported is 0) — RO-Zero
b. RsvdP_3 — RO-Zero
c. VC Low Priority Extended VC Count
 (if VC Capability Supported is 1) — RW

(if VC Capability Supported is 0)	RO-Zero
d. RsvdP_7	RO-Zero
e. MFVC Extended VC Count	
(if MFVC Capability Supported is 1)	RW
(if MFVC Capability Supported is 0)	RO-Zero
f. RsvdP_11	RO-Zero
g. MFVC Low Priority Extended VC Count	
(if MFVC Capability Supported is 1)	RW
(if MFVC Capability Supported is 0)	RO-Zero
h. RsvdP_15	RO-Zero
i. Global Key	
(if Is Main BF is 1)	RW
(if Is Main BF is 0)	RO-Zero
j. RsvdP_30-28	RO-Zero
k. Global Key Check Enable	
(if Is Main BF is 1)	RW
(if Is Main BF is 0)	RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Function Table BIR field value) plus the offset (value in the Function Table Offset field multiplied by 8). The value of [size] is the value in the Function Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the MaxVH field inclusive must be tested.

Function Table Entry (n) Function Control 2 ([table] + ([n] * [size])) + 0Ch — DWORD
(for Endpoints)

a. VC Config Changed Interrupt Enable	
(if VC Capability Supported is 1)	RW
(if VC Capability Supported is 0)	RO-Zero
b. MFVC Config Changed Interrupt Enable	
(if MFVC Capability Supported is 1)	RW
(if MFVC Capability Supported is 0)	RO-Zero
c. PF Reset Initiated Interrupt Enable	
(if VF Migration Supported is 1)	RW
(if VF Migration Supported is 0)	RO-Zero
d. VF Migration Status Interrupt Enable	
(if VF Migration Supported is 1)	RW
(if VF Migration Supported is 0)	RO-Zero
e. VF Enable Interrupt Enable	
(if VF Mapping Supported is 1)	RW
(if VF Mapping Supported is 0)	RO-Zero
f. RsvdP_8-5	RO-Zero
g. VF Migration Capable	
(if VF Migration Supported is 1)	RW
(if VF Migration Supported is 0)	RO-Zero
h. RsvdP_15-10	RO-Zero

i. InitialVFs
 (for PFs with VF Mapping Supported as 1) RW
 (for PFs with VF Mapping Supported as 0) RO
 (for non-PFs) RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Function Table BIR field value) plus the offset (value in the Function Table Offset field multiplied by 8). The value of [size] is the value in the Function Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the MaxVH field inclusive must be tested.

Function Table Entry (n) Function Control 3 ([table] + ([n] * [size])) + 10h — DWORD
(for Endpoints)

a. Base LVF
 (if VF Mapping Supported is 1) RW
 (if VF Mapping Supported is 0) RO-Zero
b. TotalVFs
 (if VF Migration Supported is 1) RW
 (if VF Migration Supported is 0) RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Function Table BIR field value) plus the offset (value in the Function Table Offset field multiplied by 8). The value of [size] is the value in the Function Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the MaxVH field inclusive must be tested.

Function Table Entry (n) Function Status ([table] + ([n] * [size])) + 14h — DWORD
(for Endpoints)

a. VC Config Changed
 (if VC Capability Supported is 1) RW1C
 (if VC Capability Supported is 0) RO-Zero
b. MFVC Config Changed
 (if MFVC Capability Supported is 1) RW1C
 (if MFVC Capability Supported is 0) RO-Zero
c. PF Reset Initiated
 (if VF Migration Supported is 1) RW1C
 (if VF Migration Supported is 0) RO-Zero
d. VF Migration Status
 (if VF Migration Supported is 1) RW1C
 (if VF Migration Supported is 0) RO-Zero
e. VF Enable Changed
 (if VF Mapping Supported is 1) RW1C
 (if VF Mapping Supported is 0) RO-Zero
f. VF Initialization Pending

(if VF Migration Supported is 1)	RW1C
(if VF Migration Supported is 0)	RO-Zero
g. RsvdZ_7-6	RO-Zero
h. VF Enabled	RO
i. VF Migration Enabled	
(if VF Migration Supported is 1)	RO
(if VF Migration Supported is 0)	RO-Zero
j. RsvdZ_15-10	RO-Zero
k. NumVFs	RO

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Function Table BIR field value) plus the offset (value in the Function Table Offset field multiplied by 8). The value of [size] is the value in the Function Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the MaxVH field inclusive must be tested.

Function Table Entry (n) VC to VL Map 1 ([table] + ([n] * [size])) + 18h –– DWORD
(for Endpoints)

a. VC0 VL Map	
(if Is Main BF is 1 and MaxVL is non-zero and VC Capability Supported is 1)	
after first writing VC0 VL Map Enable with 0	RW
after first writing VC0 VL Map Enable with 1	RO
(if Is Main BF is 1 and MaxVL is 000b)	RO-Zero
(if Is Main BF is 1 and VC Capability Supported is 0)	RO-Zero
(if Is Main BF is 0)	RO-Zero
b. RsvdP_3	RO-Zero
c. VC0 VL Map Enable	
(if Is Main BF is 1 and MaxVL is non-zero and VC Capability Supported is 1)	RW
(if Is Main BF is 1 and MaxVL is 000b)	RO
(if Is Main BF is 1 and VC Capability Supported is 0)	RO
(if Is Main BF is 0)	RO-Zero
d. RsvdP_7-5	RO-Zero
e. VC1 VL Map	
(if Is Main BF is 1 and MaxVL is non-zero and VC Capability Supported is 1 and Num VC Resources Hardware Present is 1 or greater)	
after first writing VC1 VL Map Enable with 0	RW
after first writing VC1 VL Map Enable with 1	RO
(if Is Main BF is 1 and MaxVL is 000b)	RO-Zero
(if Is Main BF is 1 and VC Capability Supported is 0)	RO-Zero
(if Is Main BF is 1 and Num VC Resources Hardware Present is less than 1)	RO-Zero
(if Is Main BF is 0)	RO-Zero
f. RsvdP_11	RO-Zero
g. VC1 VL Map Enable	
(if Is Main BF is 1 and MaxVL is non-zero and VC Capability Supported is 1	

and Num VC Resources Hardware Present is 1 or greater)	RW
(if Is Main BF is 1 and MaxVL is 000b)	RO-Zero
(if Is Main BF is 1 and VC Capability Supported is 0)	RO-Zero
(if Is Main BF is 1 and Num VC Resources Hardware Present is less than 1)	RO-Zero
(if Is Main BF is 0)	RO-Zero
h. RsvdP_15-13	RO-Zero
i. VC2 VL Map	
(if Is Main BF is 1 and MaxVL is non-zero and VC Capability Supported is 1 and Num VC Resources Hardware Present is 2 or greater)	
after first writing VC2 VL Map Enable with 0	RW
after first writing VC2 VL Map Enable with 1	RO
(if Is Main BF is 1 and MaxVL is 000b)	RO-Zero
(if Is Main BF is 1 and VC Capability Supported is 0)	RO-Zero
(if Is Main BF is 1 and Num VC Resources Hardware Present is less than 2)	RO-Zero
(if Is Main BF is 0)	RO-Zero
j. RsvdP_19	RO-Zero
k. VC2 VL Map Enable	
(if Is Main BF is 1 and MaxVL is non-zero and VC Capability Supported is 1 and Num VC Resources Hardware Present is 2 or greater)	RW
(if Is Main BF is 1 and MaxVL is 000b)	RO-Zero
(if Is Main BF is 1 and VC Capability Supported is 0)	RO-Zero
(if Is Main BF is 1 and Num VC Resources Hardware Present is less than 2)	RO-Zero
(if Is Main BF is 0)	RO-Zero
l. RsvdP_23-21	RO-Zero
m. VC3 VL Map	
(if Is Main BF is 1 and MaxVL is non-zero and VC Capability Supported is 1 and Num VC Resources Hardware Present is 3 or greater)	
after first writing VC3 VL Map Enable with 0	RW
after first writing VC3 VL Map Enable with 1	RO
(if Is Main BF is 1 and MaxVL is 000b)	RO-Zero
(if Is Main BF is 1 and VC Capability Supported is 0)	RO-Zero
(if Is Main BF is 1 and Num VC Resources Hardware Present is less than 3)	RO-Zero
(if Is Main BF is 0)	RO-Zero
n. RsvdP_27	RO-Zero
o. VC3 VL Map Enable	
(if Is Main BF is 1 and MaxVL is non-zero and VC Capability Supported is 1 and Num VC Resources Hardware Present is 3 or greater)	RW
(if Is Main BF is 1 and MaxVL is 000b)	RO-Zero
(if Is Main BF is 1 and VC Capability Supported is 0)	RO-Zero
(if Is Main BF is 1 and Num VC Resources Hardware Present is less than 3)	RO-Zero
(if Is Main BF is 0)	RO-Zero
p. RsvdP_31-29	RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Function Table BIR field value) plus the offset (value in the Function Table Offset field multiplied by 8). The value of [size] is the value in the Function Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the MaxVH field inclusive must be tested.

Function Table Entry (n) VC to VL Map 2 ([table] + ([n] * [size])) + 1Ch — DWORD
(for Endpoints)

a. VC4 VL Map	
(if Is Main BF is 1 and MaxVL is non-zero and VC Capability Supported is 1 and Num VC Resources Hardware Present is 4 or greater)	
after first writing VC4 VL Map Enable with 0	RW
after first writing VC4 VL Map Enable with 1	RO
(if Is Main BF is 1 and MaxVL is 000b)	RO-Zero
(if Is Main BF is 1 and VC Capability Supported is 0)	RO-Zero
(if Is Main BF is 1 and Num VC Resources Hardware Present is less than 4)	RO-Zero
(if Is Main BF is 0)	RO-Zero
b. RsvdP_3	RO-Zero
c. VC4 VL Map Enable	
(if Is Main BF is 1 and MaxVL is non-zero and VC Capability Supported is 1 and Num VC Resources Hardware Present is 4 or greater)	RW
(if Is Main BF is 1 and MaxVL is 000b)	RO-Zero
(if Is Main BF is 1 and VC Capability Supported is 0)	RO-Zero
(if Is Main BF is 1 and Num VC Resources Hardware Present is less than 4)	RO-Zero
(if Is Main BF is 0)	RO-Zero
d. RsvdP_7-5	RO-Zero
e. VC5 VL Map	
(if Is Main BF is 1 and MaxVL is non-zero and VC Capability Supported is 1 and Num VC Resources Hardware Present is 5 or greater)	
after first writing VC5 VL Map Enable with 0	RW
after first writing VC5 VL Map Enable with 1	RO
(if Is Main BF is 1 and MaxVL is 000b)	RO-Zero
(if Is Main BF is 1 and VC Capability Supported is 0)	RO-Zero
(if Is Main BF is 1 and Num VC Resources Hardware Present is less than 5)	RO-Zero
(if Is Main BF is 0)	RO-Zero
f. RsvdP_11	RO-Zero
g. VC5 VL Map Enable	
(if Is Main BF is 1 and MaxVL is non-zero and VC Capability Supported is 1 and Num VC Resources Hardware Present is 5 or greater)	RW
(if Is Main BF is 1 and MaxVL is 000b)	RO-Zero
(if Is Main BF is 1 and VC Capability Supported is 0)	RO-Zero

(if Is Main BF is 1 and Num VC Resources Hardware Present is less than 5) RO-Zero
(if Is Main BF is 0) RO-Zero

h. RsvdP_15-13 RO-Zero

i. VC6 VL Map
(if Is Main BF is 1 and MaxVL is non-zero and VC Capability Supported is 1 and Num VC Resources Hardware Present is 6 or greater)
after first writing VC6 VL Map Enable with 0 RW
after first writing VC6 VL Map Enable with 1 RO
(if Is Main BF is 1 and MaxVL is 000b) RO-Zero
(if Is Main BF is 1 and VC Capability Supported is 0) RO-Zero
(if Is Main BF is 1 and Num VC Resources Hardware Present is less than 6) RO-Zero
(if Is Main BF is 0) RO-Zero

j. RsvdP_19 RO-Zero

k. VC6 VL Map Enable
(if Is Main BF is 1 and MaxVL is non-zero and VC Capability Supported is 1 and Num VC Resources Hardware Present is 6 or greater) RW
(if Is Main BF is 1 and MaxVL is 000b) RO-Zero
(if Is Main BF is 1 and VC Capability Supported is 0) RO-Zero
(if Is Main BF is 1 and Num VC Resources Hardware Present is less than 6) RO-Zero
(if Is Main BF is 0) RO-Zero

l. RsvdP_23-21 RO-Zero

m. VC7 VL Map
(if Is Main BF is 1 and MaxVL is non-zero and VC Capability Supported is 1 and Num VC Resources Hardware Present is 7)
after first writing VC7 VL Map Enable with 0 RW
after first writing VC7 VL Map Enable with 1 RO
(if Is Main BF is 1 and MaxVL is 000b) RO-Zero
(if Is Main BF is 1 and VC Capability Supported is 0) RO-Zero
(if Is Main BF is 1 and Num VC Resources Hardware Present is less than 7) RO-Zero
(if Is Main BF is 0) RO-Zero

n. RsvdP_27 RO-Zero

o. VC7 VL Map Enable
(if Is Main BF is 1 and MaxVL is non-zero and VC Capability Supported is 1 and Num VC Resources Hardware Present is 7) RW
(if Is Main BF is 1 and MaxVL is 000b) RO-Zero
(if Is Main BF is 1 and VC Capability Supported is 0) RO-Zero
(if Is Main BF is 1 and Num VC Resources Hardware Present is less than 7) RO-Zero
(if Is Main BF is 0) RO-Zero

p. RsvdP_31-29 RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Function Table BIR field value) plus the offset (value in the Function Table Offset field multiplied by 8). The value of [size] is the value in the Function Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the MaxVH field inclusive must be tested.

Function Table Entry (n) Reserved ([table] + ([n] * [size])) + 20h — 4 DWORDS

(for Endpoints)

a. Reserved register (1st DW) — RO-Zero
b. Reserved register (2nd DW) — RO-Zero
c. Reserved register (3rd DW) — RO-Zero
d. Reserved register (4th DW) — RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Function Table BIR field value) plus the offset (value in the Function Table Offset field multiplied by 8). The value of [size] is the value in the Function Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the MaxVH field inclusive must be tested.

Function Table Entry (n) VC Resource State (m) ([table] + ([n] * [size])) + 30h + ([m] * 4) — DWORD

(for Endpoints)

a. VC Enabled
 (if [m] is 0) — RO-Ones
 (if [m] is non-zero
 and [m] is less than or equal to Num VC Resources Hardware Present
 and [m] is less than or equal to VC Extended VC Count) — RO
 (if [m] is non-zero
 and [m] is less than or equal to Num VC Resources Hardware Present
 and [m] is greater than VC Extended VC Count) — RO-Zero
b. VC Negotiation Pending
 (if [m] is less than or equal to Num VC Resources Hardware Present
 and [m] is less than or equal to VC Extended VC Count) — RO
 (if [m] is less than or equal to Num VC Resources Hardware Present
 and [m] is greater than VC Extended VC Count) — RO-Zero
c. RsvdZ_3-2 — RO-Zero
d. VC ID
 (if [m] is 0) — RO-Zero
 (if [m] is non-zero
 and [m] is less than or equal to Num VC Resources Hardware Present
 and [m] is less than or equal to VC Extended VC Count) — RO
 (if [m] is non-zero
 and [m] is less than or equal to Num VC Resources Hardware Present
 and [m] is greater than VC Extended VC Count) — RO-Zero
e. RsvdZ_15-7 — RO-Zero
f. TC to VC Map

(if [m] is 0) RO
(if [m] is non-zero
and [m] is less than or equal to Num VC Resources Hardware Present
and [m] is less than or equal to VC Extended VC Count) RO
(if [m] is non-zero
and [m] is less than or equal to Num VC Resources Hardware Present
and [m] is greater than VC Extended VC Count) RO-Zero

g. RsvdZ_31-24 RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested. The register group is tested twice if the Num VC Resources Hardware Present field is greater than 0. The first time it is tested after the VC Extended VC Count field is written with the value returned in the Num VC Resources Hardware Present field. The second time it is tested after the VC Extended VC Count field is written with 000b, but only if the Num VC Resources Hardware Present field is greater than 0.)

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Function Table BIR field value) plus the offset (value in the Function Table Offset field multiplied by 8). The value of [size] is the value in the Function Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the MaxVH field inclusive must be tested. All values of [m] between 0 and the value in the Num VC Resources Hardware Present field inclusive must be tested.

Function Table Entry (n) MFVC Resource State (m) ([table] + ([n] * [size])) + 30h + [offset] + ([m] * 4) — DWORD

(for Endpoints)

a. VC Enabled
(if [m] is 0) RO-Ones
(if [m] is non-zero
and [m] is less than or equal to Num MFVC Resources Hardware Present
and [m] is less than or equal to MFVC Extended VC Count) RO
(if [m] is non-zero
and [m] is less than or equal to Num MFVC Resources Hardware Present
and [m] is greater than MFVC Extended VC Count) RO-Zero

b. VC Negotiation Pending
(if [m] is less than or equal to Num MFVC Resources Hardware Present
and [m] is less than or equal to MFVC Extended VC Count) RO
(if [m] is less than or equal to Num MFVC Resources Hardware Present
and [m] is greater than MFVC Extended VC Count) RO-Zero

c. RsvdZ_3-2 RO-Zero

d. VC ID
(if [m] is 0) RO-Zero
(if [m] is non-zero
and [m] is less than or equal to Num MFVC Resources Hardware Present
and [m] is less than or equal to MFVC Extended VC Count) RO
(if [m] is non-zero
and [m] is less than or equal to Num MFVC Resources Hardware Present
and [m] is greater than MFVC Extended VC Count) RO-Zero

e. RsvdZ_15-7 RO-Zero
f. TC to VC Map
(if [m] is 0) RO
(if [m] is non-zero
and [m] is less than or equal to Num MFVC Resources Hardware Present
and [m] is less than or equal to MFVC Extended VC Count) RO
(if [m] is non-zero
and [m] is less than or equal to Num MFVC Resources Hardware Present
and [m] is greater than MFVC Extended VC Count) RO-Zero
g. RsvdZ_31-24 RO-Zero

(This group of registers only exists if the MFVC Capability Supported field is a 1, and therefore this group of registers is not tested if this condition is not true. The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested. If this register group is tested at all, it is tested twice if the Num VC Resources Hardware Present field is greater than 0. The first time it is tested after the MFVC Extended VC Count field is written with the value returned in the Num MFVC Resources Hardware Present field. The second time it is tested after the MFVC Extended VC Count field is written with 000b, but only if the Num VC Resources Hardware Present field is greater than 0.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Function Table BIR field value) plus the offset (value in the Function Table Offset field multiplied by 8). The value of [size] is the value in the Function Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the MaxVH field inclusive must be tested. If the MFVC Capability Supported field is a 1, then all values of [m] between 0 and the value in the Num MFVC Resources Hardware Present field inclusive must be tested. The value of [offset] is the value returned by the Num VC Resources Present field plus one and then multiplied by 4.

Function Table Entry (n) Reserved ([table] + ([n] * [size])) + 30h + [offset] + ([m] * 4) — [r] DWORDS
(for Endpoints)
(all bits) RO-Zero

(This group of registers only exists if [r] is larger than 0, and therefore this group of registers is not tested if this condition is not true. The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Function Table BIR field value) plus the offset (value in the Function Table Offset field multiplied by 8). The value of [size] is the value in the Function Table Entry Size field multiplied by 4. The value of [r] is ((([Function Table Entry Size] * 4) – ((12 * 4) + [offset])) / 4). All values of [n] between 0 and the value in the MaxVH field inclusive must be tested. All values of [m] between 0 and (((([Function Table Entry Size] * 4) - ((12 * 4) + [offset])) / 4) – 1) must be tested. The value of [offset] is the ([Num VC Resources Present] + 1) * 4 + {only if the MFVC Capability Supported field is a 1: (([Num MFVC Resources Present] + 1) * 4)}.

Port Interrupt Status Bitmap ([table] - 8) — 8 DWORDS
(for Switch Ports)

a. (bits [Num Port Table Entries]-1 to 0)
 (for bit [n] if Port Table Entry [n] Port Present is 1 and VS is Authorized) RO
 Note: All values of [n] from 0 to [Num Port Table Entries]-1 are tested.
 (for bit [n] if Port Table Entry [n] Port Present is 0) RO-Zero
 Note: All values of [n] from 0 to [Num Port Table Entries]-1 are tested.
 (if VS is not Authorized) RO-Zero
b. (bits (8 * 32) - 1 to [Num Port Table Entries]) RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8).

Port Table Entry (n) Port Capability ([table] + ([n] * [size])) + 00h — DWORD
(for Switch Ports)

a. Port Present
 (if VS is Authorized) RO
 (if VS is not Authorized) RO-Zero
b. Non-PCIe Port (Management Port)
 (if VS is Authorized) RO
 (if VS is not Authorized) RO-Zero
c. Link MR Capable
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RO
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
d. Link Direction Supported
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RO
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO
 (if VS is not Authorized) RO-Zero
e. Port Direction Supported
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RO
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO
 (if VS is not Authorized) RO-Zero
f. RsvdZ_15-8 RO-Zero
g. MaxVH
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0
 and Link MR Capable is 1) RO
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0
 and Link MR Capable is 0) RO-Zero
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
h. PCIe Offset
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RO
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested.

Port Table Entry (n) Port Control 1 ([table] + ([n] * [size])) + 04h — DWORD
(for Switch Ports)

a. Port DL_Up Interrupt Enable
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RW
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
b. Port DL_Down Interrupt Enable
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RW
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
c. Port PCIe Capability Interrupt Enable
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RW
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
d. Link Retrain Interrupt Enable
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RW
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
e. Beacon/WAKE# Interrupt Enable
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RW or RO-Zero
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
f. MR Uncorrectable Fatal TLP Error Interrupt Enable
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RW
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
g. RsvdP_6 RO-Zero
h. MR Uncorrectable Global Key Error Interrupt Enable
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RW
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
i. MR Correctable Global Key Error Interrupt Enable
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0 and VS Global Key Entering Check Supported is 1) RW
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0 and VS Global Key Exiting Check Supported is 1) RW
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0 and VS Global Key Entering Check Supported is 0

and VS Global Key Exiting Check Supported is 0)	RO-Zero
(if VS is Authorized and Non-PCIe Port (Management Port) is 1)	RO-Zero
(if VS is not Authorized)	RO-Zero

j. RsvdP_9 RO-Zero

k. Physical Hot-Plug Interrupt Enable

(if VS is Authorized and Non-PCIe Port (Management Port) is 0)	RW
(if VS is Authorized and Non-PCIe Port (Management Port) is 1)	RO-Zero
(if VS is not Authorized)	RO-Zero

l. RsvdP_15-11 RO-Zero

m. NumVH

(if VS is Authorized and Non-PCIe Port (Management Port) is 0)	
after first writing MR Enable with 0	RW
after first writing MR Enable with 1	RO
(if VS is Authorized and Non-PCIe Port (Management Port) is 1)	RO-Zero
(if VS is not Authorized)	RO-Zero

n. RsvdP_30-24 RO-Zero

o. MR Enable

(if VS is Authorized and Non-PCIe Port (Management Port) is 0)	RW
(if VS is Authorized and Non-PCIe Port (Management Port) is 1)	RO-Zero
(if VS is not Authorized)	RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested.

Port Table Entry (n) Port Control 2 ([table] + ([n] * [size])) + 08h — DWORD

(for Switch Ports)

a. Port Enable

(if VS is Authorized and Non-PCIe Port (Management Port) is 0)	RW
(if VS is Authorized and Non-PCIe Port (Management Port) is 1)	RO-Zero
(if VS is not Authorized)	RO-Zero

b. Link MR-IOV Enable

(if VS is Authorized and Non-PCIe Port (Management Port) is 0 and Link MR Capable is 1)	RW
(if VS is Authorized and Non-PCIe Port (Management Port) is 0 and Link MR Capable is 0)	RO-Zero
(if VS is Authorized and Non-PCIe Port (Management Port) is 1)	RO-Zero
(if VS is not Authorized)	RO-Zero

c. RsvdP_7-2 RO-Zero

d. Link Direction Control

(if VS is Authorized and Non-PCIe Port (Management Port) is 0) (only those values supported in Link Direction Supported are written)	RW
(if VS is Authorized and Non-PCIe Port (Management Port) is 1)	RO-Zero
(if VS is not Authorized)	RO-Zero

e. RsvdP_11-10 RO-Zero
f. PM_PME Triggers Beacon/WAKE#
(if VS is Authorized and Non-PCIe Port (Management Port) is 0) RW
(if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
(if VS is not Authorized) RO-Zero
g. Send PME_Enter_L23 DLLP RO-Zero
h. Port Direction Control
(if VS is Authorized and Non-PCIe Port (Management Port) is 0 and Port Direction Supported is 11b) RW
(if VS is Authorized and Non-PCIe Port (Management Port) is 0 and Port Direction Supported is 10b) RO-Ones
(if VS is Authorized and Non-PCIe Port (Management Port) is 0 and Port Direction Supported is 01b) RO-Zero
(if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
(if VS is not Authorized) RO-Zero
i. RsvdP_15 RO-Zero
j. VL Enable
(if VS is Authorized and Non-PCIe Port (Management Port) is 0)
(for bit 0) RO-Ones
(for bits [MaxVL] to 1) RW
(for bits 7 to [MaxVL] + 1) RO-Zero
(if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
(if VS is not Authorized) RO-Zero
k. RsvdP_31-24 RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested.

Port Table Entry (n) Port Status ([table] + ([n] * [size])) + 0Ch — DWORD

(for Switch Ports)
a. Port DL_Up Interrupt Status
(if VS is Authorized and Non-PCIe Port (Management Port) is 0) RW1C
(if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
(if VS is not Authorized) RO-Zero
b. Port DL_Down Interrupt Status
(if VS is Authorized and Non-PCIe Port (Management Port) is 0) RW1C
(if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
(if VS is not Authorized) RO-Zero
c. Port PCIe Capability Interrupt Status
(if VS is Authorized and Non-PCIe Port (Management Port) is 0) RW1C
(if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
(if VS is not Authorized) RO-Zero
d. Link Retrain Interrupt Status

(if VS is Authorized and Non-PCIe Port (Management Port) is 0)	RW1C
(if VS is Authorized and Non-PCIe Port (Management Port) is 1)	RO-Zero
(if VS is not Authorized)	RO-Zero
e. Beacon/WAKE# Interrupt Status	
(if VS is Authorized and Non-PCIe Port (Management Port) is 0)	RW1C or RO-Zero
(if VS is Authorized and Non-PCIe Port (Management Port) is 1)	RO-Zero
(if VS is not Authorized)	RO-Zero
f. RsvdZ_9-5	RO-Zero
g. Physical Hot-Plug Interrupt Status	
(if VS is Authorized and Non-PCIe Port (Management Port) is 0)	RW1C
(if VS is Authorized and Non-PCIe Port (Management Port) is 1)	RO-Zero
(if VS is not Authorized)	RO-Zero
h. RsvdZ_15-11	RO-Zero
i. VL Negotiation Pending	
(if VS is Authorized and Non-PCIe Port (Management Port) is 0)	RO
(if VS is Authorized and Non-PCIe Port (Management Port) is 1)	RO-Zero
(if VS is not Authorized)	RO-Zero
j. RsvdZ_31-24	RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested.

Port Table Entry (n) Link Partner Training Status ([table] + ([n] * [size])) + 10h — DWORD

(for Switch Ports)

a. Link Partner Detected	
(if VS is Authorized and Non-PCIe Port (Management Port) is 0)	RO
(if VS is Authorized and Non-PCIe Port (Management Port) is 1)	RO-Zero
(if VS is not Authorized)	RO-Zero
b. Link Direction Status	
(if VS is Authorized and Non-PCIe Port (Management Port) is 0)	RO
(if VS is Authorized and Non-PCIe Port (Management Port) is 1)	RO-Zero
(if VS is not Authorized)	RO-Zero
c. Link Partner is MR	
(if VS is Authorized and Non-PCIe Port (Management Port) is 0)	RO
(if VS is Authorized and Non-PCIe Port (Management Port) is 1)	RO-Zero
(if VS is not Authorized)	RO-Zero
d. RsvdZ_7-4	RO-Zero
e. Link Partner MaxVH	
(if VS is Authorized and Non-PCIe Port (Management Port) is 0)	RO
(if VS is Authorized and Non-PCIe Port (Management Port) is 1)	RO-Zero
(if VS is not Authorized)	RO-Zero

f. Link Partner MaxVL
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RO
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
g. RsvdZ_19 RO-Zero
h. Link Partner Protocol Version
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RO
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
i. Link Partner was Authorized
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RO
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
j. Link Partner Device/Port Type
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RO
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
k. Link Partner Mixed Device/Port Type
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RO
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
l. RsvdZ_29 RO-Zero
m. Link Partner VH FC
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RO
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
n. RsvdZ_31 RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested.

Port Table Entry (n) VL Arbitration Capability and Status ([table] + ([n] * [size])) + 14h – – DWORD

(for Switch Ports)
a. VL Arbitration Capability
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0
 and MaxVL is non-zero)
 (bits 11, 5-0) RO
 (bits 10-6) RO-Zero
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0
 and MaxVL is 0) RO-Zero
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero

b. VL Arbitration Status
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RO
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
c. RsvdZ_13 RO-Zero
d. Reference Clock
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RO-Zero
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
e. MaxVL
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RO
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
f. RsvdZ_23-19 RO-Zero
g. Maximum Time Slots
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RO
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
h. RsvdZ_31 RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested.

Port Table Entry (n) VL Arbitration Control ([table] + ([n] * [size])) + 18h — DWORD
(for Switch Ports)

a. Load VL Arbitration Table RO-Zero
b. RsvdP_7-1 RO-Zero
c. VL Arbitration Select
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0
 and MaxVL is non-zero) RW
 (only values corresponding to those reported in VL Arbitration Capability are written)
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0
 and MaxVL is 0) RO-Zero
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
d. RsvdP_15-12 RO-Zero
e. VL Strict Priority Arbitration
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0
 and MaxVL is non-zero) RW
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0
 and MaxVL is 0) RO-Zero
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero

f. RsvdP_31-24 RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested.

Port Table Entry (n) VL Arbitration Table Offset ([table] + ([n] * [size])) + 1Ch — DWORD

(for Switch Ports)

a. RsvdZ_1-0 RO-Zero
b. VL Arbitration Table Offset
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RO
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested.

Port Table Entry (n) MR Error Status ([table] + ([n] * [size])) + 20h — WORD

(for Switch Ports)

a. MR First Error Pointer
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) ROS
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
b. MR Uncorrectable Fatal TLP Error Status
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RW1CS
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
c. RsvdZ_5 RO-Zero
d. MR Uncorrectable Global Key Error Status
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) RW1CS
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
e. MR Correctable Global Key Error Status
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0
 and VS Global Key Entering Check Supported is 1) RW1CS
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0
 and VS Global Key Exiting Check Supported is 1) RW1CS
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0

and VS Global Key Entering Check Supported is 0
and VS Global Key Exiting Check Supported is 0) RO-Zero
(if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
(if VS is not Authorized) RO-Zero

f. RsvdZ_14-8 RO-Zero

g. MR Multiple Uncorrectable Error
(if VS is Authorized and Non-PCIe Port (Management Port) is 0) RW1CS
(if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
(if VS is not Authorized) RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested.

Port Table Entry (n) MR Error Control ([table] + ([n] * [size])) + 22h — WORD

(for Switch Ports)

a. RsvdP_3-0 RO-Zero

b. MR Uncorrectable Fatal TLP Error Mask
(if VS is Authorized and Non-PCIe Port (Management Port) is 0) RWS
(if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
(if VS is not Authorized) RO-Zero

c. RsvdP_5 RO-Zero

d. MR Uncorrectable Global Key Error Mask
(if VS is Authorized and Non-PCIe Port (Management Port) is 0) RWS
(if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
(if VS is not Authorized) RO-Zero

e. MR Correctable Global Key Error Mask
(if VS is Authorized and Non-PCIe Port (Management Port) is 0
and VS Global Key Entering Check Supported is 1) RWS
(if VS is Authorized and Non-PCIe Port (Management Port) is 0
and VS Global Key Exiting Check Supported is 1) RWS
(if VS is Authorized and Non-PCIe Port (Management Port) is 0
and VS Global Key Entering Check Supported is 0
and VS Global Key Exiting Check Supported is 0) RO-Zero
(if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
(if VS is not Authorized) RO-Zero

f. RsvdP_15-8 RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the

value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested.

Port Table Entry (n) Header Log Register ([table] + ([n] * [size])) + 24h — 9 DWORDS
(for Switch Ports)

a. Header Log register (1st DW)
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) ROS
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
b. Header Log register (2nd DW)
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) ROS
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
c. Header Log register (3rd DW)
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) ROS
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
d. Header Log register (4th DW)
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) ROS
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
e. Header Log register (5th DW)
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) ROS
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
f. Header Log register (6th DW)
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) ROS
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
g. Header Log register (7th DW)
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) ROS
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
h. Header Log register (8th DW)
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) ROS
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero
i. Header Log register (9th DW)
 (if VS is Authorized and Non-PCIe Port (Management Port) is 0) ROS
 (if VS is Authorized and Non-PCIe Port (Management Port) is 1) RO-Zero
 (if VS is not Authorized) RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the

value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested.

Port Table Entry (n) Reserved ([table] + ([n] * [size])) + 48h + ([m] * 4) — [r] DWORDS
(for Switch Ports)
(all bits) RO-Zero

(This group of registers only exists if [r] is larger than 0, and therefore this group of registers is not tested if this condition is not true. The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. The value of [r] is ([offset] - (19 * 4) / 4). All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. All values of [m] between 0 and (([offset] - (19 * 4) / 4) - 1) must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4.

Port Table Entry (n) PCI Bridge Control ([table] + ([n] * [size])) + [offset] + 00h — WORD
(for Switch Ports, if PCIe Offset is non-zero)
a. Secondary Bus Reset RW
b. RsvdP_15-1 RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested.

Port Table Entry (n) PCI Express Capabilities ([table] + ([n] * [size])) + [offset] + 02h — WORD
(for Switch Ports, if PCIe Offset is non-zero)
a. Capability Version RO
b. Device/Port Type RO-Zero
c. Slot Implemented HwInit
d. Interrupt Message Number RO-Zero
e. Undefined_14 RO
Note: This was once TCS Routing Supported.
f. RsvdP_15 RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested.

Port Table Entry (n) Device Capabilities ([table] + ([n] * [size])) + [offset] + 04h — DWORD

(for Switch Ports, if PCIe Offset is non-zero)

a. Max_Payload_Size Supported	RO
b. Phantom Functions Supported	RO-Zero
c. Extended Tag Field Supported	RO
d. Endpoint L0s Acceptable Latency	RO-Zero
e. Endpoint L1 Acceptable Latency	RO-Zero
f. Undefined_12 Note: This was once Attention Button Present.	RO
g. Undefined_13 Note: This was once Attention Indicator Present.	RO
h. Undefined_14 Note: This was once Power Indicator Present.	RO
i. Role-Based Error Reporting	RO-Ones
j. RsvdP_17-16	RO-Zero
k. Captured Slot Power Limit Value	RO
l. Captured Slot Power Limit Scale	RO
m. Function Level Reset Capability	RO-Zero
n. RsvdP_31-29	RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested.

Port Table Entry (n) Device Control ([table] + ([n] * [size])) + [offset] + 08h — WORD

(for Switch Ports, if PCIe Offset is non-zero)

a. Correctable Error Reporting Enable	RO-Zero
b. Non-Fatal Error Reporting Enable	RO-Zero
c. Fatal Error Reporting Enable	RO-Zero
d. Unsupported Request Reporting Enable	RO-Zero
e. Enable Relaxed Ordering	RO-Zero
f. Max_Payload_Size	RO-Zero
g. Extended Tag Field Enable	RO-Zero

h. Phantom Functions Enable	RO-Zero
i. Aux Power PM Enable	
(if Aux Current is non-zero in PM Capability)	RWS
(if Aux Current is 000b in PM Capability)	RWS or RO-Zero
j. Enable No Snoop	RO-Zero
k. Max_Read_Request_Size	RO-Zero
l. Bridge Configuration Retry Enable /Initiate Function Level Reset	RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested.

Port Table Entry (n) Device Status ([table] + ([n] * [size])) + [offset] + 0Ah — WORD
(for Switch Ports, if PCIe Offset is non-zero)

a. Correctable Error Detected	RO-Zero
b. Non-Fatal Error Detected	RO-Zero
c. Fatal Error Detected	RO-Zero
d. Unsupported Request Detected	RO-Zero
e. AUX Power Detected	RO
f. Transactions Pending	RO-Zero
g. Emergency Power Reduction Detected	RO-Zero
(For Base 3.1 or later testing)	
(if Port Direction Control is 1 (downstream port))	RO-Zero
(if Port Direction Control is 0 (upstream port))	
(if Port Table Entry Emergency Power Reduction Supported is not 00b)	RW1C
(if Port Table Entry Emergency Power Reduction Supported is 00b)	RO-Zero
h. RsvdZ_15-7	
(For Base 3.1 or later testing)	RO-Zero
i. RsvdZ_15-6	
(For Base 3.0 or earlier testing)	RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of

[offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested.

Port Table Entry (n) Link Capabilities ([table] + ([n] * [size])) + [offset] + 0Ch — DWORD

(for Switch Ports, if PCIe Offset is non-zero)

a.	Max Link Speed/Supported Link Speeds	RO
b.	Maximum Link Width	RO
c.	Active State Power Management (ASPM) Support	RO
d.	L0s Exit Latency	RO
e.	L1 Exit Latency	RO
f.	Clock Power Management	
	(if Port Direction Control is 1 (downstream port))	RO
	(if Port Direction Control is 0 (upstream port))	RO-Zero
g.	Surprise Down Error Reporting Capable	RO-Ones
h.	Data Link Layer Link Active Reporting Capable	RO-Ones
i.	Link Bandwidth Notification Capability	RO-Ones
j.	ASPM Optionality Compliance	
	(For Base 2.x or later testing)	HwInit
k.	RsvdP_23	
	(For Base 2.x or later testing)	RO-Zero
l.	RsvdP_23-22	
	(For Base 1.x testing)	RO-Zero
m.	Port Number	RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested.

Port Table Entry (n) Link Control ([table] + ([n] * [size])) + [offset] + 10h — WORD

(for Switch Ports, if PCIe Offset is non-zero)

a.	Active State Power Management (ASPM) Control	RW
b.	RsvdP_2	RO-Zero
c.	Read Completion Boundary (RCB)	RO-Zero
d.	Link Disable	
	(if Link Direction Supported (bit 2) is 1)	RW
	(if Link Direction Supported (bit 2) is 0 and Port Direction Control is 1 (downstream port))	RW
	(if Link Direction Supported (bit 2) is 0 and Port Direction Control is 0 (upstream port))	RO-Zero
e.	Retrain Link	RO-Zero
f.	Common Clock Configuration	RW
g.	Extended Synch	

(for any Switch Port with M-PCIe Extended Capability)	RW or RO-Zero
(for any Switch Port without M-PCIe Extended Capability)	RW
h. Enable Clock Power Management	
(if Port Direction Control is 1 (downstream port))	RO-Zero
(if Port Direction Control is 0 (upstream port) and Port Table Entry Clock Power Management as 1)	RW
i. Hardware Autonomous Width Disable	RW or RO-Zero
j. Link Bandwidth Management Interrupt Enable	
(if Port Direction Control is 1 (downstream port))	RW
(if Port Direction Control is 0 (upstream port))	RO-Zero
k. Link Autonomous Bandwidth Interrupt Enable	
(if Port Direction Control is 1 (downstream port))	RW
(if Port Direction Control is 0 (upstream port))	RO-Zero
l. RsvdP_15-12	
(For Base 2.x or earlier testing)	RO-Zero
m. RsvdP_13-12	
(For Base 3.x or later testing)	RO-Zero
n. DRS Signaling Control	
(For Base 3.x or later testing)	
(if Port Direction Control is 1 (downstream port) and DRS Supported as 1)	RW
(if Port Direction Control is 1 (downstream port) and DRS Supported as 0)	RO-Zero
(if Port Direction Control is 0 (upstream port))	RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested.

Port Table Entry (n) Link Status ([table] + ([n] * [size])) + [offset] + 12h — WORD

(for Switch Ports, if PCIe Offset is non-zero)

a. Current Link Speed	RO
b. Negotiated Link Width	RO
c. Undefined_10	RO
Note: This was once Link Training Error.	
d. Link Training	
(if Port Direction Control is 1 (downstream port))	RO
(if Port Direction Control is 0 (upstream port))	RO-Zero
e. Slot Clock Configuration	HwInit
f. Data Link Layer Link Active	
(if Port Direction Control is 1 (downstream port))	RO
(if Port Direction Control is 0 (upstream port))	RO-Zero

g. Link Bandwidth Management Status
 (if Port Direction Control is 1 (downstream port)) RW1C
 (if Port Direction Control is 0 (upstream port)) RO-Zero
h. Link Autonomous Bandwidth Status
 (if Port Direction Control is 1 (downstream port)) RW1C
 (if Port Direction Control is 0 (upstream port)) RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested.

Port Table Entry (n) Slot Capabilities ([table] + ([n] * [size])) + [offset] + 14h — DWORD
(for Switch Ports, if PCIe Offset is non-zero)

a. Attention Button Present HwInit
b. Power Controller Present HwInit
c. MRL Sensor Present HwInit
d. Attention Indicator Present HwInit
e. Power Indicator Present HwInit
f. Hot-Plug Surprise HwInit
g. Hot-Plug Capable HwInit
h. Slot Power Limit Value HwInit
i. Slot Power Limit Scale HwInit
j. Electromechanical Interlock Present HwInit
k. No Command Completed Support HwInit
l. Physical Slot Number HwInit

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested. If Port Table Entry Slot Implemented is 0, then the entire register is tested as RO-Zero.

Port Table Entry (n) Slot Control ([table] + ([n] * [size])) + [offset] + 18h — WORD
(for Switch Ports, if PCIe Offset is non-zero)

a. Attention Button Pressed Enable
 (if Port Table Entry Attention Button Present is 1) RW

(if Port Table Entry Attention Button Present is 0) RW or RO-Zero

b. Power Fault Detected Enable RW or RO-Zero

c. MRL Sensor Changed Enable
(if Port Table Entry MRL Sensor Present is 1) RW
(if Port Table Entry MRL Sensor Present is 0) RW or RO-Zero

d. Presence Detect Changed Enable
(if Port Table Entry Hot-Plug Capable is 1) RW
(if Port Table Entry Hot-Plug Capable is 0) RW or RO-Zero

e. Command Completed Interrupt Enable
(if Port Table Entry No Command Completed Support is 0) RW
(if Port Table Entry No Command Completed Support is 1) RO-Zero

f. Hot-Plug Interrupt Enable
(if Port Table Entry Hot-Plug Capable is 1) RW
(if Port Table Entry Hot-Plug Capable is 0) RW or RO-Zero

g. Attention Indicator Control
(if Port Table Entry Attention Indicator Present is 1
and Port Table Entry No Command Completed Support is 1) RW
(if Port Table Entry Attention Indicator Present is 0) RW or RO-Zero

h. Power Indicator Control
(if Port Table Entry Power Indicator Present is 1
and Port Table Entry No Command Completed Support is 1) RW
(if Port Table Entry Power Indicator Present is 0) RW or RO-Zero

i. Power Controller Control
(if Port Table Entry Power Controller Present is 1
and Port Table Entry No Command Completed Support is 1) RW
Note: Writing Power Controller Control with 1 in a Downstream Port with a slot causes the slot to power off. The test should restore this field to 0 when completing testing of this register.

j. Electromechanical Interlock Control RO-Zero
Note: The Electromechanical Interlock Control field always returns 0 when read.

k. Data Link Layer State Changed Enable
(if Port Table Entry Data Link Layer Link Active Reporting Capable is 1) RW
(if Port Table Entry Data Link Layer Link Active Reporting Capable is 0) RW or RO-Zero

l. RsvdP_15-13
(For Base 2.x or earlier testing) RO-Zero

m. Auto Slot Power Limit Disable
(For Base 3.x or later testing)
(if Port Direction Control is 1 (downstream port)
and DPC Extended Capability is present) RW
(if Port Direction Control is 1 (downstream port)

and DPC Extended Capability is not present)	RW or RO-Zero
(otherwise)	RO-Zero

n. RsvdP_15-14

(For Base 3.x or later testing)	RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested. If Port Table Entry Slot Implemented is 0, then the entire register is tested as RO-Zero.

Port Table Entry (n) Slot Status ([table] + ([n] * [size])) + [offset] + 1Ah — WORD

(for Switch Ports, if PCIe Offset is non-zero)

a. Attention Button Pressed

(if Port Table Entry Attention Button Present is 1)	RW1C
(if Port Table Entry Attention Button Present is 0)	RO-Zero

b. Power Fault Detected

(if Port Table Entry Power Controller Present is 1)	RW1C
(if Port Table Entry Power Controller Present is 0)	RO-Zero

c. MRL Sensor Changed

(if Port Table Entry MRL Sensor Present is 1)	RW1C
(if Port Table Entry MRL Sensor Present is 0)	RO-Zero

d. Presence Detect Changed — RW1C
Note: The Presence Detect Changed field cannot be tested for default value on form factors that don't provide an out-of-band presence signal, as in-band presence will be cleared upon entry to Detect state, and will be updated with a fresh value upon exit from Detect state, which can result in a presence change.

e. Command Completed

(if Port Table Entry No Command Completed Support is 0)	RW1C
(if Port Table Entry No Command Completed Support is 1)	RO-Zero

f. MRL Sensor State — RO
g. Presence Detect State — RO
h. Electromechanical Interlock Status — RO
i. Data Link Layer State Changed — RW1C
j. RsvdZ_15-9 — RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the

value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested. If Port Table Entry Slot Implemented is 0, then the entire register is tested as RO-Zero.

Port Table Entry (n) Device Capabilities 2 ([table] + ([n] * [size])) + [offset] + 1Ch — DWORD

(for Switch Ports, if PCIe Offset is non-zero)

a. Completion Timeout Ranges Supported	RO-Zero
b. Completion Timeout Disable Supported	RO-Zero
c. ARI Forwarding Supported	RO-Zero
d. AtomicOp Routing Supported (For Base 2.x or later testing)	RO
e. 32-bit AtomicOp Completer Supported (For Base 2.x or later testing)	RO
f. 64-bit AtomicOp Completer Supported (For Base 2.x or later testing)	RO
g. 128-bit CAS Completer Supported (For Base 2.x or later testing)	RO
h. No RO-enabled PR-PR Passing (For Base 2.x or later testing)	HwInit
i. LTR Mechanism Supported (For Base 2.x or later testing)	RO
j. TPH Completer Supported (For Base 2.x or later testing)	RO-Zero
k. RsvdP_17-14 (For Base 2.x)	RO-Zero
l. LN System CLS (For Base 3.x or later testing)	RO-Zero
m. 10-Bit Tag Completer Supported (For Base 4.x or later testing)	HwInit
n. 10-Bit Tag Requester Supported (For Base 4.x or later testing)	HwInit
o. RsvdP_17-16 (For Base 3.x or earlier testing)	RO-Zero
p. OBFF Supported (For Base 2.x or later testing)	HwInit
q. Extended Fmt Field Supported (For Base 2.x or later testing)	RO
r. End-End TLP Prefix Supported (For Base 2.x or later testing)	HwInit
s. Max End-End TLP Prefixes (For Base 2.x or later testing)	RO-Zero
t. Emergency Power Reduction Supported (For Base 3.1 or later testing) (if Port Direction Control is 1 (downstream port)) (if Port Direction Control is 0 (upstream port))	 RO-Zero HwInit

u. Emergency Power Reduction Initialization Required
(For Base 3.1 or later testing)
(if Port Direction Control is 1 (downstream port)) RO-Zero
(if Port Direction Control is 0 (upstream port)) HwInit
v. RsvdP_30-27
(For Base 3.1 or later testing) RO-Zero
w. RsvdP_30-24
(For Base 3.0 testing) RO-Zero
x. FRS Supported
(For Base 3.x or later testing) HwInit

y. RsvdP_31-24
(For Base 2.x testing) RO-Zero
z. RsvdP_31-6
(For Base 1.x testing) RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested.

Port Table Entry (n) Device Control 2 ([table] + ([n] * [size])) + [offset] + 20h — WORD
(for Switch Ports, if PCIe Offset is non-zero)
a. Completion Timeout Value RO-Zero
b. Completion Timeout Disable RO-Zero
c. ARI Forwarding Enable RO-Zero
d. AtomicOp Requester Enable
(For Base 2.x or later testing) RO-Zero
e. AtomicOp Egress Blocking
(For Base 2.x or later testing)
(if Port Table Entry AtomicOp Routing Supported is 1) RW
(if Port Table Entry AtomicOp Routing Supported is 0) RO-Zero
f. IDO Request Enable
(For Base 2.x or later testing) RO-Zero
g. IDO Completion Enable
(For Base 2.x or later testing) RO-Zero
h. LTR Mechanism Enable
(For Base 2.x or later testing)
(if Port Table Entry LTR Mechanism Supported is 1) RW
(if Port Table Entry LTR Mechanism Supported is 0) RW or RO-Zero
i. Emergency Power Reduction Request
(For Base 3.1 or later testing)

(if Port Direction Control is 1 (downstream port)) RO-Zero
(if Port Direction Control is 0 (upstream port))
(if Port Table Entry Emergency Power Reduction Supported not 00b) RW
(if Port Table Entry Emergency Power Reduction Supported 00b) RO-Zero

j. 10-Bit Tag Requester Enable
(For Base 4.x or later testing)
(if Port Table Entry 10-Bit Tag Requester Supported is 1) RW
(if Port Table Entry 10-Bit Tag Requester Supported is 0) RW or RO-Zero

k. RsvdP_12
(For Base 3.1 testing) RO-Zero

l. RsvdP_12-11
(For Base 3.0 or Base 2.x testing) RO-Zero

m. OBFF Enable
(For Base 2.x or later testing)
(if Port Table Entry OBFF Supported is non-zero) RW
(if Port Table Entry OBFF Supported is 0) RW or RO-Zero

n. End-End TLP Prefix Blocking
(For Base 2.x or later testing)
(if Port Table Entry End-End TLP Prefix Supported is 1) RW
(if Port Table Entry End-End TLP Prefix Supported is 0) RO-Zero

o. RsvdP_15-6
(For Base 1.x testing) RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested.

Port Table Entry (n) Device Status 2 ([table] + ([n] * [size])) + [offset] + 22h — WORD
(for Switch Ports, if PCIe Offset is non-zero)

a. RsvdZ_15-0 RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of

[offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested.

Port Table Entry (n) Link Capabilities 2 ([table] + ([n] * [size])) + [offset] + 24h — DWORD

(for Switch Ports, if PCIe Offset is non-zero)

a. RsvdP_0
 (For Base 3.x or later testing) RO-Zero
b. Supported Link Speeds Vector
 (For Base 3.x or later testing) RO
c. Crosslink Supported
 (For Base 3.x or later testing) RO
d. Lower SKP OS Generation Supported Speeds Vector
 (For Base 3.x or later testing) HwInit
e. Lower SKP OS Reception Supported Speeds Vector
 (For Base 3.x or later testing) HwInit
f. Retimer Presence Detect Supported
 (For Base 4.x or later testing) HwInit
 (For Base 3.x testing)
 (for Downstream Ports) HwInit
 (for Upstream Ports) RO-Zero
g. Two Retimers Presence Detect Supported
 (For Base 4.x or later testing) HwInit
h. RsvdP_30-25
 (For Base 4.x or later testing) RO-Zero
i. RsvdP_30-24
 (For Base 3.x testing) RO-Zero
j. DRS Supported
 (For Base 3.x or later testing) HwInit
k. RsvdP_31-0
 (For Base 2.x or earlier testing) RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested.

Port Table Entry (n) Link Control 2 ([table] + ([n] * [size])) + [offset] + 28h — WORD

(for Switch Ports, if PCIe Offset is non-zero)

a. Target Link Speed
 (For Base 2.x or later testing)

(if Port Table Entry Max Link Speed/Supported Link Speeds is 0001b) RWS or RO-Zero

(if Port Table Entry Max Link Speed/Supported Link Speeds is 0010b or greater) RWS

Note: This test must only write supported values as reported in the Port Table Entry Max Link Speed/Supported Link Speeds field.

b. Enter Compliance

(For Base 2.x or later testing)

(if Port Table Entry Max Link Speed/Supported Link Speeds is 0001b) RWS or RO-Zero

(if Port Table Entry Max Link Speed/Supported Link Speeds is 0010b or greater) RW

Note: During non-FLR testing, the Enter Compliance field cannot be tested for stickiness even though its specified register field attribute is RWS because this field is reset to zero (upon exiting Polling.Compliance) during successful link training.

Note: The Enter Compliance field cannot be tested for default value, as setting it to 1 and then doing a Hot Reset (secondary bus reset) or DL_Down (link disable/enable), will cause the link to go to Compliance Pattern state and it may not return to L0 again.

c. Hardware Autonomous Speed Disable

(For Base 2.x or later testing) RWS or RO-Zero

d. Selectable De-emphasis

(For Base 2.x or later testing)

(if Port Direction Control is 0 (upstream port)) RO-Zero

(if Port Direction Control is 1 (downstream port)) HwInit

e. Transmit Margin

(For Base 2.x or later testing)

(for any Switch Port with M-PCIe Extended Capability, or any Switch Port without M-PCIe Extended Capability and with Port Table Entry Max Link Speed/Supported Link Speeds as 0001b) RWS or RO-Zero

(for any Switch Port without M-PCIe Extended Capability and with Port Table Entry Max Link Speed/Supported Link Speeds as 0010b or greater) RW

Note: During non-FLR testing, the Transmit margin field cannot be tested for stickiness even though its specified register field attribute is RWS because this field is reset to zero (in Polling.Configuration) during successful link training.

f. Enter Modified Compliance

(For Base 2.x or later testing)

(for any Switch Port with M-PCIe Extended Capability, or any Switch Port without M-PCIe Extended Capability and with Port Table Entry Max Link Speed/Supported Link Speeds as 0001b) RWS or RO-Zero

(for any Switch Port without M-PCIe Extended Capability and with Port Table Entry Max Link Speed/Supported Link Speeds as 0010b or greater) RWS

g. Compliance SOS
(For Base 2.x or later testing)
(for any Switch Port with M-PCIe Extended Capability,
or any Switch Port without M-PCIe Extended Capability
and with Port Table Entry Max Link Speed/Supported Link Speeds as 0001b)
RWS or
RO-Zero
(for any Switch Port without M-PCIe Extended Capability
and with Port Table Entry Max Link Speed/Supported Link Speeds as 0010b or greater)
RWS

h. Compliance Preset/De-emphasis
(For Base 3.x or later testing)
(for any Switch Port with M-PCIe Extended Capability,
or any Switch Port without M-PCIe Extended Capability
and with Port Table Entry Max Link Speed/Supported Link Speeds as 0001b)
RWS or
RO-Zero
(for any Switch Port without M-PCIe Extended Capability
and with Port Table Entry Max Link Speed/Supported Link Speeds as 0010b or greater)
RWS
Note: For Base 3.x or later, this field consists of bits 15-12 of this register.

i. Compliance De-emphasis
(For Base 2.x testing)
(if Port Table Entry Max Link Speed/Supported Link Speeds is 0001b) RWS or
RO-Zero
(if Port Table Entry Max Link Speed/Supported Link Speeds is 0010b
or greater) RWS
Note: For Base 2.x, this field consists of bit 12 of this register.

j. RsvdP_15-13
(For Base 2.x testing) RO-Zero

k. RsvdP_15-0
(For Base 1.x testing) RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested.

Port Table Entry (n) Link Status 2 ([table] + ([n] * [size])) + [offset] + 2Ah — WORD
(for Switch Ports, if PCIe Offset is non-zero)

a. Current De-emphasis Level
(For Base 2.x or later testing) RO

b. Equalization 8.0 GT/s Complete

(For Base 3.x or later testing) RO

Note: During non-FLR testing, the Equalization 8.0 GT/s Complete field cannot be tested for stickiness even though its specified register field attribute is ROS because this field is reset to zero on link down, and is then again updated during link equalization.

c. Equalization 8.0 GT/s Phase 1 Successful
(For Base 3.x or later testing) RO

Note: During non-FLR testing, the Equalization 8.0 GT/s Phase 1 Successful field cannot be tested for stickiness even though its specified register field attribute is ROS because this field is reset to zero on link down, and is then again updated during link equalization.

d. Equalization 8.0 GT/s Phase 2 Successful
(For Base 3.x or later testing) RO

Note: During non-FLR testing, the Equalization 8.0 GT/s Phase 2 Successful field cannot be tested for stickiness even though its specified register field attribute is ROS because this field is reset to zero on link down, and is then again updated during link equalization.

e. Equalization 8.0 GT/s Phase 3 Successful
(For Base 3.x or later testing) RO

Note: During non-FLR testing, the Equalization 8.0 GT/s Phase 3 Successful field cannot be tested for stickiness even though its specified register field attribute is ROS because this field is reset to zero on link down, and is then again updated during link equalization.

f. Link Equalization Request 8.0 GT/s
(For Base 3.x or later testing)
(for any Switch Port with M-PCIe Extended Capability) RW1C or RO-Zero
(for any Switch Port without M-PCIe Extended Capability and Max Link Speed/Supported Link Speeds is 0011b or greater) RW1C
(for any Switch Port without M-PCIe Extended Capability and Max Link Speed/Supported Link Speeds is less than 0011b) RW1C or RO-Zero

Note: During non-FLR testing, the Link Equalization Request 8.0 GT/s field cannot be tested for stickiness even though its specified register field attribute is RW1CS because this field is updated during link equalization.

g. Retimer Presence Detected
(For Base 4.x or later testing) RO
(For Base 3.x testing)
(if Port Direction Control is 1 (downstream port)) RO
(if Port Direction Control is 0 (upstream port)) RO-Zero

Note: During non-FLR testing, the Retimer Presence Detected field cannot be tested for stickiness even though its specified register field attribute is ROS because this field is updated during link training.

h. Two Retimers Presence Detected
(For Base 4.x or later testing) RO

Note: During non-FLR testing, the Two Retimers Presence Detected field cannot be tested for stickiness even though its specified register field attribute is ROS because this field is updated during link training.

i. Crosslink Resolution
(For Base 4.x or later testing) RO

j. RsvdZ_11-10
(For Base 4.x or later testing) RO-Zero
k. RsvdZ_11-7
(For Base 3.x testing) RO-Zero
l. Downstream Component Presence
(For Base 3.x or later testing)
(if Port Direction Control is 1 (downstream port) and DRS Supported as 1) RO
(if Port Direction Control is 1 (downstream port) and DRS Supported as 0) RO-Zero
(if Port Direction Control is 0 (upstream port)) RO-Zero
m. DRS Message Received
(For Base 3.x or later testing)
(if Port Direction Control is 1 (downstream port) and DRS Supported as 1) RW1C
(if Port Direction Control is 1 (downstream port) and DRS Supported as 0) RO-Zero
(if Port Direction Control is 0 (upstream port)) RO-Zero
n. RsvdZ_15-1
(For Base 2.x testing) RO-Zero
o. RsvdZ_15-0
(For Base 1.x testing) RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested.

Port Table Entry (n) Slot Capabilities 2 ([table] + ([n] * [size])) + [offset] + 2Ch — DWORD

(for Switch Ports, if PCIe Offset is non-zero)
a. RsvdP_31-0 RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested. If Port Table Entry Slot Implemented is 0, then the entire register is tested as RO-Zero.

Port Table Entry (n) Slot Control 2 ([table] + ([n] * [size])) + [offset] + 30h — WORD

(for Switch Ports, if PCIe Offset is non-zero)
a. RsvdP_15-0 RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested. If Port Table Entry Slot Implemented is 0, then the entire register is tested as RO-Zero.

Port Table Entry (n) Slot Status 2 ([table] + ([n] * [size])) + [offset] + 32h — WORD
(for Switch Ports, if PCIe Offset is non-zero)
a. RsvdZ_15-0 RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested. If Port Table Entry Slot Implemented is 0, then the entire register is tested as RO-Zero.

Port Table Entry (n) Reserved ([table] + ([n] * [size])) + [offset] + 34h + ([m] * 4) — [r] DWORDS
(for Switch Ports)
(all bits) RO-Zero

(This group of registers only exists if [r] is larger than 0, and therefore this group of registers is not tested if this condition is not true. The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. The value of [r] is ((([Port Table Entry Size] * 4) – (([offset] – 1) + (13 * 4))) / 4). All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. All values of [m] between 0 and (((([Port Table Entry Size] * 4) – (([offset] – 1) + (13 * 4))) / 4) – 1) must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4.

VS Interrupt Status Bitmap ([table] - 8) — 8 DWORDS
(for Switch Ports)
a. (bits [Num VS Table Entries]-1 to 0)
(for bit [n] if VS Table Entry [n] VS Present is 1 and VS is Authorized) RO
Note: All values of [n] from 0 to [Num VS Table Entries]-1 are tested.

(for bit [n] if VS Table Entry [n] VS Present is 0) RO-Zero
Note: All values of [n] from 0 to [Num VS Table Entries]-1 are tested.
(if VS is not Authorized) RO-Zero
b. (bits (8 * 32) - 1 to [Num VS Table Entries]) RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the VS Table BIR field value) plus the offset (value in the VS Table Offset field multiplied by 8).

VS Table Entry (n) VS Capability and Status ([table] + ([n] * [size])) + 00h — DWORD
(for Switch Ports)
a. VS Present
(if VS is Authorized) RO
(if VS is not Authorized) RO-Zero
b. RsvdZ_28-1 RO-Zero
c. VS Global Key Entering Check Supported
(if VS is Authorized) RO
(if VS is not Authorized) RO-Zero
d. VS Global Key Exiting Check Supported
(if VS is Authorized) RO
(if VS is not Authorized) RO-Zero
e. VS Global Key Terminating Check Supported
(if VS is Authorized) RO-Ones
(if VS is not Authorized) RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the VS Table BIR field value) plus the offset (value in the VS Table Offset field multiplied by 8). The value of [size] is the value in the VS Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num VS Table Entries field minus one inclusive must be tested.

VS Table Entry (n) VS Control ([table] + ([n] * [size])) + 04h — DWORD
(for Switch Ports)
a. VS Enable
(if VS is Authorized) RW or RO-Ones
(if VS is not Authorized) RO-Zero
b. VS Bridge Interrupt Enable
(if VS is Authorized) RW
(if VS is not Authorized) RO-Zero
c. VS Suppress Reset Propagation
(if VS is Authorized) RW
(if VS is not Authorized) RO-Zero
Note: Changing the value of this field may reset the associated link.

d. RsvdP_15-3 RO-Zero
e. VS Global Key Value
(if VS is Authorized) RW
(if VS is not Authorized) RO-Zero
f. RsvdP_28 RO-Zero
g. VS Global Key Entering Check Enable
(if VS is Authorized and VS Global Key Entering Check Supported is 1) RW
(if VS is Authorized and VS Global Key Entering Check Supported is 0) RO-Zero
(if VS is not Authorized) RO-Zero
h. VS Global Key Exiting Check Enable
(if VS is Authorized and VS Global Key Exiting Check Supported is 1) RW
(if VS is Authorized and VS Global Key Exiting Check Supported is 0) RO-Zero
(if VS is not Authorized) RO-Zero
i. VS Global Key Terminating Check Enable
(if VS is Authorized) RW
(if VS is not Authorized) RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the VS Table BIR field value) plus the offset (value in the VS Table Offset field multiplied by 8). The value of [size] is the value in the VS Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num VS Table Entries field minus one inclusive must be tested.

VS Table Entry (n) VS Bridge Interrupt Status ([table] + ([n] * [size])) + 08h – [r] DWORDS

(for Switch Ports)
a. (bits [Num VS Bridge Table Entries]-1 to 0)
(for bit [n] if VS Bridge Table Entry [n] Bridge Hardware Present is 1
and VS is Authorized) RO
Note: All values of [n] from 0 to [Num VS Bridge Table Entries]-1 are tested.
(for bit [n] if VS Bridge Table Entry [n] Bridge Hardware Present is 0) RO-Zero
Note: All values of [n] from 0 to [Num VS Bridge Table Entries]-1 are tested.
(if VS is not Authorized) RO-Zero
b. (bits ([r] * 32) - 1 to [Num VS Bridge Table Entries]) RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the VS Table BIR field value) plus the offset (value in the VS Table Offset field multiplied by 8). The value of [size] is the value in the VS Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num VS Table Entries field minus one inclusive must be tested. The value of [r] is ([Num VS Bridge Table Entries] divided by 32) rounded up to the next integer number.

VS Table Entry (n) Reserved ([table] + ([n] * [size])) + 08h + [offset] + ([m] * 4) –– [r] DWORDS

(for Switch Ports)
(all bits) RO-Zero

(This group of registers only exists if [r] is larger than 0, and therefore this group of registers is not tested if this condition is not true. The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the VS Table BIR field value) plus the offset (value in the VS Table Offset field multiplied by 8). The value of [size] is the value in the VS Table Entry Size field multiplied by 4. The value of [r] is ((([VS Table Entry Size] * 4) – ([offset] + (2 * 4))) / 4). All values of [n] between 0 and the value in the Num VS Table Entries field minus one inclusive must be tested. All values of [m] between 0 and ((((([VS Table Entry Size] * 4) – ([offset] + (2 * 4))) / 4) – 1) must be tested. The value of [offset] is ([Num VS Bridge Table Entries] divided by 32) rounded up to the next integer number multiplied by 4.

VS Bridge Table Entry (n, x) VS Bridge Capability and Status ([table] + (([n] * [bsize]) + ([x] * [size]))) + 00h –– DWORD

(for Switch Ports)

a. Bridge Hardware Present
 (if VS is Authorized) RO
 (if VS is not Authorized) RO-Zero
b. Hot-Plug Hardware Present
 (if VS is Authorized) RO
 (if VS is not Authorized) RO-Zero
c. RsvdZ_3-2 RO-Zero
d. Max Payload Size Supported
 (if VS is Authorized) RO
 (if VS is not Authorized) RO-Zero
e. RsvdZ_7 RO-Zero
f. Num VC Resources Hardware Present
 (if VS is Authorized) RO
 (if VS is not Authorized) RO-Zero
g. RsvdZ_15-11 RO-Zero
h. Link in Reset
 (if VS is Authorized and Port Mapped to Bridge is 1) RO
 (if VS is Authorized and Port Mapped to Bridge is 0) RO-Ones
 (if VS is not Authorized) RO-Zero
i. PME Turn Off State
 (if VS is Authorized) RO
 (if VS is not Authorized) RO-Zero
j. RsvdZ_26-18 RO-Zero
k. PME Turn Off State Changed
 (if VS is Authorized) RW1C
 (if VS is not Authorized) RO-Zero
l. Power Controller State Changed

(if VS is Authorized)	RW1C
(if VS is not Authorized)	RO-Zero
m. Power Indicator State Changed	
(if VS is Authorized)	RW1C
(if VS is not Authorized)	RO-Zero
n. Attention Indicator State Changed	
(if VS is Authorized)	RW1C
(if VS is not Authorized)	RO-Zero
o. VC Config Changed	
(if VS is Authorized)	RW1C
(if VS is not Authorized)	RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the VS Bridge Table BIR field value) plus the offset (value in the VS Bridge Table Offset field multiplied by 8). The value of [bsize] is the value in the Num VS Bridge Table Entries field multiplied by the VS Bridge Table Entry Size field multiplied by 4. The value of [size] is the value in the VS Bridge Table Entry Size field multiplied by 4. All values of [x] between 0 and the value in the Num VS Bridge Table Entries field minus one inclusive must be tested. All values of [n] between 0 and the value in the Num VS Table Entries field minus one inclusive must be tested.

VS Bridge Table Entry (n, x) VS Bridge Control 1 ([table] + (([n] * [bsize]) + ([x] * [size]))) + 04h — DWORD

(for Switch Ports)

a. Bridge Enable	
(if VS is Authorized and Bridge Hardware Present is 1)	RW
(if VS is Authorized and Bridge Hardware Present is 0)	RO
(if VS is not Authorized)	RO-Zero
b. Bridge Controls Physical Link	
(if VS is Authorized)	RW or RO-Zero
(if VS is not Authorized)	RO-Zero
c. VC Config Changed Interrupt Enable	
(if VS is Authorized)	RW
(if VS is not Authorized)	RO-Zero
d. PME Turn Off State Change Interrupt Enable	
(if VS is Authorized)	RW
(if VS is not Authorized)	RO-Zero
e. RsvdP_14-4	RO-Zero
f. Port Mapped to Bridge	
(if VS is Authorized and Bridge Enable is 1)	RW
(if VS is Authorized and Bridge Enable is 0)	RO-Zero
(if VS is not Authorized)	RO-Zero
g. Bridge VHN	
(if VS is Authorized) after first writing Port Mapped to Bridge with 0	RW

after first writing Port Mapped to Bridge with 1	RO
(if VS is not Authorized)	RO-Zero

h. Bridge Port

(if VS is Authorized)	
after first writing Port Mapped to Bridge with 0	RW
after first writing Port Mapped to Bridge with 1	RO
(if VS is not Authorized)	RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the VS Bridge Table BIR field value) plus the offset (value in the VS Bridge Table Offset field multiplied by 8). The value of [bsize] is the value in the Num VS Bridge Table Entries field multiplied by the VS Bridge Table Entry Size field multiplied by 4. The value of [size] is the value in the VS Bridge Table Entry Size field multiplied by 4. All values of [x] between 0 and the value in the Num VS Bridge Table Entries field minus one inclusive must be tested. All values of [n] between 0 and the value in the Num VS Table Entries field minus one inclusive must be tested.

VS Bridge Table Entry (n, x) VS Bridge Control 2 ([table] + (([n] * [bsize]) + ([x] * [size]))) + 08h — DWORD

(for Switch Ports)

a. RsvdP_3-0	RO-Zero
b. Max Payload Size Offered	
(if VS is Authorized)	RW
(if VS is not Authorized)	RO-Zero
c. RsvdP_7	RO-Zero
d. Extended VC Count	
(if VS is Authorized)	RW
(if VS is not Authorized)	RO-Zero
e. RsvdP_11	RO-Zero
f. Low Priority Extended VC Count	
(if VS is Authorized)	RW
(if VS is not Authorized)	RO-Zero
g. RsvdP_31-15	RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the VS Bridge Table BIR field value) plus the offset (value in the VS Bridge Table Offset field multiplied by 8). The value of [bsize] is the value in the Num VS Bridge Table Entries field multiplied by the VS Bridge Table Entry Size field multiplied by 4. The value of [size] is the value in the VS Bridge Table Entry Size field multiplied by 4. All values of [x] between 0 and the value in the Num VS Bridge Table Entries field minus one inclusive must be tested. All values of [n] between 0 and the value in the Num VS Table Entries field minus one inclusive must be tested.

VS Bridge Table Entry (n, x) Virtual Hot-Plug Signals Interface 1 ([table] + (([n] * [bsize]) + ([x] * [size]))) + 0Ch — DWORD

(for Switch Ports)

a. RsvdP_0	RO-Zero
b. Virtual Power Controller Present	
(if VS is Authorized and Hot-Plug Hardware Present is 1)	RW
(if VS is not Authorized)	RO-Zero
c. RsvdP_4-2	RO-Zero
d. Virtual Hot Plug Surprise	
(if VS is Authorized and Hot-Plug Hardware Present is 1)	RW
(if VS is not Authorized)	RO-Zero
e. Virtual Hot Plug Capable	
(if VS is Authorized and Hot-Plug Hardware Present is 1)	RW
(if VS is not Authorized)	RO-Zero
f. RsvdP_18-7	RO-Zero
g. Virtual Slot Number	
(if VS is Authorized and Hot-Plug Hardware Present is 1)	RW
(if VS is not Authorized)	RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the VS Bridge Table BIR field value) plus the offset (value in the VS Bridge Table Offset field multiplied by 8). The value of [bsize] is the value in the Num VS Bridge Table Entries field multiplied by the VS Bridge Table Entry Size field multiplied by 4. The value of [size] is the value in the VS Bridge Table Entry Size field multiplied by 4. All values of [x] between 0 and the value in the Num VS Bridge Table Entries field minus one inclusive must be tested. All values of [n] between 0 and the value in the Num VS Table Entries field minus one inclusive must be tested.

VS Bridge Table Entry (n, x) Virtual Hot-Plug Signals Interface 2 ([table] + (([n] * [bsize]) + ([x] * [size]))) + 10h — DWORD

(for Switch Ports)

a. Virtual Power Indicator State	
(if VS is Authorized and Hot-Plug Hardware Present is 1)	RO
(if VS is not Authorized)	RO-Zero
b. Virtual Attention Indicator State	
(if VS is Authorized and Hot-Plug Hardware Present is 1)	RO
(if VS is not Authorized)	RO-Zero
c. Virtual Power Controller State	
(if VS is Authorized and Hot-Plug Hardware Present is 1)	RO
(if VS is not Authorized)	RO-Zero
d. RsvdP_7-5	RO-Zero
e. Virtual Slot Implemented	
(if VS is Authorized and Hot-Plug Hardware Present is 1)	RW
(if VS is Authorized and Hot-Plug Hardware Present is 0)	RO-Zero
(if VS is not Authorized)	RO-Zero
f. Hot Plug Signals Interrupt Enable	

(if VS is Authorized and Hot-Plug Hardware Present is 1)	RW
(if VS is Authorized and Hot-Plug Hardware Present is 0)	RO-Zero
(if VS is not Authorized)	RO-Zero
g. RsvdP_15-10	RO-Zero
h. Virtual Discard Ingress Request	
(if VS is Authorized)	RW
(if VS is not Authorized)	RO-Zero
i. Virtual Presence Detect State	
(if VS is Authorized and Hot-Plug Hardware Present is 1)	RW
(if VS is not Authorized)	RO-Zero
j. Virtual Force Reset	
(if VS is Authorized and Port Direction Control is 1 (downstream port))	RW
(if VS is Authorized and Port Direction Control is 0 (upstream port))	RO-Zero
(if VS is not Authorized)	RO-Zero
k. Push Virtual Attention Button	RO-Zero
l. Signal Virtual Power Fault	RO-Zero
m. RsvdP_31-21	RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the VS Bridge Table BIR field value) plus the offset (value in the VS Bridge Table Offset field multiplied by 8). The value of [bsize] is the value in the Num VS Bridge Table Entries field multiplied by the VS Bridge Table Entry Size field multiplied by 4. The value of [size] is the value in the VS Bridge Table Entry Size field multiplied by 4. All values of [x] between 0 and the value in the Num VS Bridge Table Entries field minus one inclusive must be tested. All values of [n] between 0 and the value in the Num VS Table Entries field minus one inclusive must be tested.

VS Bridge Table Entry (n, x) VS Bridge VC ID to VL Map 1 ([table] + (([n] * [bsize]) + ([x] * [size]))) + 14h — DWORD

(for Switch Ports)

a. VC0 VL Map	
(if VS is Authorized and MaxVL is non-zero) after first writing VC0 VL Map Enable with 1	RW
after first writing VC0 VL Map Enable with 0	RO
(if VS is Authorized and MaxVL is 0)	RO-Zero
(if VS is not Authorized)	RO-Zero
b. RsvdP_3	RO-Zero
c. VC0 VL Map Enable	
(if VS is Authorized and MaxVL is non-zero)	RW
(if VS is Authorized and MaxVL is 0)	RO-Zero
(if VS is not Authorized)	RO-Zero
d. RsvdP_7-5	RO-Zero
e. VC1 VL Map	
(if VS is Authorized and MaxVL is non-zero and Num VC Resources Hardware Present is greater than or equal to 1)	

after first writing VC1 VL Map Enable with 1	RW
after first writing VC1 VL Map Enable with 0	RO
(if VS is Authorized and MaxVL is 0)	RO-Zero
(if VS is Authorized and Num VC Resources Hardware Present is less than 1)	RO-Zero
(if VS is not Authorized)	RO-Zero
f. RsvdP_11	RO-Zero
g. VC1 VL Map Enable	
(if VS is Authorized and MaxVL is non-zero and Num VC Resources Hardware Present is greater than or equal to 1)	RW
(if VS is Authorized and MaxVL is 0)	RO-Zero
(if VS is Authorized and Num VC Resources Hardware Present is less than 1)	RO-Zero
(if VS is not Authorized)	RO-Zero
h. RsvdP_15-13	RO-Zero
i. VC2 VL Map	
(if VS is Authorized and MaxVL is non-zero and Num VC Resources Hardware Present is greater than or equal to 2)	
after first writing VC2 VL Map Enable with 1	RW
after first writing VC2 VL Map Enable with 0	RO
(if VS is Authorized and MaxVL is 0)	RO-Zero
(if VS is Authorized and Num VC Resources Hardware Present is less than 2)	RO-Zero
(if VS is not Authorized)	RO-Zero
j. RsvdP_19	RO-Zero
k. VC2 VL Map Enable	
(if VS is Authorized and MaxVL is non-zero and Num VC Resources Hardware Present is greater than or equal to 2)	RW
(if VS is Authorized and MaxVL is 0)	RO-Zero
(if VS is Authorized and Num VC Resources Hardware Present is less than 2)	RO-Zero
(if VS is not Authorized)	RO-Zero
l. RsvdP_23-21	RO-Zero
m. VC3 VL Map	
(if VS is Authorized and MaxVL is non-zero and Num VC Resources Hardware Present is greater than or equal to 3)	
after first writing VC3 VL Map Enable with 1	RW
after first writing VC3 VL Map Enable with 0	RO
(if VS is Authorized and MaxVL is 0)	RO-Zero
(if VS is Authorized and Num VC Resources Hardware Present is less than 3)	RO-Zero
(if VS is not Authorized)	RO-Zero
n. RsvdP_27	RO-Zero
o. VC3 VL Map Enable	
(if VS is Authorized and MaxVL is non-zero and Num VC Resources Hardware Present is greater than or equal to 3)	RW
(if VS is Authorized and MaxVL is 0)	RO-Zero
(if VS is Authorized	

and Num VC Resources Hardware Present is less than 3) RO-Zero
(if VS is not Authorized) RO-Zero

p. RsvdP_31-29 RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the VS Bridge Table BIR field value) plus the offset (value in the VS Bridge Table Offset field multiplied by 8). The value of [bsize] is the value in the Num VS Bridge Table Entries field multiplied by the VS Bridge Table Entry Size field multiplied by 4. The value of [size] is the value in the VS Bridge Table Entry Size field multiplied by 4. All values of [x] between 0 and the value in the Num VS Bridge Table Entries field minus one inclusive must be tested. All values of [n] between 0 and the value in the Num VS Table Entries field minus one inclusive must be tested.

VS Bridge Table Entry (n, x) VS Bridge VC ID to VL Map 2 ([table] + (([n] * [bsize]) + ([x] * [size]))) + 18h — DWORD

(for Switch Ports)

a. VC4 VL Map
(if VS is Authorized and MaxVL is non-zero
and Num VC Resources Hardware Present is greater than or equal to 4)
after first writing VC4 VL Map Enable with 1 RW
after first writing VC4 VL Map Enable with 0 RO
(if VS is Authorized and MaxVL is 0) RO-Zero
(if VS is Authorized
and Num VC Resources Hardware Present is less than 4) RO-Zero
(if VS is not Authorized) RO-Zero

b. RsvdP_3 RO-Zero

c. VC4 VL Map Enable
(if VS is Authorized and MaxVL is non-zero
and Num VC Resources Hardware Present is greater than or equal to 4) RW
(if VS is Authorized and MaxVL is 0) RO-Zero
(if VS is Authorized
and Num VC Resources Hardware Present is less than 4) RO-Zero
(if VS is not Authorized) RO-Zero

d. RsvdP_7-5 RO-Zero

e. VC5 VL Map
(if VS is Authorized and MaxVL is non-zero
and Num VC Resources Hardware Present is greater than or equal to 5)
after first writing VC5 VL Map Enable with 1 RW
after first writing VC5 VL Map Enable with 0 RO
(if VS is Authorized and MaxVL is 0) RO-Zero
(if VS is Authorized
and Num VC Resources Hardware Present is less than 5) RO-Zero
(if VS is not Authorized) RO-Zero

f. RsvdP_11 RO-Zero

g. VC5 VL Map Enable
(if VS is Authorized and MaxVL is non-zero

and Num VC Resources Hardware Present is greater than or equal to 5)	RW
(if VS is Authorized and MaxVL is 0)	RO-Zero
(if VS is Authorized	
and Num VC Resources Hardware Present is less than 5)	RO-Zero
(if VS is not Authorized)	RO-Zero
h. RsvdP_15-13	RO-Zero
i. VC6 VL Map	
(if VS is Authorized and MaxVL is non-zero	
and Num VC Resources Hardware Present is greater than or equal to 6)	
after first writing VC6 VL Map Enable with 1	RW
after first writing VC6 VL Map Enable with 0	RO
(if VS is Authorized and MaxVL is 0)	RO-Zero
(if VS is Authorized	
and Num VC Resources Hardware Present is less than 6)	RO-Zero
(if VS is not Authorized)	RO-Zero
j. RsvdP_19	RO-Zero
k. VC6 VL Map Enable	
(if VS is Authorized and MaxVL is non-zero	
and Num VC Resources Hardware Present is greater than or equal to 6)	RW
(if VS is Authorized and MaxVL is 0)	RO-Zero
(if VS is Authorized	
and Num VC Resources Hardware Present is less than 6)	RO-Zero
(if VS is not Authorized)	RO-Zero
l. RsvdP_23-21	RO-Zero
m. VC7 VL Map	
(if VS is Authorized and MaxVL is non-zero	
and Num VC Resources Hardware Present is equal to 7)	
after first writing VC7 VL Map Enable with 1	RW
after first writing VC7 VL Map Enable with 0	RO
(if VS is Authorized and MaxVL is 0)	RO-Zero
(if VS is Authorized	
and Num VC Resources Hardware Present is less than 7)	RO-Zero
(if VS is not Authorized)	RO-Zero
n. RsvdP_27	RO-Zero
o. VC7 VL Map Enable	
(if VS is Authorized and MaxVL is non-zero	
and Num VC Resources Hardware Present is equal to 7)	RW
(if VS is Authorized and MaxVL is 0)	RO-Zero
(if VS is Authorized	
and Num VC Resources Hardware Present is less than 7)	RO-Zero
(if VS is not Authorized)	RO-Zero
p. RsvdP_31-29	RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the VS Bridge Table BIR field

value) plus the offset (value in the VS Bridge Table Offset field multiplied by 8). The value of [bsize] is the value in the Num VS Bridge Table Entries field multiplied by the VS Bridge Table Entry Size field multiplied by 4. The value of [size] is the value in the VS Bridge Table Entry Size field multiplied by 4. All values of [x] between 0 and the value in the Num VS Bridge Table Entries field minus one inclusive must be tested. All values of [n] between 0 and the value in the Num VS Table Entries field minus one inclusive must be tested.

VS Bridge Table Table Entry (n, x) Reserved ([table] + (([n] * [bsize]) + ([x] * [size]))) + 1Ch — 4 DWORDS

(for Switch Ports)

a. Reserved register (1st DW) RO-Zero
b. Reserved register (2nd DW) RO-Zero
c. Reserved register (3rd DW) RO-Zero
d. Reserved register (4th DW) RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the VS Bridge Table BIR field value) plus the offset (value in the VS Bridge Table Offset field multiplied by 8). The value of [bsize] is the value in the Num VS Bridge Table Entries field multiplied by the VS Bridge Table Entry Size field multiplied by 4. The value of [size] is the value in the VS Bridge Table Entry Size field multiplied by 4. All values of [x] between 0 and the value in the Num VS Bridge Table Entries field minus one inclusive must be tested. All values of [n] between 0 and the value in the Num VS Table Entries field minus one inclusive must be tested.

VS Bridge Table Table Entry (n, x) VC Resource State (m) ([table] + (([n] * [bsize]) + ([x] * [size]))) + 2Ch + ([m] * 4) — DWORD

(for Switch Ports)

a. VC Resource [m] VC Enabled
 (if [m] is 0) RO-Ones
 (if [m] is non-zero
 and [m] is less than or equal to Num VC Resources Hardware Present
 and [m] is less than or equal to Extended VC Count) RO
 (if [m] is non-zero
 and [m] is less than or equal to Num VC Resources Hardware Present
 and [m] is greater than Extended VC Count) RO-Zero
b. VC Resource [m] VC Negotiation Pending
 (if [m] is less than or equal to Num VC Resources Hardware Present
 and [m] is less than or equal to Extended VC Count) RO
 (if [m] is less than or equal to Num VC Resources Hardware Present
 and [m] is greater than Extended VC Count) RO-Zero
c. RsvdZ_3-2 RO-Zero
d. VC Resource [m] VC ID
 (if [m] is 0) RO-Zero
 (if [m] is non-zero
 and [m] is less than or equal to Num VC Resources Hardware Present
 and [m] is less than or equal to Extended VC Count) RO

(if [m] is non-zero
and [m] is less than or equal to Num VC Resources Hardware Present
and [m] is greater than Extended VC Count) RO-Zero

e. RsvdZ_15-7 RO-Zero

f. VC Resource [m] TC to VC Map
(if [m] is 0) RO
(if [m] is non-zero
and [m] is less than or equal to Num VC Resources Hardware Present
and [m] is less than or equal to Extended VC Count) RO
(if [m] is non-zero
and [m] is less than or equal to Num VC Resources Hardware Present
and [m] is greater than Extended VC Count) RO-Zero

g. RsvdZ_31-24 RO-Zero

(The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested. The register group is tested twice if the Num VC Resources Hardware Present field is greater than 0. The first time it is tested after the Extended VC Count field is written with the value returned in the Num VC Resources Hardware Present field. The second time it is tested after the Extended VC Count field is written with 000b, but only if the Num VC Resources Hardware Present field is greater than 0.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the VS Bridge Table BIR field value) plus the offset (value in the VS Bridge Table Offset field multiplied by 8). The value of [bsize] is the value in the Num VS Bridge Table Entries field multiplied by the VS Bridge Table Entry Size field multiplied by 4. The value of [size] is the value in the VS Bridge Table Entry Size field multiplied by 4. All values of [x] between 0 and the value in the Num VS Bridge Table Entries field minus one inclusive must be tested. All values of [n] between 0 and the value in the Num VS Table Entries field minus one inclusive must be tested. All values of [m] between 0 and the value in the Num VC Resources Hardware Present field inclusive must be tested.

Statistics Descriptor Table Entry (n) Statistics Descriptor Table Entry [table] + 00h – 8 DWORDS

(for Endpoints and Switch Ports)

a. Standard S-Bits (bits 127-0) RO

b. Group 1 Vendor Specific S-Bits (bits 167-128) RO

c. Group 1 Collection ID (bits 175-168)
(if any Group 1 Vendor Specific S-Bits are non-zero) RO
(if all Group 1 Vendor Specific S-Bits are zero) RO-Zero

d. Group 1 Vendor ID (bits 191-176)
(if any Group 1 Vendor Specific S-Bits are non-zero) RO
(if all Group 1 Vendor Specific S-Bits are zero) RO-Zero

e. Group 2 Vendor Specific S-Bits (bits 231-192) RO

f. Group 2 Collection ID (bits 239-232)
(if any Group 2 Vendor Specific S-Bits are non-zero) RO
(if all Group 2 Vendor Specific S-Bits are zero) RO-Zero

g. Group 2 Vendor ID (bits 255-240)
(if any Group 2 Vendor Specific S-Bits are non-zero) RO
(if all Group 2 Vendor Specific S-Bits are zero) RO-Zero

(This group of registers only exists if the Number of Statistics Descriptors field is non-zero, and therefore this group of registers is not tested if this condition is not true. The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.) Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Statistics Descriptor Table BIR field value) plus the offset (value in the Statistics Descriptor Table Offset field multiplied by 8). All values of [n] between 0 and the value in the Number of Statistics Descriptors field minus one inclusive must be tested.

Statistics Block Table Entry (n) Statistics Block Capability [table] + 00h –DWORD

(for Endpoints and Switch Ports)

a. Statistics Block Status	RO
b. RsvdZ_15-2	RO-Zero
c. Statistics Counter Table Size	RO

(This group of registers only exists if the Number of Statistics Blocks field is non-zero, and therefore this group of registers is not tested if this condition is not true. The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.) Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Statistics Block Table BIR field value) plus the offset (value in the Statistics Block Table Offset field multiplied by 8). All values of [n] between 0 and the value in the Number of Statistics Blocks field minus one inclusive must be tested.

Statistics Block Table Entry (n) Statistics Counter Table Offset [table] + 04h –DWORD

(for Endpoints and Switch Ports)

a. RsvdZ_3-0	RO-Zero
b. Statistics Counter Table Offset	RO

(This group of registers only exists if the Number of Statistics Blocks field is non-zero, and therefore this group of registers is not tested if this condition is not true. The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.) Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Statistics Block Table BIR field value) plus the offset (value in the Statistics Block Table Offset field multiplied by 8). All values of [n] between 0 and the value in the Number of Statistics Blocks field minus one inclusive must be tested.

Statistics Block Table Entry (n) Statistics Waiting Period [table] + 08h –DWORD

(for Endpoints and Switch Ports)

a. Statistics Waiting Period	RW
b. RsvdP_31-16	RO-Zero

(This group of registers only exists if the Number of Statistics Blocks field is non-zero, and therefore this group of registers is not tested if this condition is not true. The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Statistics Block Table BIR field value) plus the offset (value in the Statistics Block Table Offset field multiplied by 8). All values of [n] between 0 and the value in the Number of Statistics Blocks field minus one inclusive must be tested.

Statistics Block Table Entry (n) Statistics Counting Period [table] + 0Ch –DWORD

(for Endpoints and Switch Ports)

a. Statistics Counting Period	RW
b. RsvdP_31-24	RO-Zero

(This group of registers only exists if the Number of Statistics Blocks field is non-zero, and therefore this group of registers is not tested if this condition is not true. The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Statistics Block Table BIR field value) plus the offset (value in the Statistics Block Table Offset field multiplied by 8). All values of [n] between 0 and the value in the Number of Statistics Blocks field minus one inclusive must be tested.

Statistics Block Table Entry (x) Statistics Counter Table Entry (n) Statistics Capability and Control ([table, x] + ([n] * [size])) + 00h – DWORD

(for Endpoints and Switch Ports)

a. Port Number	
(for Switch Ports)	RO
(for Endpoints)	RO-Zero
b. Statistics Descriptor Index	RO
c. Counter Width	
d. RsvdP_22	RO-Zero
e. Counter Enable	RW or RO-Ones
f. Statistics Select	RW or RO

(This group of registers only exists if the Number of Statistics Blocks field is non-zero, and therefore this group of registers is not tested if this condition is not true. The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table, x] is the BAR contents (pointed to by the Statistics Block Table BIR field value) plus the offset (for Statistics Block Table Entry (x) the value in the Statistics Counter Table Offset field multiplied by 16). The value of [size] is for Statistics Block Table Entry (x) the value in the Statistics Counter Table Size field multiplied by 16. All values of [x] between 0 and the value in the Number of Statistics Blocks field minus one inclusive must be tested. All values of [n] between 0 and the value in the Statistics Counter Table Size field minus one inclusive must be tested.

Statistics Block Table Entry (x) Statistics Counter Table Entry (n) Statistics Filter Enable and Control ([table, x] + ([n] * [size])) + 04h – DWORD

(for Endpoints and Switch Ports)

a. Filter Enable and Control	RW

(This group of registers only exists if the Number of Statistics Blocks field is non-zero, and therefore this group of registers is not tested if this condition is not true. The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.) Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table, x] is the BAR contents (pointed to by the Statistics Block Table BIR field value) plus the offset (for Statistics Block Table Entry (x) the value in the Statistics Counter Table Offset field multiplied by 16). The value of [size] is for Statistics Block Table Entry (x) the value in the Statistics Counter Table Size field multiplied by 16. All values of [x] between 0 and the value in the Number of Statistics Blocks field minus one inclusive must be tested. All values of [n] between 0 and the value in the Statistics Counter Table Size field minus one inclusive must be tested.

Statistics Block Table Entry (x) Statistics Counter Table Entry (n) Statistics Counter Low ([table, x] + ([n] * [size])) + 08h – DWORD

(for Endpoints and Switch Ports)

a. (if Counter Width is greater than 31: bits 31 to 0) RO
b. (if Counter Width is less than 32: bits [Counter Width] to 0) RO
c. (if Counter Width is less than 31: bits 31 to ([Counter Width] + 1)) RO-Zero

(This group of registers only exists if the Number of Statistics Blocks field is non-zero, and therefore this group of registers is not tested if this condition is not true. The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.) Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table, x] is the BAR contents (pointed to by the Statistics Block Table BIR field value) plus the offset (for Statistics Block Table Entry (x) the value in the Statistics Counter Table Offset field multiplied by 16). The value of [size] is for Statistics Block Table Entry (x) the value in the Statistics Counter Table Size field multiplied by 16. All values of [x] between 0 and the value in the Number of Statistics Blocks field minus one inclusive must be tested. All values of [n] between 0 and the value in the Statistics Counter Table Size field minus one inclusive must be tested.

Statistics Block Table Entry (x) Statistics Counter Table Entry (n) Statistics Counter High ([table, x] + ([n] * [size])) + 0Ch – DWORD

(for Endpoints and Switch Ports)

a. (if Counter Width is 63: bits 31 to 0) RO
b. (if Counter Width is less than 63 and greater than 31: bits ([Counter Width]-32) to 0) RO
c. (if Counter Width is less than 63 and greater than 31: bits 31 to ([Counter Width]-32 + 1)) RO-Zero
d. (if Counter Width is less than 32: bits 31 to 0) RO-Zero

(This group of registers only exists if the Number of Statistics Blocks field is non-zero, and therefore this group of registers is not tested if this condition is not true. The MR Enable field must be written with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.) Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table, x] is the BAR contents (pointed to by the Statistics Block Table BIR field value) plus the offset (for Statistics Block Table Entry (x) the value in the Statistics Counter

Table Offset field multiplied by 16). The value of [size] is for Statistics Block Table Entry (x) the value in the Statistics Counter Table Size field multiplied by 16. All values of [x] between 0 and the value in the Number of Statistics Blocks field minus one inclusive must be tested. All values of [n] between 0 and the value in the Statistics Counter Table Size field minus one inclusive must be tested.

12. The following default value checks are performed:

MR-IOV Control Register Default Value (Offset 08h) — DWORD
(for Endpoints)

a. Function Table Interrupt Enable 0
b. Statistics Interrupt Enable 0
c. MR Uncorrectable Fatal TLP Error Interrupt Enable 0
d. MR Uncorrectable Global Key Error Interrupt Enable 0
e. MR Enable 0
f. VL Enable
 (if Is Main BF is 1 and MR Enable is written with 1) 01h
 (The MR Enable field must be written with the appropriate value before this field is tested.)

MR-IOV Control Register Default Value (Offset 08h) — DWORD
(for Switch Ports)

a. Port Interrupt Enable 0
b. VS Interrupt Enable 0
c. Statistics Interrupt Enable 0
d. MR Switch Number 0000h

MR-IOV Status Register Default Value (Offset 0Ch) — DWORD
(for Endpoints)

a. MSI Scheduled 0

MR-IOV Status Register Default Value (Offset 0Ch) — DWORD
(for Switch Ports)

a. Statistics Interrupt Status 0
b. MSI Scheduled 0

MR-IOV VH Counts Register Default Value (Offset 10h) — DWORD
(for Endpoints)

a. NumVH
 (if Is Main BF is 1 and MR Enable is written with 0) 00h
 (The MR Enable field must be written with the appropriate value before this field is tested.)

MR-IOV Watchdog Timer Control Default Value Register (Offset 14h) — DWORD
(for Switch Ports)

a. Watchdog Timer Interval 00h

MR-IOV VL Arbitration Capability and Status Default Value Register (Offset 20h) — DWORD
(for Endpoints)

a. VL Arbitration Status 0

MR-IOV VL Arbitration Control Default Value Register (Offset 24h) — DWORD
(for Endpoints)

a. VL Strict Priority Arbitration 00h

MR-IOV MR Error Control Default Value Register (Offset 2Eh) — WORD

(for Endpoints)

a. MR Uncorrectable Fatal TLP Error Mask 0
b. MR Uncorrectable Global Key Error Mask 0

Function Table Entry (n) Function Control 1 Default Value ([table] + ([n] * [size])) + 08h — DWORD

(for Endpoints)

a. VC Extended VC Count 000b
b. VC Low Priority Extended VC Count 000b
c. MFVC Extended VC Count 000b
d. MFVC Low Priority Extended VC Count 000b
e. Global Key 000h
f. Global Key Check Enable 0

(After returning the function to its default state test software must wait 1 second, then it must write the MR Enable field with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Function Table BIR field value) plus the offset (value in the Function Table Offset field multiplied by 8). The value of [size] is the value in the Function Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the MaxVH field inclusive must be tested.

Function Table Entry (n) Function Control 2 Default Value ([table] + [n] * size]) + 0Ch -– DWORD

(for Endpoints)

a. VC Config Changed Interrupt Enable 0
b. MFVC Config Changed Interrupt Enable 0
c. PF Reset Initiated Interrupt Enable 0
d. VF Migration Status Interrupt Enable 0
e. VF Enable Interrupt Enable 0
f. VF Migration Capable 0
g. InitialVFs
 (for PFs with VF Mapping Supported as 1) 0000h
 (for non-PFs) 0000h

(After returning the function to its default state test software must wait 1 second, then it must write the MR Enable field with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Function Table BIR field value) plus the offset (value in the Function Table Offset field multiplied by 8). The value of [size] is the value in the Function Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the MaxVH field inclusive must be tested.

Function Table Entry (n) Function Control 3 Default Value ([table] + ([n] * [size])) + 10h — DWORD

(for Endpoints)

a. TotalVFs 0000h

(After returning the function to its default state test software must wait 1 second, then it must write the MR Enable field with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Function Table BIR field value) plus the offset (value in the Function Table Offset field multiplied by 8). The value of [size] is the value in the Function Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the MaxVH field inclusive must be tested.

Function Table Entry (n) Function Status Default Value ([table] + ([n] * [size])) + 14h — DWORD

(for Endpoints)

a. VC Config Changed 0
b. MFVC Config Changed 0
c. PF Reset Initiated 0
d. VF Migration Status 0
e. VF Initialization Pending 0

(After returning the function to its default state test software must wait 1 second, then it must write the MR Enable field with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Function Table BIR field value) plus the offset (value in the Function Table Offset field multiplied by 8). The value of [size] is the value in the Function Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the MaxVH field inclusive must be tested.

Function Table Entry (n) VC to VL Map 1 Default Value ([table] + ([n] * [size])) + 18h — DWORD

(for Endpoints)

a. VC0 VL Map
(if Is Main BF is 1 and MaxVL is non-zero
and VC Capability Supported is 1) 000b
b. VC0 VL Map Enable
(if Is Main BF is 1 and MaxVL is non-zero
and VC Capability Supported is 1) 0 or 1
c. VC1 VL Map
(if Is Main BF is 1 and MaxVL is non-zero
and VC Capability Supported is 1
and Num VC Resources Hardware Present is 1 or greater) 001b
d. VC1 VL Map Enable
(if Is Main BF is 1 and MaxVL is non-zero
and VC Capability Supported is 1
and Num VC Resources Hardware Present is 1 or greater) 0
e. VC2 VL Map
(if Is Main BF is 1 and MaxVL is non-zero

and VC Capability Supported is 1
and Num VC Resources Hardware Present is 2 or greater) 010b

f. VC2 VL Map Enable
(if Is Main BF is 1 and MaxVL is non-zero
and VC Capability Supported is 1
and Num VC Resources Hardware Present is 2 or greater) 0

g. VC3 VL Map
(if Is Main BF is 1 and MaxVL is non-zero
and VC Capability Supported is 1
and Num VC Resources Hardware Present is 3 or greater) 011b

h. VC3 VL Map Enable
(if Is Main BF is 1 and MaxVL is non-zero
and VC Capability Supported is 1
and Num VC Resources Hardware Present is 3 or greater) 0

(After returning the function to its default state test software must wait 1 second, then it must write the MR Enable field with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Function Table BIR field value) plus the offset (value in the Function Table Offset field multiplied by 8). The value of [size] is the value in the Function Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the MaxVH field inclusive must be tested.

Function Table Entry (n) VC to VL Map 2 Default Value ([table] + ([n] * [size])) + 1Ch — DWORD

(for Endpoints)

a. VC4 VL Map
(if Is Main BF is 1 and MaxVL is non-zero
and VC Capability Supported is 1
and Num VC Resources Hardware Present is 4 or greater) 100b

b. VC4 VL Map Enable
(if Is Main BF is 1 and MaxVL is non-zero
and VC Capability Supported is 1
and Num VC Resources Hardware Present is 4 or greater) 0

c. VC5 VL Map
(if Is Main BF is 1 and MaxVL is non-zero
and VC Capability Supported is 1
and Num VC Resources Hardware Present is 5 or greater) 101b

d. VC5 VL Map Enable
(if Is Main BF is 1 and MaxVL is non-zero
and VC Capability Supported is 1
and Num VC Resources Hardware Present is 5 or greater) 0

e. VC6 VL Map
(if Is Main BF is 1 and MaxVL is non-zero
and VC Capability Supported is 1
and Num VC Resources Hardware Present is 6 or greater) 110b

f. VC6 VL Map Enable

(if Is Main BF is 1 and MaxVL is non-zero
and VC Capability Supported is 1
and Num VC Resources Hardware Present is 6 or greater) 0

g. VC7 VL Map
(if Is Main BF is 1 and MaxVL is non-zero
and VC Capability Supported is 1
and Num VC Resources Hardware Present is 7 or greater) 111b

h. VC7 VL Map Enable
(if Is Main BF is 1 and MaxVL is non-zero
and VC Capability Supported is 1
and Num VC Resources Hardware Present is 7 or greater) 0

(After returning the function to its default state test software must wait 1 second, then it must write the MR Enable field with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Function Table BIR field value) plus the offset (value in the Function Table Offset field multiplied by 8). The value of [size] is the value in the Function Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the MaxVH field inclusive must be tested.

Port Table Entry (n) Port Capability Default Value ([table] + ([n] * [size])) + 00h — DWORD

(for Switch Ports)

a. Link Direction Supported
(if VS is Authorized and Non-PCIe Port (Management Port) is 1) 001b

b. Port Direction Supported
(if VS is Authorized and Non-PCIe Port (Management Port) is 0) 01b, 10b, or 11b
(if VS is Authorized and Non-PCIe Port (Management Port) is 1) 10b

(After returning the function to its default state test software must wait 1 second, then it must write the MR Enable field with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested.

Port Table Entry (n) Port Control 1 Default Value ([table] + ([n] * [size])) + 04h — DWORD

(for Switch Ports)

a. Port DL_Up Interrupt Enable 0
b. Port DL_Down Interrupt Enable 0
c. Port PCIe Capability Interrupt Enable 0
d. Link Retrain Interrupt Enable 0
e. Beacon/WAKE# Interrupt Enable 0

f. MR Uncorrectable Fatal TLP Error Interrupt Enable 0
g. MR Uncorrectable Global Key Error Interrupt Enable 0
h. MR Correctable Global Key Error Interrupt Enable 0
i. Physical Hot-Plug Interrupt Enable 0

(After returning the function to its default state test software must wait 1 second, then it must write the MR Enable field with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested.

Port Table Entry (n) Port Control 2 Default Value ([table] + ([n] * [size])) + 08h –– DWORD

(for Switch Ports)
a. VL Enable
(if VS is Authorized and Non-PCIe Port (Management Port) is 0) 01h

(After returning the function to its default state test software must wait 1 second, then it must write the MR Enable field with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested.

Port Table Entry (n) VL Arbitration Capability and Status Default Value ([table] + ([n] * [size])) + 14h –– DWORD

(for Switch Ports)
a. VL Arbitration Status 0

(After returning the function to its default state test software must wait 1 second, then it must write the MR Enable field with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested.

Port Table Entry (n) VL Arbitration Control Default Value ([table] + ([n] * [size])) + 18h –– DWORD

(for Switch Ports)
a. Load VL Arbitration Table 0
b. VL Strict Priority Arbitration 00h

(After returning the function to its default state test software must wait 1 second, then it must write the MR Enable field with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested.

Port Table Entry (n) MR Error Control Default Value ([table] + ([n] * [size])) + 22h — WORD

(for Switch Ports)

a. MR Uncorrectable Fatal TLP Error Mask 0
b. MR Uncorrectable Global Key Error Mask 0
c. MR Correctable Global Key Error Mask 0

(After returning the function to its default state test software must wait 1 second, then it must write the MR Enable field with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested.

Port Table Entry (n) PCI Express Capabilities Default Value ([table] + ([n] * [size])) + [offset] + 02h — WORD

(for Switch Ports, if PCIe Offset is non-zero)

a. Capability Version 2h

(After returning the function to its default state test software must wait 1 second, then it must write the MR Enable field with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested.

Port Table Entry (n) Link Control Default Value ([table] + ([n] * [size])) + [offset] + 10h -– WORD

(for Switch Ports, if PCIe Offset is non-zero)

a. Link Disable 0
b. Common Clock Configuration 0
c. Extended Synch 0
d. Enable Clock Power Management 0

e. Hardware Autonomous Width Disable 0
f. Link Bandwidth Management Interrupt Enable 0
g. Link Autonomous Bandwidth Interrupt Enable 0
h. DRS Signaling Control
(For Base 3.x or later testing) 00b

(After returning the function to its default state test software must wait 1 second, then it must write the MR Enable field with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested.

Port Table Entry (n) Slot Control Default Value ([table] + ([n] * [size])) + [offset] + 18h -– WORD

(for Switch Ports, if PCIe Offset is non-zero)
a. Attention Button Pressed Enable 0
b. Power Fault Detected Enable 0
c. MRL Sensor Changed Enable 0
d. Presence Detect Changed Enable 0
e. Command Completed Interrupt Enable 0
f. Hot-Plug Interrupt Enable 0
g. Data Link Layer State Changed Enable 0

(After returning the function to its default state test software must wait 1 second, then it must write the MR Enable field with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested.

Port Table Entry (n) Slot Status Default Value ([table] + ([n] * [size])) + [offset] + 1Ah –– WORD

(for Switch Ports, if PCIe Offset is non-zero)
a. Attention Button Pressed 0
b. Power Fault Detected 0
c. MRL Sensor Changed 0
d. Command Completed 0

(After returning the function to its default state test software must wait 1 second, then it must write the MR Enable field with 0, then the NumVH field must be written with the value

returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested.

Port Table Entry (n) Device Control 2 Default Value ([table] + ([n] * [size])) + [offset] + 20h — WORD

(for Switch Ports, if PCIe Offset is non-zero)

a. AtomicOp Egress Blocking 0
b. LTR Mechanism Enable 0
c. Emergency Power Reduction Request
 (For Base 3.1 or later testing) 0
d. 10-Bit Tag Requester Enable
 (For Base 4.x or later testing) 0
e. OBFF Enable
 (For Base 2.x or later testing) 00b
f. End-End TLP Prefix Blocking 0

(After returning the function to its default state test software must wait 1 second, then it must write the MR Enable field with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested.

Port Table Entry (n) Link Control 2 Default Value ([table] + ([n] * [size])) + [offset] + 28h — WORD

(for Switch Ports, if PCIe Offset is non-zero)

a. Target Link Speed
 (For Base 2.x or later testing) [HLS]
 see Note below
 Note: The Highest supported Link Speed [HLS] is the value returned in the Port Table Entry Max Link Speed/Supported Link Speeds. [HLS] may also be 0000b if Max Link Speed/Supported Link Speeds returns 0001b (2.5 GT/s only).
 Note: This test must only write supported values as reported in the Port Table Entry Max Link Speed/Supported Link Speeds field.
b. Hardware Autonomous Speed Disable
 (For Base 2.x or later testing) 0
c. Transmit Margin

(For Base 2.x or later testing) 000b

d. Enter Modified Compliance
(For Base 2.x or later testing) 0

e. Compliance SOS
(For Base 2.x or later testing) 0

f. Compliance Preset/De-emphasis
(For Base 3.x or later testing) 0000b
Note: For Base 3.x or later, this field consists of bits 15-12 of this register.

g. Compliance De-emphasis
(For Base 2.x testing) 0
Note: For Base 2.x, this field consists of bit 12 of this register.

Note: The Enter Compliance field cannot be tested for default value, as setting it to 1 and then doing a Hot Reset (secondary bus reset) or DL_Down (link disable/enable), will cause the link to go to Compliance Pattern state and it may not return to L0 again.

(After returning the function to its default state test software must wait 1 second, then it must write the MR Enable field with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of [offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested.

Port Table Entry (n) Link Status 2 Default Value ([table] + ([n] * [size])) + [offset] + 2Ah — WORD

(for Switch Ports, if PCIe Offset is non-zero)

a. Link Equalization Request 8.0 GT/s
(For Base 3.x or later testing:
if Max Link Speed/Supported Link Speeds is 0010b or less) 0
Note: A function under test that supports 8.0 GT/s will participate in Link Equalization, so the default values of the 8.0 GT/s equalization status fields cannot be tested on an 8.0 GT/s capable device.
Note: The DRS Message Received field cannot be tested for default value, even though it will clear in a Downstream Port on DL_Down, because when the link retrains, new DRS Messages may be received.

(After returning the function to its default state test software must wait 1 second, then it must write the MR Enable field with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the Port Table BIR field value) plus the offset (value in the Port Table Offset field multiplied by 8). The value of [size] is the value in the Port Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num Port Table Entries field minus one inclusive must be tested. The value of

[offset] is the value in the PCIe Offset field multiplied by 4. If the PCIe Offset field is zero, then this register does not exist and is not tested.

VS Table Entry (n) VS Control Default Value ([table] + ([n] * [size])) + 04h — DWORD

(for Switch Ports)

a. VS Bridge Interrupt Enable	0
b. VS Global Key Value	000h
c. VS Global Key Entering Check Enable	0
d. VS Global Key Exiting Check Enable	0
e. VS Global Key Terminating Check Enable	0

(After returning the function to its default state test software must wait 1 second, then it must write the MR Enable field with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the VS Table BIR field value) plus the offset (value in the VS Table Offset field multiplied by 8). The value of [size] is the value in the VS Table Entry Size field multiplied by 4. All values of [n] between 0 and the value in the Num VS Table Entries field minus one inclusive must be tested.

VS Bridge Table Entry (n, x) VS Bridge Capability and Status Default Value ([table] + (([n] * [bsize]) + ([x] * [size]))) + 00h — DWORD

(for Switch Ports)

a. PME Turn Off State Changed	0
b. Power Controller State Changed	0
c. Power Indicator State Changed	0
d. Attention Indicator State Changed	0
e. VC Config Changed	0

(After returning the function to its default state test software must wait 1 second, then it must write the MR Enable field with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)

Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the VS Bridge Table BIR field value) plus the offset (value in the VS Bridge Table Offset field multiplied by 8). The value of [bsize] is the value in the Num VS Bridge Table Entries field multiplied by the VS Bridge Table Entry Size field multiplied by 4. The value of [size] is the value in the VS Bridge Table Entry Size field multiplied by 4. All values of [x] between 0 and the value in the Num VS Bridge Table Entries field minus one inclusive must be tested. All values of [n] between 0 and the value in the Num VS Table Entries field minus one inclusive must be tested.

VS Bridge Table Entry (n, x) VS Bridge Control 1 Default Value ([table] + (([n] * [bsize]) + ([x] * [size]))) + 04h — DWORD

(for Switch Ports)

a. VC Config Changed Interrupt Enable	0
b. PME Turn Off State Change Interrupt Enable	0

(After returning the function to its default state test software must wait 1 second, then it must write the MR Enable field with 0, then the NumVH field must be written with the value

returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the VS Bridge Table BIR field value) plus the offset (value in the VS Bridge Table Offset field multiplied by 8). The value of [bsize] is the value in the Num VS Bridge Table Entries field multiplied by the VS Bridge Table Entry Size field multiplied by 4. The value of [size] is the value in the VS Bridge Table Entry Size field multiplied by 4. All values of [x] between 0 and the value in the Num VS Bridge Table Entries field minus one inclusive must be tested. All values of [n] between 0 and the value in the Num VS Table Entries field minus one inclusive must be tested.

VS Bridge Table Entry (n, x) Virtual Hot-Plug Signals Interface 2 Default Value ([table] + (([n] * [bsize]) + ([x] * [size]))) + 10h — DWORD

(for Switch Ports)

a.	Virtual Slot Implemented	0
b.	Hot Plug Signals Interrupt Enable	0
c.	Virtual Discard Ingress Request	0
d.	Virtual Presence Detect State (if VS is Authorized and Hot-Plug Hardware Present is 1)	0
e.	Virtual Force Reset	0

(After returning the function to its default state test software must wait 1 second, then it must write the MR Enable field with 0, then the NumVH field must be written with the value returned by the MaxVH field, and then the MR Enable field must be written with 1 before this register is tested.)
Note: Testing this requires programming the designated Memory BAR and enabling Memory space. The value of [table] is the BAR contents (pointed to by the VS Bridge Table BIR field value) plus the offset (value in the VS Bridge Table Offset field multiplied by 8). The value of [bsize] is the value in the Num VS Bridge Table Entries field multiplied by the VS Bridge Table Entry Size field multiplied by 4. The value of [size] is the value in the VS Bridge Table Entry Size field multiplied by 4. All values of [x] between 0 and the value in the Num VS Bridge Table Entries field minus one inclusive must be tested. All values of [n] between 0 and the value in the Num VS Table Entries field minus one inclusive must be tested.

13. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
14. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one MR-IOV Extended Capability structure is present.
- ❑ A VF contains a MR-IOV Extended Capability structure.

- An RCRB contains a MR-IOV Extended Capability structure.
- The MR-IOV Extended Capability structure is present in any function other than the following: Endpoint; Legacy Endpoint; Root Complex Integrated Endpoint; Switch Upstream Port; Switch Downstream Port.
- The Capability Version field does not report 1h.
- The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- For an Endpoint, the implemented VL Enable fields are not RW when MR Enable is 1.
- For an Endpoint, the implemented VL Enable fields are not RO when MR Enable is 0.
- For an Endpoint, the NumVH field is not RW when MR Enable is 0.
- For an Endpoint, the NumVH field is not RO when MR Enable is 1.
- For an Endpoint, the Function Table Entry Size field is less than 16.
- For an Endpoint, the Function Table BIR field contains a reserved value.
- For an Endpoint, the Function Table BIR field value points to a non-memory BAR.
- For an Endpoint, the Function Table Offset field is less than 4.
- For an Endpoint, the LVF Table BIR field returns a reserved value.
- For an Endpoint, the LVF Table BIR field value points to a non-memory BAR.
- For an Endpoint that has the VL Arbitration Present field as 1, the VL Arbitration Capability field returns a reserved value.
- For an Endpoint that has the VL Arbitration Present field as 1 and the VL Arbitration Capability field supports Time-based WRR arbitration, the Reference Clock field returns a reserved value.
- For a Switch Port, the VS Authorization Bitmap Offset field returns a value less than 100h.
- For a Switch Port, the Port Table Entry Size field is less than 31.
- For a Switch Port, the Port Table BIR field contains a reserved value.
- For a Switch Port, the Port Table BIR field value points to a non-memory BAR.
- For a Switch Port, the Port Table Offset field is less than 4.
- For a Switch Port, the VS Table Entry Size field is less than 3.
- For a Switch Port, the VS Table BIR field contains a reserved value.
- For a Switch Port, the VS Table BIR field value points to a non-memory BAR.
- For a Switch Port, the VS Table Offset field is less than 4.
- For a Switch Port, the VS Bridge Table Entry Size field is less than 12.
- For a Switch Port, the VS Bridge Table BIR field contains a reserved value.
- For a Switch Port, the VS Bridge Table BIR field value points to a non-memory BAR.
- If VL Arbitration is supported, the VL Arbitration Table BIR field contains a reserved value.

- If VL Arbitration is supported, the VL Arbitration Table BIR field value points to a non-memory BAR.
- The Number of Statistics Blocks field returns a value greater than 31.
- Unimplemented bits in the Statistics Block Start/Busy register always return 0.
- Unimplemented bits in the Statistics Block Stop/Busy register always return 0.
- If the Number of Statistics Descriptors field is non-zero, the Statistics Descriptor Table BIR field contains a reserved value.
- If the Number of Statistics Descriptors field is non-zero, the Statistics Descriptor Table BIR field value points to a non-memory BAR.
- If the Number of Statistics Blocks field is non-zero, the Statistics Block Table BIR field contains a reserved value.
- If the Number of Statistics Blocks field is non-zero, the Statistics Block Table BIR field value points to a non-memory BAR.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

The test *warns* if:

- For a Switch Port, the Number of Statistics Blocks field returns 0.
- For a Switch Port, the Number of Statistics Descriptors field returns 0.

A.2 TD_1_65x M-PCIe Extended Capability Structure

The test verifies that if the function under test reports a M-PCIe Extended Capability structure, it is implemented as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*
- *M-PCIe ECN (to Base 3.0)*
- *ECN SR-IOV Table Updates (to SR-IOV 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 0020h (M-PCIe Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. For Base 2.x or earlier testing: if the Extended Capability ID of 0020h is found in an Extended Capability structure, the test terminates with a failure.
4. For Base 4.x or later testing: if the Extended Capability ID of 0020h is found in an Extended Capability structure, the test terminates with a failure.
5. For Base 3.x testing: if the Extended Capability ID of 0020h is found in an Extended Capability structure for a VF, the test terminates with a failure.
6. For Base 3.x testing: if the Extended Capability ID of 0020h is found in an Extended Capability structure for device type that is a Root Complex Integrated Endpoint or a Root Complex Event Collector, the test terminates with a failure.
7. For Base 3.x or later testing: if the Extended Capability ID of 0020h is found in an Extended Capability structure for a function associated with an upstream port and the function is not function 0, the test terminates with a failure.
8. For Base 3.x testing: if the Extended Capability ID of 0020h is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 0020h is not found in an Extended Capability structure, the test skips to step 15.
9. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
10. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
11. For Base 3.x testing: read a DWORD located at offset 04h (M-PCIe Capabilities register) and perform each of the following checks on the fields of the DWORD read:
 a. The Maximum TX LANE Width Capability field bit 0 must be 1. If not, this is recorded as a failure, but the test continues.
 b. The Maximum RX LANE Width Capability field bit 0 must be 1. If not, this is recorded as a failure, but the test continues.
 c. The Maximum TX LANE Width Capability field bit 7 must be 0. If not, this is recorded as a failure, but the test continues.
 d. The Maximum RX LANE Width Capability field bit 7 must be 0. If not, this is recorded as a failure, but the test continues.
12. For Base 3.x testing: read a DWORD located at offset 0Ch (M-PCIe Status register) and perform each of the following checks on the fields of the DWORD read:
 a. The M-PCIe Current Link Speed Status field must be 01b or 10b for 2.5 GT/s test cases. All other encodings are reserved and are recorded as a failure, but the test continues.
 b. The TX LANE Width Status field must be 00 0000b, 00 0001b, 00 0010b, 00 0100b, 00 1000b, 00 1100b, 01 0000b, or 10 0000b. All other encodings are reserved and are recorded as a failure, but the test continues.

c. The RX LANE Width Status field must be 00 0000b, 00 0001b, 00 0010b, 00 0100b, 00 1000b, 00 1100b, 01 0000b, or 10 0000b. All other encodings are reserved and are recorded as a failure, but the test continues.

13. The following register field characteristic checks are performed:

M-PCIe Extended Capability Header (Offset 00h) — DWORD

a. PCI Express Extended Capability ID	RO
b. Capability Version	RO
c. Next Capability Offset	RO

M-PCIe Capabilities Register (Offset 04h) — DWORD

a. M-PCIe Link Speed Capability	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
b. RsvdP_14-2	RO-Zero
c. Configuration.Software Supported	
(for Upstream Ports)	RO-Zero
(for Downstream Ports)	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
d. Maximum TX LANE Width Capability	
(for non-FLR testing)	HwInit
(for FLR testing)	RO
e. Maximum RX LANE Width Capability	
(for non-FLR testing)	HwInit
(for FLR testing)	RO

M-PCIe Control Register (Offset 08h) — DWORD

a. M-PCIe Target Link Speed Control	RW
b. RsvdP_31-2	RO-Zero

M-PCIe Status Register (Offset 0Ch) — DWORD

a. M-PCIe Current Link Speed Status	RO
b. RsvdZ_14-2	RO-Zero
c. M-PCIe Configuration.Software Status	
(for Downstream Ports)	RO
(for Upstream Ports)	RO-Zero
d. TX LANE Width Status	RO
e. RX LANE Width Status	RO

M-PCIe LANE Error Status Register (Offset 10h) — DWORD

a. (bits [Maximum Link Width-1] - 0)	RW1CS
b. (if [Maximum Link Width] is less than 32:	
bits 31 - [Maximum Link Width])	RO-Zero

M-PCIe Phy Control Address Register (Offset 14h) — DWORD

(for Downstream Ports)

a. Lower Addr[7:0]	RW
b. RsvdP_15-8	RO-Zero
c. Upper Addr[4:0]	RW

d. RsvdP_23-21 RO-Zero
e. Upper Addr[5] RW
f. Phy Location RW
g. RsvdP_29-28 RO-Zero
h. Read RO-Zero
Note: For Downstream Ports, writing the Read field causes the port to issue a RRAP read operation if supported (the Configuration.Software Supported field returns 1). The Read field always returns 0 when read.
i. Config RW
Note: For Downstream Ports, writing the Config field with 1, causes the port to leave L0 once it issues a RRAP operation if supported (the Configuration.Software Supported field returns 1). To avoid a link down, test software should only write the Config field with 0.

M-PCIe Phy Control Address Register (Offset 14h) — DWORD

(for Upstream Ports)
a. RsvdP_31-0 RO-Zero

M-PCIe Phy Control Data Register (Offset 18h) — DWORD

(for Downstream Ports)
a. Phy Register Data RW
b. RsvdP_28-8 RO-Zero
c. Phy Control Error RO
d. RRAP Abort (A) RO
e. Phy Control Pending RO
Note: For Downstream Ports, writing either the Read field with 1 or writing the Phy Register Data field, causes the port to issue a RRAP operation if supported (the Configuration.Software Supported field returns 1). During the RRAP operation the Phy Control Pending field will return 1, until the operation completes, so test software should allow up to 60 ms for the operation to complete and for the Phy Control Pending field to clear.

Note: For Downstream Ports, before testing this register, test software should clear the M-PCIe Phy Control Address register to all zeroes, to ensure that no RRAP operation is sent, if supported (the Configuration.Software Supported field returns 1), to the port on the other side of the link.

M-PCIe Phy Control Data Register (Offset 18h) — DWORD

(for Upstream Ports)
a. RsvdP_31-0 RO-Zero

14. The following default value checks are performed:

M-PCIe Control Register Default Value (Offset 08h) — DWORD

a. M-PCIe Target Link Speed Control 01b

M-PCIe Phy Control Address Register Default Value (Offset 14h) — DWORD

(for Downstream Ports)
a. Lower Addr[7:0] 00h
b. Upper Addr[4:0] 00000b
c. Upper Addr[5] 0
d. Phy Location 000b

M-PCIe Phy Control Data Register Default Value (Offset 18h) –– DWORD

(for Downstream Ports)

a. Phy Control Error 0
b. RRAP Abort (A) 0
c. Phy Control Pending 0

Note: For Downstream Ports, writing either the Read field with 1 or writing the Phy Register Data field, causes the port to issue a RRAP operation if supported (the Configuration.Software Supported field returns 1). During the RRAP operation the Phy Control Pending field will return 1, until the operation completes, so test software should allow up to 60 ms for the operation to complete and for the Phy Control Pending field to clear.

Note: For Downstream Ports, before testing this register, test software should clear the M-PCIe Phy Control Address register to all zeroes, to ensure that no RRAP operation is sent, if supported (the Configuration.Software Supported field returns 1), to the port on the other side of the link.

15. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
16. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ A M-PCIe Extended Capability structure is present (for Base 4.x or later testing only).
- ❑ More than one M-PCIe Extended Capability structure is present.
- ❑ A VF contains a M-PCIe Extended Capability structure.
- ❑ A Root Complex Integrated Endpoint or a Root Complex Event Collector contains a M-PCIe Extended Capability structure.
- ❑ For a multi-function device associated with an upstream port, the M-PCIe Extended Capability structure is present in a function other than function 0.
- ❑ The Capability Version field does not report 1h.
- ❑ The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b.
- ❑ The M-PCIe Extended Capability structure is present in a VF.
- ❑ The Maximum TX LANE Width Capability field has bit 0 return 0 (x1 not supported).
- ❑ The Maximum RX LANE Width Capability field has bit 0 return 0 (x1 not supported).
- ❑ The Maximum TX LANE Width Capability field has bit 7 return 1 (undefined value).
- ❑ The Maximum RX LANE Width Capability field has bit 7 return 1 (undefined value).

- The M-PCIe Current Link Speed Status field is not one of the defined values.
- The TX LANE Width Status field is not one of the defined values.
- The RX LANE Width Status field is not one of the defined values.
- Any of the register field characteristic tests fail.
- Any of the default value tests fail.

APPENDIX B. Obsolete Test Details

Tests that are no longer supported in this version of the test document are listed below for historical reference purposes. Existing test numbers should only be re-used in the event that the test is re-instated, or a new test is developed that overlaps the coverage of the obsolete test.

B.1 TD_1_33 Root Complex Integrated Endpoint

B.2 TD_1_35x Configuration Access Correlation Extended Capability Structure

Test TD_1_35x is now replaced by TD_1_35, as this Extended Capability structure is no longer supported by the current Base Specification. The test description below applies to a previous version of the Base Specification, when the capability structure was supported, and is included only for historical reasons.

The test verifies that if the function under test reports a PCI Express Configuration Access Correlation Extended Capability structure, it is implemented as defined in the relevant specifications. (A Configuration Access Correlation Extended Capability structure can only be implemented in a Base 1.1 device. Starting with Base 2.0, a Configuration Access Correlation Extended Capability structure is no longer supported and must not be implemented.)

Relevant Specifications

- *PCI Express Base Specification*
- *ECN Trusted Configuration Space (to Base 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Extended Capability ID field for each of the detected Extended Capability structures. Determine how many instances of the Extended Capability ID of 000Ch (Configuration Access Correlation Extended Capability) are found. If more than one is found, the test terminates with a failure.
3. If the Extended Capability ID of 000Ch is found in an Extended Capability structure for a VF, the test terminates with a failure.
4. If the Extended Capability ID of 000Ch is found in an Extended Capability structure for an RCRB, the test terminates with a failure.
5. For Base 2.x or later testing: if the Extended Capability ID of 000Ch is found in an Extended Capability structure, the test terminates with a failure.
6. For Base 1.x testing: if the Extended Capability ID of 000Ch is found in an Extended Capability structure, the following steps are performed on that Extended Capability structure. If the Extended Capability ID of 000Ch is not found in an Extended Capability structure, the test skips to step 10.
7. The Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
8. The Next Capability Offset field must be 000h or greater than 0FFh and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
9. The following register field characteristic checks are performed:

 Configuration Access Correlation Extended Capability Header (Offset 00) — DWORD

 a. Extended Capability ID — RO
 b. Capability Version — RO
 c. Next Capability Offset — RO

 Device Correlation Register (Offset 04) — DWORD

 (all bits) — RO

10. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
11. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one Configuration Access Correlation Extended Capability structure is present.
- ❑ A VF contains a Configuration Access Correlation Extended Capability structure.
- ❑ An RCRB contains a Configuration Access Correlation Extended Capability structure.

- The Configuration Access Correlation Extended Capability structure is present in any function (for Base 2.x or later testing only).
- The Capability Version field does not report 1h (for Base 1.x testing only).
- The Next Capability Offset field does not report 000h or a value greater than 0FFh or the lower two bits are not 00b (for Base 1.x testing only).
- Any of the register field characteristic tests fail (for Base 1.x testing only).

B.3 TD_1_36 Trusted Config Space Header

Test TD_1_36 is no longer supported, as this Trusted Capability structure is no longer supported by the current Base Specification. The test description below applies to a previous version of the Base Specification, when the capability structure was supported, and is included only for historical reasons.

The test verifies that if the function under test reports support for Trusted Configuration Space, it implements a Trusted Configuration Space Header as defined in the relevant specifications.

The test requires a platform that supports Trusted Configuration Cycles.

Relevant Specifications

- *ECN Trusted Configuration Space (to Base 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types implementing Trusted Configuration Space.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. For Base 1.x testing: read the 12 bits from location 004h (First Trusted Capability Offset field) in Trusted Configuration Space and perform the following checks and if any are not as stated, this is recorded as a failure, but the test continues:
 a. The lower two bits must be zero (00b).
 b. The value read, if non-zero, must be greater than 007h and less than FFDh.
3. The following register field characteristic checks are performed:

 Trusted Configuration Register 1 (Trusted Location 00h) — DWORD

 a. Trusted Class Code — RO
 b. RsvdP_31-24 — RO-Zero

 Trusted Configuration Register 2 (Trusted Location 04h) — DWORD

 a. First Trusted Capability Offset — RO

b. RsvdP_31-12 RO-Zero

4. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- The First Trusted Capability Offset field does not report 000h or a value greater than 007h or the lower two bits are not 00b (for Base 1.x testing only).
- Any of the register field characteristic tests fail.

B.4 TD_1_37 Configuration Access Correlation Trusted Capability Structure

Test TD_1_37 is no longer supported, as this Trusted Capability structure is no longer supported by the current Base Specification. The test description below applies to a previous version of the Base Specification, when the capability structure was supported, and is included only for historical reasons.

The test verifies that if the function under test reports a Configuration Access Correlation Trusted Capability structure, it is implemented as defined in the relevant specifications. (A Configuration Access Correlation Trusted Capability structure can only be implemented in a Base 1.1 device. Starting with Base 2.0, a Configuration Access Correlation Trusted Capability structure is no longer supported and must not be implemented.)

The test requires a platform that supports Trusted Configuration Cycles.

Relevant Specifications

- *ECN Trusted Configuration Space (to Base 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types implementing Trusted Configuration Space.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Trusted Capability ID field for each of the detected Trusted Capability structures. Determine how many instances of the Trusted Capability ID of 0001h (Configuration Access

Correlation Trusted Capability) are found. If more than one is found, the test terminates with a failure.

3. If the Trusted Capability ID of 0001h is found in an Trusted Capability structure for an RCRB, the test terminates with a failure.
4. For Base 2.x or later testing: if the Trusted Capability ID of 0001h is found in a Trusted Capability structure, the test terminates with a failure.
5. For Base 1.x testing: if the Trusted Capability ID of 0001h is found in a Trusted Capability structure, the following steps are performed on that Trusted Capability structure. If the Trusted Capability ID of 0001h is not found in a Trusted Capability structure, the test skips to step 9.
6. The Trusted Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
7. The Next Trusted Capability Offset field must be 000h or greater than 007h and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
8. The following register field characteristic checks are performed:

 Configuration Access Correlation Trusted Capability Header (Offset 00) –– DWORD

 a. Trusted Capability ID — RO
 b. Trusted Capability Version — RO
 c. Next Trusted Capability Offset — RO

 Device Correlation Register (Offset 04) –– DWORD

 (all bits) — RO

9. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
10. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ More than one Configuration Access Correlation Trusted Capability structure is present.
- ❑ An RCRB contains a Configuration Access Correlation Trusted Capability structure.
- ❑ The Configuration Access Correlation Trusted Capability structure is present in any function (for Base 2.x or later testing only).
- ❑ The Trusted Capability Version field does not report 1h (for Base 1.x testing only).
- ❑ The Next Trusted Capability Offset field does not report 000h or a value greater than 007h or the lower two bits are not 00b (for Base 1.x testing only).
- ❑ Any of the register field characteristic tests fail.

B.5 TD_1_38 Vendor-Specific Trusted Capability Structure

Test TD_1_38 is no longer supported, as this Trusted Capability structure is no longer supported by the current Base Specification. The test description below applies to a previous version of the Base Specification, when the capability structure was supported, and is included only for historical reasons.

The test verifies that if a function under test reports a Vendor-Specific Trusted Capability structure, it is implemented as defined in the relevant specifications.

The test requires a platform that supports Trusted Configuration Cycles.

Relevant Specifications

- *ECN Trusted Configuration Space (to Base 1.1)*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on all device/port types implementing Trusted Configuration Space.

This test is run on any RCRB associated with the function under test.

Starting Configuration

This test is run with functions starting in the D0-Uninitialized state following the standard initialization procedures in Section 2.1.1. Testing in additional Dx states may be optionally supported. ASPM states of the upstream and downstream ports are disabled for this test.

Overview of Test Steps:

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Examine the Trusted Capability ID field for each of the detected Trusted Capability structures. Determine how many instances of the Trusted Capability ID of 0002h (Vendor-Specific Trusted Capability) are found.
3. If the Trusted Capability ID of 0002h is found in a Trusted Capability structure for an RCRB, the test terminates with a failure.
4. If the Trusted Capability ID of 0002h is found in a Trusted Capability structure, the following steps are performed for each instance of that Trusted Capability structure. If the Trusted Capability ID of 0002h is not found in a Trusted Capability structure, the test skips to step 11.
5. The Trusted Capability Version field must be 1h. If not, this is recorded as a failure, but the test continues.
6. The Next Trusted Capability Offset field must be 000h or greater than 007h and the lower 2 bits of this field must be 00b. If not, this is recorded as a failure, but the test continues.
7. If the Next Trusted Capability Offset field is non-zero, it must return a value less than the starting offset of this Trusted Capability structure by at least 4 bytes or must be larger than the starting offset of this Trusted Capability structure plus the VSTC Length field value rounded to the next highest DWORD boundary. If not, this is recorded as a failure, but the test continues.
8. The value for the VSTC Length field must be at least 00Ch (12 bytes). If not, this is recorded as a failure, but the test continues.

9. If the VSTC Length field is greater than 00Ch, test software reads each byte starting at offset 0Ch, and continuing until the byte length given by the value in the VSTC Length field is reached. (This checks that Vendor-Specific registers can be read safely. No check on the returned data value is done.)
10. The following register field characteristic checks are performed:

Vendor-Specific Capability Trusted Capability Header (Offset 00h) — DWORD

a. PCI Express Trusted Capability ID	RO
b. Trusted Capability Version	RO
c. Next Trusted Capability Offset	RO

Vendor-Specific Header (Offset 04h) — DWORD

a. VSTC ID	RO
b. VSTC Rev	RO
c. VSTC Length	RO

VSTC Vendor ID (Offset 08h) — DWORD

a. VSTC Vendor ID	RO
b. RsvdP_31-16	RO-Zero

11. For functions under test that have a link, the test is run at each of the following link speeds (based on the Data Rate selection):
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.
12. If the device type is Root Port or Root Complex Integrated Endpoint, then the test is repeated using each RCRB associated with the function under test, or associated with an RCRB that is itself associated with the function under test. All offsets in the tests are now relative to the RCRB's base address and all cycles are now memory space accesses.

The test *fails* if:

- ❑ An RCRB contains a Vendor-Specific Trusted Capability structure.
- ❑ The Trusted Capability Version field does not report 1h.
- ❑ The Next Trusted Capability Offset field does not report 000h or a value greater than 007h or the lower two bits are not 00b.
- ❑ The Next Trusted Capability Offset field, when non-zero, is not at least 4 bytes less than the current Trusted Capability offset or it is less than the current Trusted Capability offset plus the VSTC Length field value rounded to the next highest DWORD boundary.
- ❑ The VSTC Length field is less than 12.
- ❑ Any of the register field characteristic tests fail.

B.6 TD_2_2x ASPM Link Training Stress

Test TD_2_2x is no longer supported as it requires the test program to modify the ASPM settings on the link, which is not required. This test has been replaced by TD_2_2) which performs a similar test without changing the ASPM settings.

The test verifies that the function under test correctly handles link retraining when it is initiated using the Link Control register of the downstream port connected to the function under test as required in the relevant specifications. The test also verifies that if the function under test implements ASPM, test software attempts to configure the function under test to a variety of different ASPM settings will not cause the device to operate abnormally, as defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on upstream ports of PCI Express Endpoints, Legacy Endpoints, Switch Upstream Ports, and PCI Express to PCI/PCI-X Bridges.

(Note: The downstream port connected to the function under test must be known to operate correctly in each of its supported ASPM modes.)

Starting Configuration

The device is placed into the desired starting state (D0-Uninitialized) following the standard initialization sequence in Section 2.1.1. Testing in additional Dx states may be optionally supported.

Overview of Test Steps

Test software performs the following steps:

1. Test software resets the bus connected to the function under test following the procedure describe in Section 2.1.1.1.
2. Read the Active State Power Management (ASPM) Support field from the Link Capabilities register of the function under test (this will also be referred to as the upstream port of the link). Record this value in Upstream ASPM [UASPMS].
3. Read the Active State Power Management (ASPM) Support field from the Link Capabilities register of the immediate upstream device's port (the downstream port of the link connected to the function under test), which will be referred to as the downstream port of the link. Record this value in Downstream ASPM [DASPMS].
4. Read the Retimer Presence Detect Supported field from the Link Capabilities 2 register of the immediate upstream device's port (the downstream port of the link connected to the function under test), and if the field's value is 0, then set [RTPSNT] to 0, but if the field's value is 1 then:
 a. Read the Retimer Presence Detected field from the Link Status 2 register of the immediate upstream device's port (the downstream port of the link connected to the function under test). Record this value in Retimer Present [RTPSNT].
5. If [RTPSNT] is 1, then skip to step 1.

6. Read the Two Retimers Presence Detect Supported field from the Link Capabilities 2 register of the immediate upstream device's port (the downstream port of the link connected to the function under test), and if the field's value is 0, then set [RTPSNT] to 0, but if the field's value is 1 then:
 a. Read the Two Retimers Presence Detected field from the Link Status 2 register of the immediate upstream device's port (the downstream port of the link connected to the function under test). Record this value in [RTPSNT].
7. Test software configures the function under test following the procedure described in Section 2.1.1. If the procedure fails to complete successfully, the test terminates with failure.
8. Test software modifies at least one non-sticky register field value from its default value. Any of the following fields can be used as long as they are implemented as RW in the target: Memory Space Enable (Command register); I/O Space Enable (Command register); Bus Master Enable (Command register); Interrupt Disable (Command register). If none of these fields are implemented as RW in the target, then other non-sticky RW fields can be used. If test software cannot find any non-sticky RW field in the target, then this step is skipped.
9. Test software reads the Negotiated Link Width field (Link Status register) for both the function under test and the downstream port of the link. Both values must be the same otherwise the test terminates with failure. If the same, the value is recorded in the Link Width Value [LWV].
10. Test software writes 1 to the Retrain Link field (Link Control register) on the downstream port of the link using a WORD access, while preserving all the other fields in this register.
11. Test software reads the Link Training field (Link Status register) on the downstream port of the link, until it returns 0.
12. Test software reads the Negotiated Link Width field (Link Status register) for both the function under test and the downstream port of the link. Both values must be the same otherwise the test terminates with failure. If the same, the value must be the same as [LWV] otherwise the test terminates with failure.
13. Test software reads back the register field programmed to a non-default value in step 2 and confirms it has not changed back to its default value. If it has changed back then the test terminates with failure.
14. Use the level of testing to determine the interpretation of the Active State Power Management (ASPM) Support field, and what values to write to the Active State Power Management (ASPM) Control field in the Link Control register of the upstream port of the link and the downstream port of the link. If the function under test is not a VF, but is part of a multi-function device (the Multi-Function Device field of Header Type register is 1), then the same ASPM setting value must be written to all non-VF functions in that multi-function device. If the function under test is a VF, then the ASPM setting value must be written to the PF associated with that VF, as well as any other non-VF functions in the multi-function device. If [RTPSNT] is 1, then all [UASPMS] and [DASPMS] values are modified so that bit 0 of the Active State Power Management (ASPM) Control field is forced to 0b (L0s disabled).
 a. For Base 1.x testing: use Table 1 in Section 2.1.2.21.1, together with [UASPMS] and [DASPMS] to determine which ASPM combinations are supported, perform step 1-7 for each of the supported ASPM combinations in Table 1 in Section 2.1.2.21.1. If the total number of iterations is less than 100, repeat this entire step again.

b. For Base 2.x or later testing: read the ASPM Optionality Compliance field from the Link Capabilities register in both the upstream port of the link and the downstream port of the link, and based on their reported values perform the following:
 i. If the ASPM Optionality Compliance field is 0 in both the upstream port of the link and the downstream port of the link, use Table 1 in Section 2.1.2.21.1, together with [UASPMS] and [DASPMS] to determine which ASPM combinations are supported, perform steps 1-7 for each of the supported ASPM combinations in Table 1 in Section 2.1.2.21.1. If the total number of iterations is less than 100, repeat this entire step again.
 ii. If the ASPM Optionality Compliance field is 1 in the upstream port of the link and the ASPM Optionality Compliance field is 0 in the downstream port of the link, use Table 2 in Section 2.1.2.21.2, together with [UASPMS] and [DASPMS] to determine which ASPM combinations are supported, perform steps 1-7 for each of the supported ASPM combinations in Table 2 in Section 2.1.2.21.2. If the total number of iterations is less than 100, repeat this entire step again.
 iii. If the ASPM Optionality Compliance field is 0 in the upstream port of the link and the ASPM Optionality Compliance field is 1 in the downstream port of the link, use Table 3 in Section 2.1.2.21.3, together with [UASPMS] and [DASPMS] to determine which ASPM combinations are supported, perform steps 1-7 for each of the supported ASPM combinations in Table 3 in Section 2.1.2.21.3. If the total number of iterations is less than 100, repeat this entire step again.
 iv. If the ASPM Optionality Compliance field is 1 in both the upstream port of the link and the downstream port of the link, use Table 4 in Section 2.1.2.21.4, together with [UASPMS] and [DASPMS] to determine which ASPM combinations are supported, perform steps 1-7 for each of the supported ASPM combinations in Table 4 in Section 2.1.2.21.4. If the total number of iterations is less than 100, repeat this entire step again.

15. For functions under test that have a link, the test is run at each of the following link speeds:
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- The reported Negotiated Link Width of the upstream component fails to match the Negotiated Link Width of the downstream component.
- Link retraining causes the Negotiated Link Width to change.
- Link retraining causes the upstream port to reset (restoring default values).

B.7 TD_2_5 Response to Different Bus and Device Numbers

Test TD_2_5 is no longer supported as it requires the test program to re-arrange the bus topology of the platform, which is an ability the test program cannot support.

The test verifies that the function under test views itself as the recipient of any Type 0 configuration requests it receives regardless of the Bus Number in the configuration request. Additionally, for a non-ARI device it is required to view itself as the recipient of any Type 0 configuration requests it receives regardless of the Device Number in the configuration request. This is defined in the relevant specifications.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on upstream ports of PCI Express Endpoints, Legacy Endpoints, Switch Upstream Ports, and PCI Express to PCI/PCI-X Bridges.

Starting Configuration

Function under test is completely uninitialized following a reset.

Overview of Test Steps

Test software performs the following steps:

1. Configure the function under test following the procedure described in Section 2.1.1.
2. Check if the function implements the ARI Extended Capability (Extended Capability ID of 000Eh). If it does, then record that this is an ARI device, otherwise record that this is a non-ARI device.
3. If this is a non-ARI device, configure the function under test following the procedure described in Section 2.1.1, but such that at various points in the configuration sequence different Device Numbers and Bus Numbers are used in the commands sent to the function under test. If the procedure fails to complete successfully, the test terminates with failure.
4. If this is an ARI device, configure the function under test following the procedure described in Section 2.1.1, but such that at various points in the configuration sequence different Bus Numbers are used in the commands sent to the function under test. If the procedure fails to complete successfully, the test terminates with failure.
5. Repeat the appropriate configuration sequence for the function under test (either step 1 or step 1) for 100 iterations.
6. For functions under test that have a link, the test is run at each of the following link speeds:
 a. 2.5 GT/s (for devices that are capable). See Section 2.1.2.12 for details.
 b. 5.0 GT/s (for devices that are capable). See Section 2.1.2.13 for details.
 c. 8.0 GT/s (for devices that are capable). See Section 2.1.2.14 for details.
 d. 16.0 GT/s (for devices that are capable). See Section 2.1.2.15 for details.

The test *fails* if:

- The function under test fails to respond to any part of the standard configuration sequence.

B.8 TD_3_3 Accurate Slot Reporting

Test TD_3_3 is no longer supported as it requires the system to reboot while the test is running, which the test cannot support. Also it requires the removal of all PCI Express cards, which cannot be done if some cards are required to support the test itself (such as a display card).

The test verifies that the system under test can accurately report physically available slots (those that are not used by system-integrated devices or are not exposed) versus silicon supported ports that are not connected to physical slots. The test prompts the user to unpopulate/populate the physical slots under test.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on downstream ports of Root Ports, Switch Downstream Ports, and PCI/PCI-X to PCI Express Bridges.

Starting Configuration

For a non-Root Port function under test, it is completely uninitialized following a reset, except that the bus number fields are initialized with valid numbers.

The immediate downstream device (the upstream port of the link connected to the function under test) is completely uninitialized following a reset.

Overview of Test Steps

Test software performs the following steps:

1. Prompt the user to power down (if necessary) and remove all PCI Express cards from physically exposed slots.
2. After a system reboot (if necessary) test software examines the PCI Express Capabilities register for each Downstream Port in the system.
3. For each Downstream Port that has a PCI Express Capabilities register that has the Slot Implemented field returns 1:
 a. Test software checks the Presence Detect State field (Slot Status register). If the Presence Detect State field returns 1 the test fails and is terminated.
 b. Test software checks the Presence Detect State field (Slot Status register). If the Presence Detect State field returns 0 record this as an implemented slot on a Downstream Port that does not have a card present.
4. Prompt the user to power down (if necessary) and populate with PCI Express cards each of the physically exposed slots.
5. After a system reboot (if necessary) test software does the following for each of the previously unpopulated Downstream Ports that has a PCI Express Capabilities register that has the Slot Implemented field set to 1(using the information recorded in step 3):
 a. Test software checks the Presence Detect State field (Slot Status register). If the Presence Detect State field returns 0 the test fails and is terminated.

The test *fails* if:

- A populated physical slot cannot be unpopulated by the user (as indicated by the Presence Detect State field of the Slot Status register returning 1).
- An unpopulated physical slot cannot be populated by the user (as indicated by the Presence Detect State field of the Slot Status register returning 0).

B.9 TD_3_4 Basic Hot-Plug Insertion

Test TD_3_4 is no longer supported as it requires the removal of all PCI Express cards, which cannot be done if some cards are required to support the test itself (such as a display card).

The test verifies that the system under test can properly handle hot-plug situations of hot insert and that each downstream port connected to a physical slot accurately reports its hot-plug state in its Slot Capabilities, Slot Control, and Slot Status registers. The test prompts the user to unpopulate/populate the hot-plug slots under test. If an attention button is implemented, the test also prompts the user to press it.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on downstream ports of Root Ports, Switch Downstream Ports, and PCI/PCI-X to PCI Express Bridges.

Starting Configuration

For a non-Root Port function under test, it is completely uninitialized following a reset, except that the bus number fields are initialized with valid numbers.

The immediate downstream device (the upstream port of the link connected to the function under test) is completely uninitialized following a reset.

Overview of Test Steps

Test software performs the following steps:

1. Prompt the user to power down (if necessary) and remove all PCI Express cards from physically exposed slots (hot-plug slots and optionally non-hot-plug slots).
2. After a system reboot (if necessary) test software examines the PCI Express Capabilities register for each Downstream Port in the system.
3. For each Downstream Port that has a PCI Express Capabilities register that has both the Slot Implemented field (PCI Express Capabilities register) returns 1 and the Hot-Plug Capable field (Slot Capabilities register) returns 1:
 a. Test software identifies for the user, the slot currently under test by doing the following:
 i A message is presented displaying to the user, the value read from the Physical Slot Number field (Slot Capabilities register).
 ii If the Attention Indicator Present field (Slot Capabilities register) returns 1, test software writes the Attention Indicator Control field (Slot Control register) with 10b (Blink). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status).
 b. Test software blinks the power indicator for the slot currently under test by doing the following:
 i If the Power Indicator Present field (Slot Capabilities register) returns 1, test software writes the Power Indicator Control field (Slot Control register) with 10b (Blink). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this

does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status). Test software reads the Power Indicator Control field (Slot Control register) to verify that it returns 10b (Blink) and if it does not the test fails for this slot, and the remaining steps are skipped.

c. Test software powers down the slot currently under test by doing the following:
 i If the Power Controller Present field (Slot Capabilities register) returns 1, test software writes the Power Controller Control field (Slot Control register) with 1 (Power Off). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status). Test software reads the Power Controller Control field (Slot Control register) to verify that it returns 1 (slot power is off) and if it does not the test fails for this slot, and the remaining steps are skipped.
 ii Test software waits for 1 second to allow power to settle in the off state.
d. Test software turns off the power indicator for the slot currently under test by doing the following:
 i If the Power Indicator Present field (Slot Capabilities register) returns 1, test software writes the Power Indicator Control field (Slot Control register) with 11b (Off). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status). Test software reads the Power Indicator Control field (Slot Control register) to verify that it returns 11b (Off) and if it does not the test fails for this slot, and the remaining steps are skipped.
e. Test software opens the slot currently under test by doing the following:
 i If the Electromechanical Interlock Present field (Slot Capabilities register) returns 1, test software reads the Electromechanical Interlock Status field (Slot Status register) and only if it returns 1 (engaged) does it writes the Electromechanical Interlock Control field (Slot Control register) with 1 (toggle interlock). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status).
f. Test software checks the attention button for the slot currently under test by doing the following:
 i If the Attention Button Present field (Slot Capabilities register) returns 1, test software writes the Attention Button Pressed field (Slot Control register) with 1 to clear the

previous status. Test software then prompts the user to press the attention button for the slot under test. Test software then checks that the Attention Button Pressed field (Slot Status register) returns 1 and if it does not the test fails for this slot and the test continues with the next step. Test software writes the Attention Button Pressed field (Slot Status register) with 1 (to clear the status).

g. If the Data Link Layer Link Active Reporting Capable field (Link Capabilities register) returns 1, test software writes the Data Link Layer State Changed field (Slot Status register) with 1 (to clear the status).
h. Test software writes the Presence Detect Changed field (Slot Status register) with 1 (to clear the status).
i. Test software prompts the user to insert a hot-pluggable PCI Express card into the slot under test, but to not yet close any mechanical retention mechanism (if present).
j. Test software locks the slot currently under test by doing the following:
 i If the MRL Sensor Present field (Slot Capabilities register) returns 1, test software writes the MRL Sensor Changed field (Slot Status register) with 1 (to clear the status).
 ii If the MRL Sensor Present field (Slot Capabilities register) returns 1, test software presents a message to the user, asking that they move the mechanical release latch for the slot under test to the closed position.
 iii If the MRL Sensor Present field (Slot Capabilities register) returns 1, test software checks that the MRL Sensor Changed field (Slot Status register) returns 1, and if it does not the test fails for this slot and the test continues with the next step. Test software writes the MRL Sensor Changed field (Slot Status register) with 1 (to clear the status).
 iv If the MRL Sensor Present field (Slot Capabilities register) returns 1, test software checks that the MRL Sensor State field (Slot Status register) returns 0 (Closed), and if it does not the test fails for this slot the remaining steps are skipped.
k. Test software closes the slot currently under test by doing the following:
 i If the Electromechanical Interlock Present field (Slot Capabilities register) returns 1, test software reads the Electromechanical Interlock Status field (Slot Status register) and only if it returns 0 (disengaged) does it writes the Electromechanical Interlock Control field (Slot Control register) with 1 (toggle interlock). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status). Test software reads the Electromechanical Interlock Status field (Slot Status register) to verify that it returns 1 (engaged) and if it does not the test fails for this slot, and the remaining steps are skipped.
l. Test software powers up the slot currently under test by doing the following:
 i If the Power Controller Present field (Slot Capabilities register) returns 1, test software writes the Power Fault Detected field (Slot Status register) with 1 (to clear the status).
 ii If the Power Controller Present field (Slot Capabilities register) returns 1, test software writes the Power Controller Control field (Slot Control register) with 0 (Power On). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, then the test fails for this slot, and

the remaining steps are skipped. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status). Test software reads the Power Controller Control field (Slot Control register) to verify that it returns 0 (slot power is on) and if it does not the test fails for this slot, and the remaining steps are skipped.

m. Test software check for power faults in the slot currently under test by doing the following:
 i If the Power Controller Present field (Slot Capabilities register) returns 1, test software reads the Power Fault Detected field (Slot Status register) to verify that it returns 0 (no faults) and if it does not the test fails for this slot, steps c-d are repeated (to power down the slot and turn off the power indicator), and the remaining steps are skipped.
n. Test software turns on the power indicator for the slot currently under test by doing the following:
 i If the Power Indicator Present field (Slot Capabilities register) returns 1, test software writes the Power Indicator Control field (Slot Control register) with 01b (On). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status). Test software reads the Power Indicator Control field (Slot Control register) to verify that it returns 01b (On) and if it does not the test fails for this slot, and the remaining steps are skipped.
o. Test software checks that the Presence Detect Changed field (Slot Status register) returns 1 (presence detect state has changed) and if it does not the test fails for this slot and the remaining steps are skipped. Test software writes the Presence Detect Changed field (Slot Status register) with 1 (to clear the status).
p. Test software checks that the Presence Detect State field (Slot Status register) returns 1 (card present) and if it does not the test fails for this slot and the remaining steps are skipped.
q. Test software waits for 1 second to allow Data Link Layer to become active. Note: Test software is required to allow 1 second from the hot-plug event until it determines the device does not function.
r. Test software reads that the Link Disable field (Link Control register) and only if it returns 1 (disabled), it writes the Link Disable field (Link Control register) with a 0 (to re-enable the link) using a WORD access, while preserving all the other fields in this register.
s. Test software then repeatedly reads the Link Training field (Link Status register), until it returns 0. If it does not return 0 within 1 second the test fails for this slot and the remaining steps are skipped.
t. If the Data Link Layer Link Active Reporting Capable field (Link Capabilities register) returns 1, test software checks that the Data Link Layer State Changed field (Slot Status register) returns 1 (data link layer link active state has changed) and if it does not the test fails for this slot and the remaining steps are skipped. Test software writes the Data Link Layer State Changed field (Slot Status register) with 1 (to clear the status).
u. Test software configures at least one of the functions on the PCI Express card added to the slot under testing using the standard method described in Section 2.1.1.2. If it does not configure properly the test fails for this slot and the remaining steps are skipped.
v. Test software clears the attention indicator for the slot currently under test by doing the following:

i If the Attention Indicator Present field (Slot Capabilities register) returns 1, test software writes the Attention Indicator Control field (Slot Control register) with 11b (Off). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status).

4. The test is repeated with all PCI Express cards that are supported by the slot under test's form factor (e.g., different add-in card connector widths, different add-in card link speeds, different add-in card power consumptions, etc.).

The test *fails* if:

- The No Command Completed Support field is 0, but the Command Completed field status does not return 1 within the time allowance after initiating a command.
- The Power Controller Control field does not properly reflect the last command (power on/power off) written to it, for a slot that indicates it implements a power controller.
- Writing a 1 to the Power Controller Control field does not turn power off to a slot that indicates it implements a power controller.
- The Power Indicator Control field does not properly reflect the last command (power indicator on/power indicator off) written to it, for a slot that indicates it implements a power indicator.
- Pressing the attention button does not cause the Attention Button Pressed field to be cleared, for a slot that indicates it implements an attention button.
- Closing the mechanical retention latch on a slot does not cause the MRL Sensor Changed field to be set, for a slot that indicates it implements a MRL sensor.
- Closing the mechanical retention latch on a slot does not cause the MRL Sensor State field to be cleared, for a slot that indicates it implements a MRL sensor.
- The Electromechanical Interlock field does not indicate the engaged state when the interlock is toggled to the engaged setting, for a slot that indicates it implements an electromechanical interlock.
- The hot-plug command to power on the slot does not complete properly, for a slot that indicates it implements a power controller.
- Writing a 0 to the Power Controller Control field does not turn power on to a slot that indicates it implements a power controller.
- The Power Fault Detected field indicates a power fault following a power on of the slot, for a slot that indicates it implements a power controller.
- Powering on a slot with a card installed does not cause the Presence Detect Changed field to be set.
- Powering on a slot with a card installed does not cause the Presence Detect State field to be set.
- Powering on a slot with a card installed does not result in successful link training.

- Powering on a slot with a card installed does not cause the Data Link Layer State Changed field to be set, for a slot that indicates it implements data link layer active reporting capability.
- A card that has been hot inserted cannot be successfully configured.

B.10 TD_3_5 Basic Hot-Plug Removal

Test TD_3_5 is no longer supported as it requires the removal of all PCI Express cards, which cannot be done if some cards are required to support the test itself (such as a display card).

The test verifies that the system under test can properly handle hot-plug situations of hot remove and that each downstream port connected to a physical slot accurately reports its hot-plug state in its Slot Capabilities, Slot Control, and Slot Status registers. The test prompts the user to populate/unpopulate the hot-plug slots under test. If an attention button is implemented, the test also prompts the user to press it.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on downstream ports of Root Ports, Switch Downstream Ports, and PCI/PCI-X to PCI Express Bridges.

Starting Configuration

For a non-Root Port function under test, it is completely uninitialized following a reset, except that the bus number fields are initialized with valid numbers.

The immediate downstream device (the upstream port of the link connected to the function under test) is completely uninitialized following a reset.

Overview of Test Steps

Test software performs the following steps:

1. Prompt the user to power down (if necessary) and install PCI Express cards in all physically exposed slots (hot-plug slots and optionally non-hot-plug slots).
2. After a system reboot (if necessary) test software examines the PCI Express Capabilities register for each Downstream Port in the system.
3. For each Downstream Port that has a PCI Express Capabilities register that has both the Slot Implemented field (PCI Express Capabilities register) returns 1 and the Hot-Plug Capable field (Slot Capabilities register) returns 1:
 a. Test software identifies for the user, the slot currently under test by doing the following:
 i A message is presented displaying to the user, the value read from the Physical Slot Number field (Slot Capabilities register).
 ii If the Attention Indicator Present field (Slot Capabilities register) returns 1, test software writes the Attention Indicator Control field (Slot Control register) with 10b (Blink). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is

repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status).

b. Test software checks the attention button for the slot currently under test by doing the following:
 i If the Attention Button Present field (Slot Capabilities register) returns 1, test software writes the Attention Button Pressed field (Slot Control register) with 1 to clear the previous status. Test software then prompts the user to press the attention button for the slot under test. Test software then checks that the Attention Button Pressed field (Slot Status register) returns 1 and if it does not the test fails for this slot and the test continues with the next step. Test software writes the Attention Button Pressed field (Slot Status register) with 1 (to clear the status).
c. Test software writes the Link Disable field (Link Control register) with a 1 (to disable the link) using a WORD access, while preserving all the other fields in this register.
d. Test software blinks the power indicator for the slot currently under test by doing the following:
 i If the Power Indicator Present field (Slot Capabilities register) returns 1, test software writes the Power Indicator Control field (Slot Control register) with 10b (Blink). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status). Test software reads the Power Indicator Control field (Slot Control register) to verify that it returns 10b (Blink) and if it does not the test fails for this slot, and the remaining steps are skipped.
e. If the Data Link Layer Link Active Reporting Capable field (Link Capabilities register) returns 1, test software writes the Data Link Layer State Changed field (Slot Status register) with 1 (to clear the status).
f. Test software writes the Presence Detect Changed field (Slot Status register) with 1 (to clear the status).
g. Test software powers down the slot currently under test by doing the following:
 i If the Power Controller Present field (Slot Capabilities register) returns 1, test software writes the Power Fault Detected field (Slot Status register) with 1 (to clear the status).
 ii If the Power Controller Present field (Slot Capabilities register) returns 1, test software writes the Power Controller Control field (Slot Control register) with 1 (Power Off). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status). Test software reads the Power Controller Control field (Slot Control register) to verify that it returns 1 (slot power is off) and if it does not the test fails for this slot, and the remaining steps are skipped.
 iii Test software waits for 1 second to allow power to settle in the off state.

h. Test software turns off the power indicator for the slot currently under test by doing the following:
 i If the Power Indicator Present field (Slot Capabilities register) returns 1, test software writes the Power Indicator Control field (Slot Control register) with 11b (Off). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status). Test software reads the Power Indicator Control field (Slot Control register) to verify that it returns 11b (Off) and if it does not the test fails for this slot, and the remaining steps are skipped.

i. Test software opens the slot currently under test by doing the following:
 i If the Electromechanical Interlock Present field (Slot Capabilities register) returns 1, test software reads the Electromechanical Interlock Status field (Slot Status register) and only if it returns 1 (engaged) does it writes the Electromechanical Interlock Control field (Slot Control register) with 1 (toggle interlock). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status). Test software reads the Electromechanical Interlock Status field (Slot Status register) to verify that it returns 0 (disengaged) and if it does not the test fails for this slot, and the remaining steps are skipped.

j. Test software unlocks the slot currently under test by doing the following:
 i If the MRL Sensor Present field (Slot Capabilities register) returns 1, test software writes the MRL Sensor Changed field (Slot Status register) with 1 (to clear the status).
 ii If the MRL Sensor Present field (Slot Capabilities register) returns 1, test software presents a message to the user, asking that they move the mechanical release latch for the slot under test to the open position.
 iii If the MRL Sensor Present field (Slot Capabilities register) returns 1, test software checks that the MRL Sensor Changed field (Slot Status register) returns 1, and if it does not the test fails for this slot and the test continues with the next step. Test software writes the MRL Sensor Changed field (Slot Status register) with 1 (to clear the status).
 iv If the MRL Sensor Present field (Slot Capabilities register) returns 1, test software checks that the MRL Sensor State field (Slot Status register) returns 1 (Open), and if it does not the test fails for this slot and the test continues with the next step.

k. Test software prompts the user to remove the hot-pluggable PCI Express card from the slot under test.

l. Test software check for power faults in the slot currently under test by doing the following:
 i If the Power Controller Present field (Slot Capabilities register) returns 1, test software reads the Power Fault Detected field (Slot Status register) to verify that it returns 0 (no faults) and if it does not the test fails for this slot, steps g-h are repeated (to power down the slot and turn off the power indicator), and the remaining steps are skipped.

m. Test software checks that the Presence Detect Changed field (Slot Status register) returns 1 (presence detect state has changed) and if it does not the test fails for this slot and the remaining steps are skipped. Test software writes the Presence Detect Changed field (Slot Status register) with 1 (to clear the status).
n. Test software checks that the Presence Detect State field (Slot Status register) returns 0 (slot empty) and if it does not the test fails for this slot and the remaining steps are skipped.
o. If the Data Link Layer Link Active Reporting Capable field (Link Capabilities register) returns 1, test software checks that the Data Link Layer State Changed field (Slot Status register) returns 1 (data link layer link active state has changed) and if it does not the test fails for this slot and the remaining steps are skipped. Test software writes the Data Link Layer State Changed field (Slot Status register) with 1 (to clear the status).
p. Test software clears the attention indicator for the slot currently under test by doing the following:
 i If the Attention Indicator Present field (Slot Capabilities register) returns 1, test software writes the Attention Indicator Control field (Slot Control register) with 11b (Off). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status).

4. The test is repeated with all PCI Express cards that are supported by the slot under test's form factor (e.g., different add-in card connector widths, different add-in card link speeds, different add-in card power consumptions, etc.).

The test *fails* if:

- The No Command Completed Support field is 0, but the Command Completed field status does not return 1 within the time allowance after initiating a command.
- Pressing the attention button does not cause the Attention Button Pressed field to be cleared, for a slot that indicates it implements an attention button.
- The Power Controller Control field does not properly reflect the last command (power on/power off) written to it, for a slot that indicates it implements a power controller.
- The hot-plug command to power off the slot does not complete properly, for a slot that indicates it implements a power controller.
- Writing a 1 to the Power Controller Control field does not turn power off to a slot that indicates it implements a power controller.
- The Power Indicator Control field does not properly reflect the last command (power indicator on/power indicator off) written to it, for a slot that indicates it implements a power indicator.
- The Electromechanical Interlock field does not indicate the engaged state when the interlock is toggled to the engaged setting, for a slot that indicates it implements an electromechanical interlock.
- Opening the mechanical retention latch on a slot does not cause the MRL Sensor Changed field to be set, for a slot that indicates it implements a MRL sensor.

- Opening the mechanical retention latch on a slot does not cause the MRL Sensor State field to be set, for a slot that indicates it implements a MRL sensor.
- Removing a card from a slot does not cause the Presence Detect Changed field to be set.
- Removing a card from a slot does not cause the Presence Detect State field to be cleared.
- Removing a card from a slot does not cause the Data Link Layer State Changed field to be set, for a slot that indicates it implements data link layer active reporting capability.

B.11 TD_3_6 Basic Hot-Plug Surprise Removal

Test TD_3_6 is no longer supported as it requires the removal of all PCI Express cards, which cannot be done if some cards are required to support the test itself (such as a display card).

The test verifies that the system under test can properly handle hot-plug situations of surprise hot remove and that each downstream port connected to a physical slot accurately reports its hot-plug state in its Slot Capabilities, Slot Control, and Slot Status registers. The test prompts the user to populate/unpopulate the hot-plug slots under test.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on downstream ports of Root Ports, Switch Downstream Ports, and PCI/PCI-X to PCI Express Bridges.

Starting Configuration

For a non-Root Port function under test, it is completely uninitialized following a reset, except that the bus number fields are initialized with valid numbers.

The immediate downstream device (the upstream port of the link connected to the function under test) is completely uninitialized following a reset.

Overview of Test Steps

Test software performs the following steps:

1. Prompt the user to power down (if necessary) and install PCI Express cards in all physically exposed slots (hot-plug slots and optionally non-hot-plug slots).
2. After a system reboot (if necessary) test software examines the PCI Express Capabilities register for each Downstream Port in the system.
3. For each Downstream Port that has a PCI Express Capabilities register that has all three of the Slot Implemented field (PCI Express Capabilities register) returns 1, the Hot-Plug Capable field (Slot Capabilities register) returns 1, and the Hot-Plug Surprise field (Slot Capabilities register) returns 1:
 a. Test software identifies for the user, the slot currently under test by doing the following:
 i A message is presented displaying to the user, the value read from the Physical Slot Number field (Slot Capabilities register).

ii If the Attention Indicator Present field (Slot Capabilities register) returns 1, test software writes the Attention Indicator Control field (Slot Control register) with 10b (Blink). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status).

b. If the Attention Button Present field (Slot Capabilities register) returns 1, test software writes the Attention Button Pressed field (Slot Control register) with 1 (to clear the status).
c. If the Data Link Layer Link Active Reporting Capable field (Link Capabilities register) returns 1, test software writes the Data Link Layer State Changed field (Slot Status register) with 1 (to clear the status).
d. Test software writes the Presence Detect Changed field (Slot Status register) with 1 (to clear the status).
e. Test software checks the attention button for the slot currently under test by doing the following:
 i If the Attention Button Present field (Slot Capabilities register) returns 1, test software checks that the Attention Button Pressed field (Slot Status register) returns 0 and if it does not the test fails for this slot and the test continues with the next step.
f. Test software prompts the user to remove the hot-pluggable PCI Express card from the slot under test.
g. Test software checks that the Presence Detect Changed field (Slot Status register) returns 1 (presence detect state has changed) and if it does not the test fails for this slot and the remaining steps are skipped. Test software writes the Presence Detect Changed field (Slot Status register) with 1 (to clear the status).
h. Test software checks that the Presence Detect State field (Slot Status register) returns 0 (slot empty) and if it does not the test fails for this slot and the remaining steps are skipped.
i. If the Data Link Layer Link Active Reporting Capable field (Link Capabilities register) returns 1, test software checks that the Data Link Layer State Changed field (Slot Status register) returns 1 (data link layer link active state has changed) and if it does not the test fails for this slot and the remaining steps are skipped. Test software writes the Data Link Layer State Changed field (Slot Status register) with 1 (to clear the status).
j. Test software clears the attention indicator for the slot currently under test by doing the following:
 i If the Attention Indicator Present field (Slot Capabilities register) returns 1, test software writes the Attention Indicator Control field (Slot Control register) with 11b (Off). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status).

4. The test is repeated with all PCI Express cards that are supported by the slot under test's form factor (e.g., different add-in card connector widths, different add-in card link speeds, different add-in card power consumptions, etc.).

The test *fails* if:

- The Attention Button Pressed field does not stay cleared, for a slot that indicates it implements an attention button.
- Surprise removing a card from a slot does not cause the Presence Detect Changed field to be set.
- Surprise removing a card from a slot does not cause the Presence Detect State field to be cleared.
- Surprise removing a card from a slot does not cause the Data Link Layer State Changed field to be set, for a slot that indicates it implements data link layer active reporting capability.

B.12 TD_3_7 Attention Button MRL Indicator Control

Test TD_3_7 is no longer supported as it requires the removal of all PCI Express cards, which cannot be done if some cards are required to support the test itself (such as a display card).

The test verifies that the system under test can properly reports attention buttons, MRL sensors, power indicators, and attention indicators where they are implemented, using its Slot Capabilities registers. In manual mode, the test prompts the user to visually check for the presence of attention buttons, MRL sensors, power indicators, and attention indicators. In automatic mode, the test shall accept a parameter that identifies the presence of attention buttons, MRL sensors, power indicators, and attention indicators. If an attention button is implemented, the test also prompts the user to press it. If a mechanical retention latch is present, the test also prompts the user to toggle it.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on downstream ports of Root Ports, Switch Downstream Ports, and PCI/PCI-X to PCI Express Bridges.

Starting Configuration

For a non-Root Port function under test, it is completely uninitialized following a reset, except that the bus number fields are initialized with valid numbers.

The immediate downstream device (the upstream port of the link connected to the function under test) is completely uninitialized following a reset.

Overview of Test Steps

Test software performs the following steps:

1. Test software checks each Downstream Port and records all those that have a PCI Express Capabilities register that has the Slot Implemented field (PCI Express Capabilities register) return 1.

2. Test software writes the Slot Control register, of each Downstream Port that has a PCI Express Capabilities register that has the Slot Implemented field (PCI Express Capabilities register) return 1, with a value that sets to 00b (Reserved) the following fields: Attention Indicator Control; Power Indicator Control.
3. Test software writes the Slot Status register, of each Downstream Port that has a PCI Express Capabilities register that has the Slot Implemented field (PCI Express Capabilities register) return 1, with a value that sets to 1 (to clear the status) the following fields: Attention Button Pressed; MRL Sensor Changed.
4. For each Downstream Port that has a PCI Express Capabilities register that has the Slot Implemented field (PCI Express Capabilities register) return 1:
 a. Test software identifies for the user, the slot currently under test by doing the following:
 i A message is presented displaying to the user, the value read from the Physical Slot Number field (Slot Capabilities register).
 ii If the Attention Indicator Present field (Slot Capabilities register) returns 1, test software writes the Attention Indicator Control field (Slot Control register) with 10b (Blink). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status).
 b. Test software checks the attention button for the slot currently under test by doing the following:
 i If the Attention Button Present field (Slot Capabilities register) returns 0, test software in manual mode then prompts the user to verify that there is no attention button for the slot under test, or test software in automatic mode checks the specified parameter to see if there is no attention button for the slot under test. If the user responds negatively, or if in automatic mode the specified parameter is negative, the test fails for this slot and the test continues with the next step.
 ii If the Attention Button Present field (Slot Capabilities register) returns 1, test software writes the Attention Button Pressed field (Slot Control register) with 1 to clear the previous status. Test software then prompts the user to press the attention button for the slot under test. Test software then checks that the Attention Button Pressed field (Slot Status register) returns 1 for the slot under test only and if it does not the test fails for this slot and the test continues with the next step. Test software writes the Attention Button Pressed field (Slot Status register) with 1 (to clear the status).
 iii Test software then checks that the Attention Button Pressed field (Slot Status register) returns 0 for each Downstream Port that has a PCI Express Capabilities register that has the Slot Implemented field (PCI Express Capabilities register) return 1, and if it does not the test fails for that individual slot and the test continues with the next step.
 c. Test software checks the mechanical retention latch for the slot currently under test by doing the following:
 i If the MRL Sensor Present field (Slot Capabilities register) returns 1, test software writes the MRL Sensor Changed field (Slot Status register) with 1 (to clear the status).
 ii If the MRL Sensor Present field (Slot Capabilities register) returns 1, test software reads the MRL Sensor State field (Slot Status register) and records its current value.

iii If the MRL Sensor Present field (Slot Capabilities register) returns 1, test software presents a message to the user, asking that they move the mechanical release latch for the slot under test to the opposite position.

iv If the MRL Sensor Present field (Slot Capabilities register) returns 1, test software checks that the MRL Sensor Changed field (Slot Status register) returns 1, and if it does not the test fails for this slot and the test continues with the next step. Test software writes the MRL Sensor Changed field (Slot Status register) with 1 (to clear the status).

v If the MRL Sensor Present field (Slot Capabilities register) returns 1, test software reads that the MRL Sensor State field (Slot Status register), and if it does not return the opposite value to the previously recorded value the test fails for this slot and the test continues with the next step.

d. Test software checks the attention indicator for the slot currently under test by doing the following:

i If the Attention Indicator Present field (Slot Capabilities register) returns 0, test software in manual mode then prompts the user to verify that there is no attention indicator for the slot under test, or test software in automatic mode checks the specified parameter to see if there is no attention indicator for the slot under test. If the user responds negatively, or if in automatic mode the specified parameter is negative, the test fails for this slot and the test continues with the next step.

ii If the Attention Indicator Present field (Slot Capabilities register) returns 1, test software writes the Attention Indicator Control field (Slot Control register) with 01b (On). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status). Test software checks the Attention Indicator Control field (Slot Control register) returns 01b (On), and if it does not the test fails for this slot and the test continues with the next step.

iii If the Attention Indicator Present field (Slot Capabilities register) returns 1, test software then prompts the user to verify that the attention indicator is fully on for the slot under test. If the user responds negatively, the test fails for this slot and the test continues with the next step.

iv If the Attention Indicator Present field (Slot Capabilities register) returns 1, test software writes the Attention Indicator Control field (Slot Control register) with 10b (Blink). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status). Test software checks the Attention Indicator Control field (Slot Control register) returns 10b (Blink), and if it does not the test fails for this slot and the test continues with the next step.

v If the Attention Indicator Present field (Slot Capabilities register) returns 1, test software then prompts the user to verify that the attention indicator is blinking for the slot under

test. If the user responds negatively, the test fails for this slot and the test continues with the next step.

vi If the Attention Indicator Present field (Slot Capabilities register) returns 1, test software writes the Attention Indicator Control field (Slot Control register) with 11b (Off). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status). Test software checks the Attention Indicator Control field (Slot Control register) returns 11b (Off), and if it does not the test fails for this slot and the test continues with the next step.

vii If the Attention Indicator Present field (Slot Capabilities register) returns 1, test software then prompts the user to verify that the attention indicator is fully off for the slot under test. If the user responds negatively, the test fails for this slot and the test continues with the next step.

viii If the Attention Indicator Present field (Slot Capabilities register) returns 1, test software writes the Attention Indicator Control field (Slot Control register) with 01b (On). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status). Test software checks the Attention Indicator Control field (Slot Control register) returns 01b (On), and if it does not the test fails for this slot and the test continues with the next step.

ix Test software suspends the system to S3 and then resumes it again.

x If the Attention Indicator Present field (Slot Capabilities register) returns 1, test software then checks the Attention Indicator Control field (Slot Control register) returns 01b (On), and if it does not the test fails for this slot and the test continues with the next step.

xi If the Attention Indicator Present field (Slot Capabilities register) returns 1, test software then prompts the user to verify that the attention indicator is still fully on for the slot under test. If the user responds negatively, the test fails for this slot and the test continues with the next step.

xii If the Attention Indicator Present field (Slot Capabilities register) returns 1, test software writes the Attention Indicator Control field (Slot Control register) with 10b (Blink). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status). Test software checks the Attention Indicator Control field (Slot Control register) returns 10b (Blink), and if it does not the test fails for this slot and the test continues with the next step.

xiii Test software suspends the system to S3 and then resumes it again.

xiv If the Attention Indicator Present field (Slot Capabilities register) returns 1, test software then checks the Attention Indicator Control field (Slot Control register) returns 10b (Blink), and if it does not the test fails for this slot and the test continues with the next step.

xv If the Attention Indicator Present field (Slot Capabilities register) returns 1, test software then prompts the user to verify that the attention indicator is still blinking for the slot under test. If the user responds negatively, the test fails for this slot and the test continues with the next step.

xvi If the Attention Indicator Present field (Slot Capabilities register) returns 1, test software writes the Attention Indicator Control field (Slot Control register) with 11b (Off). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status).

e. Test software checks the power indicator for the slot currently under test by doing the following:

i If the Power Indicator Present field (Slot Capabilities register) returns 0, test software in manual mode then prompts the user to verify that there is no power indicator for the slot under test, or test software in automatic mode checks the specified parameter to see if there is no power indicator for the slot under test. If in manual mode the user responds negatively, or if in automatic mode the specified parameter is negative, the test fails for this slot and the test continues with the next step.

ii If the Power Indicator Present field (Slot Capabilities register) returns 1, test software writes the Power Indicator Control field (Slot Control register) with 01b (On). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status). Test software checks the Power Indicator Control field (Slot Control register) returns 01b (On), and if it does not the test fails for this slot and the test continues with the next step.

iii If the Power Indicator Present field (Slot Capabilities register) returns 1, test software then prompts the user to verify that the power indicator is fully on for the slot under test. If the user responds negatively, the test fails for this slot and the test continues with the next step.

iv If the Power Indicator Present field (Slot Capabilities register) returns 1, test software writes the Power Indicator Control field (Slot Control register) with 10b (Blink). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field

(Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status). Test software checks the Power Indicator Control field (Slot Control register) returns 10b (Blink), and if it does not the test fails for this slot and the test continues with the next step.

v If the Power Indicator Present field (Slot Capabilities register) returns 1, test software then prompts the user to verify that the power indicator is blinking for the slot under test. If the user responds negatively, the test fails for this slot and the test continues with the next step.

vi If the Power Indicator Present field (Slot Capabilities register) returns 1, test software writes the Power Indicator Control field (Slot Control register) with 11b (Off). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status). Test software checks the Power Indicator Control field (Slot Control register) returns 11b (Off), and if it does not the test fails for this slot and the test continues with the next step.

vii If the Power Indicator Present field (Slot Capabilities register) returns 1, test software then prompts the user to verify that the power indicator is fully off for the slot under test. If the user responds negatively, the test fails for this slot and the test continues with the next step.

viii If the Power Indicator Present field (Slot Capabilities register) returns 1, test software writes the Power Indicator Control field (Slot Control register) with 01b (On). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status). Test software checks the Power Indicator Control field (Slot Control register) returns 01b (On), and if it does not the test fails for this slot and the test continues with the next step.

ix Test software suspends the system to S3 and then resumes it again.

x If the Power Indicator Present field (Slot Capabilities register) returns 1, test software then checks the Power Indicator Control field (Slot Control register) returns 01b (On), and if it does not the test fails for this slot and the test continues with the next step.

xi If the Power Indicator Present field (Slot Capabilities register) returns 1, test software then prompts the user to verify that the power indicator is still fully on for the slot under test. If the user responds negatively, the test fails for this slot and the test continues with the next step.

xii If the Power Indicator Present field (Slot Capabilities register) returns 1, test software writes the Power Indicator Control field (Slot Control register) with 10b (Blink). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is

skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status). Test software checks the Power Indicator Control field (Slot Control register) returns 10b (Blink), and if it does not the test fails for this slot and the test continues with the next step.

xiii Test software suspends the system to S3 and then resumes it again.

xiv If the Power Indicator Present field (Slot Capabilities register) returns 1, test software then checks the Power Indicator Control field (Slot Control register) returns 10b (Blink), and if it does not the test fails for this slot and the test continues with the next step.

xv If the Power Indicator Present field (Slot Capabilities register) returns 1, test software then prompts the user to verify that the power indicator is still blinking for the slot under test. If the user responds negatively, the test fails for this slot and the test continues with the next step.

xvi If the Power Indicator Present field (Slot Capabilities register) returns 1, test software writes the Power Indicator Control field (Slot Control register) with 11b (Off). If the No Command Completed Support field (Slot Capabilities register) is 0, test software polls the Command Completed field (Slot Status register) until it reads back a 1. If this does not occur after 1 second of polling, then the write to the Slot Control register is repeated. If this still does not occur after 10 repeats, the remainder of this step is skipped and the test continues with the next step. If the Command Completed field (Slot Status register) returns 1, test software writes the Command Completed field (Slot Status register) with 1 (to clear the status).

5. The test is repeated for each slot with a PCI Express device present in the slot and without any device present in the slot (if possible).

The test *fails* if:

- ❑ A slot has a visible attention button and does not accurately report its presence.
- ❑ Pressing the attention button for a slot does not cause the Attention Button Pressed field to update.
- ❑ Changing the MRL does not cause the MRL Sensor State field to indicate the changed position and the MRL Sensor Changed field to be set.
- ❑ A slot has a visible attention indicator and does not accurately report its presence.
- ❑ An attention indicator does not correctly latch a valid value written to its control register.
- ❑ An attention indicator does not transition to the state last written to its control register.
- ❑ An attention indicator does not return to the state it was in prior to a system suspend/resume cycle.
- ❑ A slot has a visible power indicator and does not accurately report its presence.
- ❑ A power indicator does not correctly latch a valid value written to its control register.
- ❑ A power indicator does not transition to the state last written to its control register.
- ❑ A power indicator does not return to the state it was in prior to a system suspend/resume cycle.

B.13 TD_3_8x Link Training Stress

Test TD_3_8x is no longer supported as it requires system to reboot while the test is running, which the test cannot support. It has been replaced by TD_3_8 which does not do a system reboot.

The test verifies that the function under test implements the Retrain Link (Link Control register) behavior as defined in the relevant specifications and can properly perform link retraining when the Retrain Link field is set. The test prompts the user to populate the slot under test.

Relevant Specifications

- *PCI Express Base Specification*

(See Section 1.3 for additional specification revision details.)

Applicable Device/Port Types

This test is run on downstream ports of Root Ports, Switch Downstream Ports, and PCI/PCI-X to PCI Express Bridges.

Starting Configuration

For a non-Root Port function under test, it is completely uninitialized following a reset, except that the bus number fields are initialized with valid numbers.

The immediate downstream device (the upstream port of the link connected to the function under test) is completely uninitialized following a reset.

Overview of Test Steps

Test software performs the following steps:

1. Test software checks that the function under test has a PCI Express Capabilities register that has the Slot Implemented field (PCI Express Capabilities register) return 1. If not, the remaining steps are skipped (this is not a failure, but the test result is reported as skipped).
2. Prompt the user to power down (if necessary) and install a PCI Express card in the physically exposed slot under test.
3. After a system reboot (if necessary) a reset of the secondary interface is initiated by test software through writing a 1 to the Secondary Bus Reset field in the function under test (for a Bridge, the Bridge Control register in the Bridge; for a Switch, the Bridge Control register in the Switch Downstream Port) using a WORD access, while preserving all the other fields in this register, and then writing a 0 using a WORD access, while preserving all the other fields in this register. (See Section 2.1.1.1.2 for details of the reset algorithm.)
4. Configure the function under test following the procedure described in Section 2.1.1.
5. Verify that a device is present in the slot.
6. Modify some non-sticky register field in the device in the slot to a non-default value. Any of the following fields can be used as long as they are implemented as RW in the target: Memory Space Enable (Command register); I/O Space Enable (Command register); Bus Master Enable (Command register); Interrupt Disable (Command register). If none of these fields are implemented as RW in the target, then other non-sticky RW fields can be used. If test software cannot find any non-sticky RW field in the target, then this step is skipped.

7. Test software reads the Negotiated Link Width field (Link Status register) for both the function under test and the device in the slot and records the values. If the two values do not agree, then the test fails and is terminated.
8. Test software reads the Current Link Speed field (Link Status register) for both the function under test and the device in the slot and records the values. If the two values do not agree, then the test fails and is terminated.
9. Test software writes a 1 to the Retrain Link field (Link Control register) of the function under test using a WORD access, while preserving all the other fields in this register.
10. The function under test is checked to see if it has completed training. Test software continuously reads the Link Training field in the Link Status register, and when it returns 0, go to the next step. If the Link Training field does not return 0 within 1 second, then the test fails, and the remaining steps are skipped.
11. Test software reads the Negotiated Link Width field (Link Status register) for both the function under test and the device in the slot and records the values. If the two values do not agree, then the test fails and is terminated. If the value does not match the previously read value, then the test fails and is terminated.
12. Test software reads the Current Link Speed field (Link Status register) for both the function under test and the device in the slot and records the values. If the two values do not agree, then the test fails and is terminated.
13. If a non-sticky RW register field was found in step 6, after the necessary delay, test software verifies the same non-sticky field (from step 6) in the device in the slot is not reset to its default value. If the value has changed to the default value, the test fails and is terminated.
14. Steps 9-13 are repeated for 100 iterations.
15. The entire test is repeated for all add-in card widths that can operate in the slot under test. For example, if the physical slot is x16 then x1, x4, x8, and x16 add-in cards are used (an interposer can be used to reduce the actual add-in card's width, in which case x2 and x12 may also be tested).

The test *fails* if:

- ❑ The reported negotiated link width of the function under test ever fails to match the negotiated link width of the device in the slot.
- ❑ The reported negotiated link speed of the function under test ever fails to match the negotiated link speed of the device in the slot.
- ❑ Link retraining causes the link to fail to complete link training.
- ❑ The reported negotiated link width of the function under test after link retraining fails to match the negotiated link width prior to link retraining.
- ❑ The reported negotiated link speed of the function under test after link retraining fails to match the negotiated link speed prior to link retraining.
- ❑ Link retraining causes the device in the slot to reset (restoring a non-sticky register field to its default value).

B.14 TD_3_9 Slot Capabilities 2, Slot Control 2, and Slot Status 2 Registers

Test TD_3_9 is now included as part of TD_1_50, as it must be run for all device/port types. The description of this test is identical to that provided for TD_1_50.

C

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